OEC Workstation Schematic Diagrams

This section provides schematic diagrams for the more complex GE OEC-built electronic modules, devices, and printed circuit boards described in this manual. The schematics are arranged in numeric order by drawing number.

Use the following alphabetic list to access a drawing by title. Click on the appropriate title or drawing number to view the drawing.

Cine Bridge PCB 00-880821
Cine Four-Disk Backplane PCB 00-879408
Cine Two-Disk Backplane PCB 00-879499
Control Panel Processor PCB 00-876611
DC Distribution PCB 00-879117
Display Adapter PCB 00-881445
Display Controller PCB 00-878955
External Interface PCB 00-879184
Image Processor PCB 00-879016
Infrared Receiver PCB 00-879378
Interconnect Diagram, Workstation 00-878981
Power Control PCB 00-880315
Surge Suppressor PCB 00-880538
System Interface PCB 00-879054
Video Controller PCB 00-879002

DWG NO.	SHT	REV
00-876611	1	A.1

M	ENGIN. REV. 1 REVISIONS		EDR
REV	DESCRIPTION	DATE	APPROVED
A	RELEASED TO MANUFACTURING PER ECO P630		
A.1	REVISED PER ECO AT35		

NOTES:

1. CCR BIT 1 MUST BE SET TO '1' FOR BUSWIDTH TO WORK PROPERLY.
2. THESE JUMPERS ARE FOR SELECTING CONFIGURATION OPTIONS.
3. INSTALL JUMPER 1-2 TO SELECT RS-232 TRANSCEIVER, 2-3 FOR RS-422. (4 PLACES)
4. UNLESS OTHERWISE SPECIFIED, ALL CAPACITANCE VALUES ARE IN MICRO-FARADS.
5. UNLESS OTHERWISE SPECIFIED, ALL RESISTOR VALUES ARE IN OHMS, 1/4W, 1%.

MEMORY MAP

PROGRAM MEMORY	0-7FFF	8-BIT	RD ONLY
CS_SRAM	8000-EFFF	8-BIT	RD/WR
ROW_DRV	F0XX	16-BIT	WR ONLY
COL_READ	F1XX	16-BIT	RD ONLY
LED_16-31_WR	F200-F3FF	16-BIT	WR ONLY
LED_00-15_WR	F400-F7FF	16-BIT	WR ONLY
DIAG_DISPLAY_WR	F800-FFFF	16-BIT	WR ONLY

-02 SHOWN
-01 INACTIVE

ITEM	QTY.	PART OR IDENT NO.	DESCRIPTION

PARTS LIST

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		CONTRACT NO.		APPROVED	DATE
		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS: +/- DECIMALS: .XX+/- .XXX+/- ANGLES: +/-	MATERIAL	DRAWN KEN JOHNSON	8/6/93
	9600		FINISH	CHECKED C. BALL	10/1/93
NEXT ASSEMBLY	USED ON			ENGINEERING KEN JOHNSON	8/6/93
APPLICATION		DO NOT SCALE DRAWING		APPROVED	

OEC MEDICAL SYSTEMS, INC.

DWG TITLE: CART CONTROL PANEL PROCESSOR SCHEMATIC DIAGRAM

SIZE: D | DWG NO.: 00-876611 | REV: A.1 | SCALE: NONE | SHEET 1 2

05-016-9/93

SHEET 1/B1 COL_READ

VCC

R40 2% 220

U23 74ABT573

AD<15..0>

P5 - 22 COL15IN
P5 - 21 COL14IN
P5 - 20 COL13IN
P5 - 19 COL12IN
P5 - 18 COL11IN
P5 - 17 COL10IN
P5 - 16 COL9IN
P5 - 15 COL8IN

R39 10K 2%

QWERTY

SHEET 1/B1 DIAG_DISPLAY_WR

U20 74ABT574

R29 100 2%

U21 74ABT574

R30 100 2%

DS1 LED_10BAR_YEL

R26 267

P6 - 14
P6 - 12
P6 - 10
P6 - 8
P6 - 5
P6 - 6
P6 - 2
P6 - 34
P6 - 20
P6 - 18

FRONT PANEL

P4 - 5
P4 - 4
P4 - 3
P4 - 2
P4 - 1

TRACK PANEL

QWERTY

VCC

R38 2% 220

U15 74ABT573

P5 - 14 COL7IN
P5 - 13 COL6IN
P5 - 12 COL5IN
P5 - 11 COL4IN
P5 - 10 COL3IN
P5 - 9 COL2IN
P5 - 8 COL1IN
P5 - 7 COL0IN

R35 10K 2%

U18 74ABT574

P5 - 32
P5 - 31
P5 - 30
P5 - 29
P5 - 28
P5 - 27
P5 - 26
P5 - 25

SD103 CR1 ROW11OUT P6 - 7
SD103 CR4 ROW10OUT P6 - 24
SD103 CR6 ROW9OUT P4 - 9
SD103 CR11 ROW8OUT P4 - 8

U22 74ABT574

SHEET 1/B1 ROW_DRV

P5 - 24
P5 - 23

SD103 CR13 ROW7OUT P4 - 7
SD103 CR10 ROW6OUT P4 - 6
SD103 CR8 ROW5OUT P5 - 6
SD103 CR3 ROW4OUT P5 - 5
SD103 CR2 ROW3OUT P5 - 4
SD103 CR7 ROW2OUT P5 - 3
SD103 CR9 ROW1OUT P5 - 2
SD103 CR12 ROW0OUT P5 - 1

R34 267

SHEET 1/D1 AD<15..0>
SHEET 1/B1 LED_16-31_WR
SHEET 1/B1 LED_00-15_WR

VCC

P4 - 30
P4 - 10
P6 - 1

U17 74ABT574

R37 100 2%

LED_31 P4 - 32
LED_30 P4 - 31
LED_29 P4 - 24
LED_28 P4 - 23
LED_27 P4 - 22
LED_26 P4 - 21
LED_25 P4 - 20
LED_24 P4 - 19

TRACK-PANEL LEDS

U16 74ABT574

R36 100 2%

LED-23 P4 - 18
LED-22 P4 - 17
LED-21 P4 - 16
LED-20 P4 - 15
LED-19 P4 - 14
LED-18 P4 - 13
LED-17 P4 - 12
LED-16 P4 - 11

TRACK_PANEL LEDS

U19 74ABT574

R28 100 2%

LED-15 P6 - 30
LED-14 P6 - 29
LED-13 P6 - 28
LED-12 P6 - 27
LED-11 P6 - 26
LED-10 P6 - 25
LED-9 P6 - 22
LED-8 P6 - 19

FRONT-PANEL LEDS

U12 74ABT574

R24 100 2%

LED-7 P6 - 17
LED-6 P6 - 15
LED-5 P6 - 16
LED-4 P6 - 13
LED-3 P6 - 11
LED-2 P6 - 9
LED-1 P6 - 4
LED-0 P6 - 3

FRONT-PANEL LEDS

R31 267

REFERENCE DESIGNATIONS

HIGHEST	UNUSED
C34	
CR13	
E13	
P7	
R40	
TP14	
U24	
Y1	

REF DESIGNATIONS	DEVICE	GND	GND	+5V	UNUSED
U5	80C196	14, 36	68	1	
U10	27C256	14		28	
U9	HCPL-4661	5		8	
U1	TC55328	14		28	
U2, 11, 15, 23	ABT573	10		20	
U24	MAX694	SHOWN		SHOWN	
U4	PAL22V10	12		24	
U8	MC3486	8		16	
U6	MC3487	8		16	
U12	74AC14	7		14	
U7	MAX233	6, 9		7	
U3	74LS08	7		14	
U14	L293D	4, 5	12, 13	SHOWN	
U13, 16-22	ABT574	10		20	

OEC MEDICAL SYSTEMS, INC.

SIZE	DWG NO.	REV
D	00-876611	A.1

SCALE: NONE SHEET 2 OF 2

05-017-9/93

PCI BUS INTERFACE

PCI BUS CONNECTOR

(FOR POWER & GND SEE SHEET 10)
(For connector detail see sheet 8)

P1 - A1 ← PCI_TRST* → JTAG_TRST* (OUT)
P1 - B2 ← PCI_TCK → JTAG_TCK (OUT)
P1 - A3 ← PCI_TMS → JTAG_TMS (OUT)
P1 - A4 ← PCI_TDI → JTAG_TDI (OUT)
P1 - B4 ← PCI_TDO → JTAG_TDO (IN)
P1 - B9 ← PRSNT1*
P1 -B11 ← PRSNT2*

P1 -A15 ← RST* → 148 RST
P1 -B16 ← CLK → 149 CLK

P1 -B39 ← LOCK* → 18 LOCK
P1 - A6 ← INTA* → 44 INTA
P1 -A43 ← PAR → 21 PAR
P1 -B40 ← PERR* → 19 PERR
P1 -B42 ← SERR* → 20 SERR

P1 -A26 ← IDSEL → 159 IDSEL
P1 -A34 ← FRAME* → 13 FRAME
P1 -B35 ← IRDY* → 14 IRDY
P1 -A36 ← TRDY* → 15 TRDY
P1 -A38 ← STOP* → 17 STOP
P1 -B37 ← DEVSEL* → 16 DEVSEL

P1 -B26 ← C/BE<3>* → C/BE<3..0>n
P1 -B33 ← C/BE<2>*
P1 -B44 ← C/BE<1>*
P1 -A52 ← C/BE<0>*

P1 -B20 ← AD<31> → AD<31..0>
P1 -A20 ← AD<30>
P1 -B21 ← AD<29>
P1 -A22 ← AD<28>
P1 -B23 ← AD<27>
P1 -A23 ← AD<26>
P1 -B24 ← AD<25>
P1 -A25 ← AD<24>
P1 -B27 ← AD<23>
P1 -A28 ← AD<22>
P1 -B29 ← AD<21>
P1 -A29 ← AD<20>
P1 -B30 ← AD<19>
P1 -A31 ← AD<18>
P1 -B32 ← AD<17>
P1 -A32 ← AD<16>
P1 -A44 ← AD<15>
P1 -B45 ← AD<14>
P1 -A46 ← AD<13>
P1 -B47 ← AD<12>
P1 -A47 ← AD<11>
P1 -B48 ← AD<10>
P1 -A49 ← AD<9>
P1 -B52 ← AD<8>
P1 -B53 ← AD<7>
P1 -A54 ← AD<6>
P1 -B55 ← AD<5>
P1 -A55 ← AD<4>
P1 -B56 ← AD<3>
P1 -A57 ← AD<2>
P1 -B58 ← AD<1>
P1 -A58 ← AD<0>

PCI BUS NO-CONNECT PINS

P1 - B7 ← N.C. INTB*
P1 - A7 ← N.C. INTC*
P1 - B8 ← N.C. INTD*
P1 - A9 ← N.C. RESERVED
P1 -B10 ← N.C. RESERVED
P1 -A11 ← N.C. RESERVED
P1 -A14 ← N.C. RESERVED
P1 -B14 ← N.C. RESERVED
P1 -A19 ← N.C. RESERVED
P1 -B18 ← N.C. REQ*
P1 -A17 ← N.C. GNT*
P1 -A41 ← N.C. SBO*
P1 -A40 ← N.C. SDONE
P1 -A60 ← N.C. REQ64*
P1 -B60 ← N.C. ACK64*

DISPLAY RESET — TP58 WHT
PCI BUS CLK — TP59 WHT
TP57 WHT LOCAL INTR 2
TP56 WHT LOCAL INTR 1
PLX_WR* TP55 WHT
PLX_RD* TP54 WHT
LRDY* TP53 WHT
CS 2* TP52 WHT
CS 1* TP60 WHT
CS 0* TP48 WHT

VCC
R58 0.25W 2% 4.7K (10 9 8 7 6 5 4 3 2)
R55 0.25W 2% 4.7K (10 9 8 7 6 5 4 3 2)
R54 0.25W 2% 330 (10 9 8 7 6 5 4 3 2)

R56 75 1% 0.125W
C459 330P 100V
R161 100

SEE SHEET 13 (PLX9050), U43

PCI9050_32BIT

LRESET	132	LW/Rn	127
BCLKO	63	WR	125
LCLK	135	RD	126
LINT2	136	BTERM	129
LINT1	137	LRDYI	128
LHOLD	134	BLAST	124
LHOLDA	133	LLOCK	139
		USER1	
		WAITO	138
		USER0	
		ADS	123
		ALE	64
		USER3	141
		CS3	
		USER2	140
		CS2	
		CS1	131
		CS0	130
		LBE<3..0>n	
		LA<27..2>	
		LAD<31..0>	
EESK	144		
EECS	142		
EEDI	145		
EEDO	143		
TEST	99		
MODE	68		

U42 NM93CS46: SK 2, CS 1, DI 3, DO 4, PE 6, PRE 7
R169 2K
R168 475
R160 475
R167 475

R60 10K (PLX_LD<31>, PLX_LD<30>, PLX_LD<29>, PLX_LD<28>, PLX_LD<27>, PLX_LD<26>, PLX_LD<25>, PLX_LD<24>)
R59 10K (PLX_LD<23>, PLX_LD<22>, PLX_LD<21>, PLX_LD<20>, PLX_LD<19>, PLX_LD<18>, PLX_LD<17>, PLX_LD<16>)
R47 10K (PLX_LD<15>, PLX_LD<14>, PLX_LD<13>, PLX_LD<12>, PLX_LD<11>, PLX_LD<10>, PLX_LD<9>, PLX_LD<8>)
R48 10K (PLX_LD<7>, PLX_LD<6>, PLX_LD<5>, PLX_LD<4>, PLX_LD<3>, PLX_LD<2>, PLX_LD<1>, PLX_LD<0>)

EPP_IRQ*
PLX_LRESET* (IN)
PLX_BCLKO (OUT)
MUXED_CLK (OUT)
PLX_LINT2* (IN)
PLX_LINT1 (IN)

PLX_LW_RD* (OUT)
PLX_LWR* (OUT)
PLX_LRD* (OUT)
PLX_BTERM* (IN)
PLX_LRDY* (IN)
PLX_BLAST* (OUT)
LPT_RESET (OUT)
PLX_LWAIT0* (OUT)
PLX_ADS* (OUT)
PLX_ALE (OUT)
PLX_CS3*
PLX_CS2* (OUT)
PLX_CS1* (OUT)
PLX_CS0* (OUT)
PLX_LBE<3..0>
PLX_LA<27..2> (OUT)
PLX_LD<31..0> (BI)
PLX_LOAD_OK* (OUT)
PLX_LFT_PIX_SEL* (IN)
PLX_RT_PIX_SEL* (IN)
PLX_LFT_PIXDATA_RD* (IN)
PLX_RT_PIXDATA_RD* (IN)

U15 74FCT162245T
OE2, DIR2 [BA], DIR2 [AB], OE1, DIR1 [AB], DIR1 [BA]
PLX_LA<14..4> (14..4) → PLX_LA<3> 3, PLX_LA<2> 2, PLX_LBE<1> 1, PLX_LBE<0> 0
PLX_8BIT_LA<14..0> (OUT)

PLX_LD<7> 26 → A7 → B7 23 → LEFT_PIX_DATA<7> 7
PLX_LD<6> 27 → A6 → B6 22 → LEFT_PIX_DATA<6> 6
PLX_LD<5> 29 → A5 → B5 20 → LEFT_PIX_DATA<5> 5
PLX_LD<4> 30 → A4 → B4 19 → LEFT_PIX_DATA<4> 4
PLX_LD<3> 32 → A3 → B3 17 → LEFT_PIX_DATA<3> 3
PLX_LD<2> 33 → A2 → B2 16 → LEFT_PIX_DATA<2> 2
PLX_LD<1> 35 → A1 → B1 14 → LEFT_PIX_DATA<1> 1
PLX_LD<0> 36 → A0 → B0 13 → LEFT_PIX_DATA<0> 0
LEFT_PIX_DATA<7..0> (BI)

PLX_LD<7> 37 → A7 → B7 12 → RT_PIX_DATA<7> 7
PLX_LD<6> 38 → A6 → B6 11 → RT_PIX_DATA<6> 6
PLX_LD<5> 40 → A5 → B5 9 → RT_PIX_DATA<5> 5
PLX_LD<4> 41 → A4 → B4 8 → RT_PIX_DATA<4> 4
PLX_LD<3> 43 → A3 → B3 6 → RT_PIX_DATA<3> 3
PLX_LD<2> 44 → A2 → B2 5 → RT_PIX_DATA<2> 2
PLX_LD<1> 46 → A1 → B1 3 → RT_PIX_DATA<1> 1
PLX_LD<0> 47 → A0 → B0 2 → RT_PIX_DATA<0> 0
RT_PIX_DATA<7..0> (BI)

U15 A BUFFER: A2 1, A1 2

DWG NO.	SHT	REV
00-878955	1	A

M	ENGIN. REV. 4.1 REVISIONS		EDR 01346
REV	DESCRIPTION	DATE	APPROVED
A	RELEASED TO MANUFACTURING PER ECO BD87		

DRAWING
LAST_MODIFIED=Thu May 21 10:58:15 1998

ITEM	QTY.	PART OR IDENT NO.	DESCRIPTION

PARTS LIST

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00-878980	9800
NEXT ASSEMBLY	USED ON
APPLICATION	

CONTRACT NO.
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS: +/-
DECIMALS: .XX +/-
.XXX +/-
ANGLES: +/-
MATERIAL
FINISH
DO NOT SCALE DRAWING

	APPROVED	DATE
DRAWN	B. SPRATT	10-24-96
CHECKED	N. NEWBOLD	4-22-97
ENGINEERING	B. SPRATT	4-22-97
APPROVED		

OEC MEDICAL SYSTEMS, INC.
DWG TITLE: 9800 DISPLAY CONTROLLER
SIZE D | DWG NO. 00-878955 | REV A
SCALE: | SHEET 1 OF 22

05-016-9-93

IP INTERFACE

DISPLAY CLOCK SELECTOR/BUFFER

TP18 PIXCLK* WHT

TP19 MUXED CLOCK WHT

U10 49FCT806T

IP_CLK_SEL*

PLX_BCLK0_SEL*

P9 - 42 IP_DIS_PIXCLK

PLX_BCLK0

R98 10K, R97 10K, R38 10K, VCC, 0 5% 0.125W R27

MON, INB, INA, OB4, OB3, OB2, OB1, OB0, OA4, OA3, OA2, OA1, OA0

R96 75, R26 75, C82 330P 100V, C83 330P 100V

IP_RT_SEL* TP43 WHT

IP_LFT_SEL* TP28 WHT

MUXED_CLK

R28 0, R95 0, R29 0, R94 0, R30 0

LFT_MUXED_CLK_A, LFT_MUXED_CLK_B, RT_MUXED_CLK_A, RT_MUXED_CLK_B, IP_AUX_PIX_SEL*, IP_RT_PIX_SEL*, IP_LFT_PIX_SEL*

IP INTERFACE CONNECTOR

NO CONNECT → 4 - P9
NO CONNECT → 5 - P9
NO CONNECT → 17 - P9
NO CONNECT → 27 - P9
NO CONNECT → 28 - P9
NO CONNECT → 39 - P9
NO CONNECT → 40 - P9

CONNECTOR GNDS

1 - P9, 2 - P9, 3 - P9, 41 - P9, 43 - P9, 44 - P9, 45 - P9, 46 - P9, 47 - P9, 48 - P9, 49 - P9, 50 - P9, 51 - P9, 52 - P9, 53 - P9, 54 - P9, 55 - P9, 56 - P9, 57 - P9, 58 - P9, 59 - P9, 60 - P9, 61 - P9, 62 - P9, 63 - P9, 64 - P9, 65 - P9, 66 - P9, 67 - P9, 68 - P9, 69 - P9, 70 - P9, 71 - P9, 72 - P9, 73 - P9, 74 - P9, 75 - P9, 76 - P9, 77 - P9, 78 - P9, 79 - P9, 80 - P9

U12 74FCT574A

P9 - 7 LD_D7, P9 - 8 LD_D6, P9 - 9 LD_D5, P9 - 10 LD_D4, P9 - 11 LD_D3, P9 - 12 LD_D2, P9 - 13 LD_D1, P9 - 14 LD_D0

D7 07, D6 06, D5 05, D4 04, D3 03, D2 02, D1 01, D0 00

LEFT_PIX_DATA<7>, LEFT_PIX_DATA<6>, LEFT_PIX_DATA<5>, LEFT_PIX_DATA<4>, LEFT_PIX_DATA<3>, LEFT_PIX_DATA<2>, LEFT_PIX_DATA<1>, LEFT_PIX_DATA<0>

LEFT_PIX_DATA<7..0>

R93 75, C80 330P 100V, R92 75, C78 330P 100V, R91 75, C77 330P 100V, R90 75, C76 330P 100V, R89 75, C75 330P 100V, R88 75, C74 330P 100V, R87 75, C73 330P 100V, R86 75, C72 330P 100V

U16 74FCT574A

P9 - 19 RD_D7, P9 - 20 RD_D6, P9 - 21 RD_D5, P9 - 22 RD_D4, P9 - 23 RD_D3, P9 - 24 RD_D2, P9 - 25 RD_D1, P9 - 26 RD_D0

RT_PIX_DATA<7>, RT_PIX_DATA<6>, RT_PIX_DATA<5>, RT_PIX_DATA<4>, RT_PIX_DATA<3>, RT_PIX_DATA<2>, RT_PIX_DATA<1>, RT_PIX_DATA<0>

RT_PIX_DATA<7..0>

R85 75, C71 330P 100V, R84 75, C70 330P 100V, R83 75, C69 330P 100V, R82 75, C68 330P 100V, R81 75, C67 330P 100V, R80 75, C66 330P 100V, R79 75, C65 330P 100V, R78 75, C64 330P 100V

U17 74FCT574A

P9 - 31 AD_D7, P9 - 32 AD_D6, P9 - 33 AD_D5, P9 - 34 AD_D4, P9 - 35 AD_D3, P9 - 36 AD_D2, P9 - 37 AD_D1, P9 - 38 AD_D0

AUX_PIX_DATA<7>, AUX_PIX_DATA<6>, AUX_PIX_DATA<5>, AUX_PIX_DATA<4>, AUX_PIX_DATA<3>, AUX_PIX_DATA<2>, AUX_PIX_DATA<1>, AUX_PIX_DATA<0>

AUX_PIX_DATA<7..0>

R77 75, C63 330P 100V, R76 75, C62 330P 100V, R75 75, C61 330P 100V, R74 75, C60 330P 100V, R73 75, C59 330P 100V, R72 75, C58 330P 100V, R71 75, C57 330P 100V, R70 75, C56 330P 100V

U14 74FCT574A

P9 - 15 DC_HDRV*, P9 - 16 DC_VDRV*, P9 - 6 LD_WREN*, P9 - 18 RD_WREN*, P9 - 30 AD_WREN*, P9 - 29 TAG*

HDRV_IN*, VDRV_IN*, L_PIXWE_IN*, R_PIXWE_IN*, AUX_PIXWE_IN*, IP_DATA_TAG*

R31 75, C160 330P 100V, R32 75, C158 330P 100V, R33 75, C155 330P 100V, R34 75, C154 330P 100V, R35 75, C152 330P 100V, R36 75, C150 330P 100V

R139 75 1% 0.125W, C140 330P 100V

R37 475

DRAWING

LAST_MODIFIED=Thu May 21 11:13:26 1998

OEC MEDICAL SYSTEMS, INC.

SIZE	DWG NO.	REV
D	00-878955	A

SCALE: | SHEET 2 OF 22

05-017-9/93

LEFT CHANNEL VIDEO DAC & OUTPUT

TP10 L_1.2V REF
TP25 L_PLL +5
TP26 L_PLL GND
TP2 ANALOG +5
TP7 ANALOG GND
TP6 ANALOG -5
PACK_TYPE=TO220HU
PHASE LOCKED LOOP +5V
ANALOG GND RAIL
ANALOG +5V RAIL
ANALOG -5V RAIL
ANALOG AND DIGITAL GROUND PLANES COMMON AT THIS POINT
TVP3030
SEE SHEET 14 (RAMDAC3), U4
MAX499
L_DAC_RESET*
L_DAC_RD*
L_DAC_WR*
PLX_8BIT_LA<3..0>
PLX_LD<7..0>
L_DAC_LCLK
L_DISPLAY_DATA<31..0>
L_DISPLAY_DATA<127..32>
L_DISPLAY_DATA<127..0>
L_VGA<7..0>
L_PLL FREQ
L_H SYNC*
L_V SYNC*
LFT_MUXED_CLK_B
L_DAC_HSYNC*
L_DAC_VSYNC*
L_DAC_BLANK*
L_VIDEO_ACTIVE_LED*
L_DAC_RCLK
LFT_RCLK
COMP_VGA_VIDEO
L_VGA_SEL
LEFT MONITOR VIDEO
LEFT INTERNAL FAST SCAN MONITOR
LEFT EXTERNAL FAST SCAN MONITOR
BACK-PANEL LEFT CONNECTOR

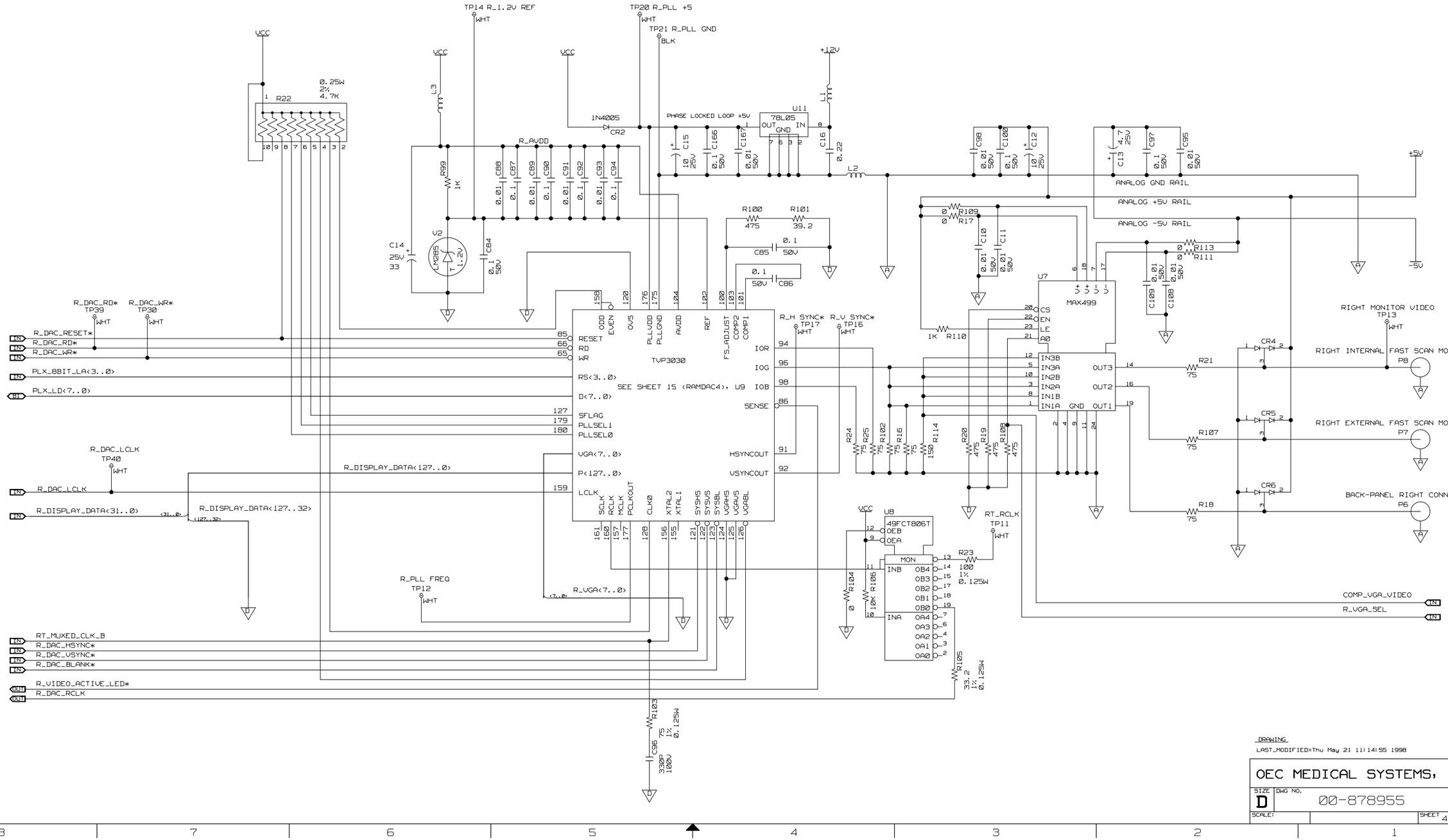
DRAWING
LAST_MODIFIED=Thu May 21 11:14:22 1998

OEC MEDICAL SYSTEMS, INC.

SIZE	DWG NO.	REV
D	00-878955	A
SCALE:		SHEET 3 OF 22

05-017-9/93

RIGHT CHANNEL VIDEO DAC & OUTPUT



DRAWING
LAST_MODIFIED=Thu May 21 11:14:55 1998

OEC MEDICAL SYSTEMS, INC.

SIZE	DWG NO.	REV
D	00-878955	A
SCALE:	SHEET 4 OF 22	

05-817-9/93

LEFT CHANNEL MASTER SLAVE FRAME BUFFER

L_SVR_RAS*
L_SVR_CAS*
L_SVR_WE<4>*
L_SVR_WE<3>*
L_SVR_WE<2>*
L_SVR_WE<1>*

L_MVR_RAS*
L_MVR_CAS*
L_MVR_WE<4>*
L_MVR_WE<3>*
L_MVR_WE<2>*
L_MVR_WE<1>*
L_MVR_SCLK
L_MVR_SCLK_EN*
L_MVR_DSF
L_MVR_DTOE*
L_FIFO_MBA
L_FIFO_ENA
L_FIFO_AEA*
L_FIFO_EFA*
L_FIFO_AFA*
L_FIFO_FFA*
L_FIFO_A_W/R*
L_FIFO_CSA*
L_FIFO_RESET*
LFT_MUXED_CLK_A

VCC
VCC

R152 2K
R151 2K

U26
FIFO 64X36X2 BMBS SPEED=20_NS

L_FIFO_SIZE1
L_FIFO_SIZE0
L_FIFO_CSB*
L_FIFO_B_W/R*
L_FIFO_ENB
L_FIFO_FFB*
L_FIFO_AFB*
L_FIFO_EFB*
L_FIFO_AEB*

SIZ1 SIZ0 SW1 SW0 BE CLKB CSB W/RnB ENB PGB FFB AFB EFB AEB PEFB MBF1
RST ODD EVEN FS1 FS0 CLKA CSA W/RnA ENA MBA PGA FFA AFA EFA AEA PEFA MBF2

PLX_LD<31..0>
B35 B34 B33 B32 B31 B30 B29 B28 B27 B26 B25 B24 B23 B22 B21 B20 B19 B18 B17 B16 B15 B14 B13 B12 B11 B10 B9 B8 B7 B6 B5 B4 B3 B2 B1 B0

LEFT_PIX_WE*
LEFT_PIX_DATA<7..0>
L_MVR_A<8..0>
L_SVR_A<8..0>

A35 A34 A33 A32 A31 A30 A29 A28 A27 A26 A25 A24 A23 A22 A21 A20 A19 A18 A17 A16 A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0

L_PIX_DATA<31..0>

LEFT MASTER
U21
VRAM 256KX16

RAS CAS WEU WEL TRG DSF SC SE QSF
A8 A7 A6 A5 A4 A3 A2 A1 A0
DQ15 DQ14 DQ13 DQ12 DQ11 DQ10 DQ09 DQ08 DQ07 DQ06 DQ05 DQ04 DQ03 DQ02 DQ01 DQ00
SQ15 SQ14 SQ13 SQ12 SQ11 SQ10 SQ09 SQ08 SQ07 SQ06 SQ05 SQ04 SQ03 SQ02 SQ01 SQ00
NC

L_MVR_A<8> L_MVR_A<7> L_MVR_A<6> L_MVR_A<5> L_MVR_A<4> L_MVR_A<3> L_MVR_A<2> L_MVR_A<1> L_MVR_A<0>
L_PIX_DATA<31> L_PIX_DATA<30> L_PIX_DATA<29> L_PIX_DATA<28> L_PIX_DATA<27> L_PIX_DATA<26> L_PIX_DATA<25> L_PIX_DATA<24> L_PIX_DATA<23> L_PIX_DATA<22> L_PIX_DATA<21> L_PIX_DATA<20> L_PIX_DATA<19> L_PIX_DATA<18> L_PIX_DATA<17> L_PIX_DATA<16> L_PIX_DATA<15> L_PIX_DATA<14> L_PIX_DATA<13> L_PIX_DATA<12> L_PIX_DATA<11> L_PIX_DATA<10> L_PIX_DATA<9> L_PIX_DATA<8> L_PIX_DATA<7> L_PIX_DATA<6> L_PIX_DATA<5> L_PIX_DATA<4> L_PIX_DATA<3> L_PIX_DATA<2> L_PIX_DATA<1> L_PIX_DATA<0>
L_DISPLAY_DATA<31> L_DISPLAY_DATA<30> L_DISPLAY_DATA<29> L_DISPLAY_DATA<28> L_DISPLAY_DATA<27> L_DISPLAY_DATA<26> L_DISPLAY_DATA<25> L_DISPLAY_DATA<24> L_DISPLAY_DATA<23> L_DISPLAY_DATA<22> L_DISPLAY_DATA<21> L_DISPLAY_DATA<20> L_DISPLAY_DATA<19> L_DISPLAY_DATA<18> L_DISPLAY_DATA<17> L_DISPLAY_DATA<16>

LEFT SLAVE
U23
VRAM 256KX16

L_SVR_A<8> L_SVR_A<7> L_SVR_A<6> L_SVR_A<5> L_SVR_A<4> L_SVR_A<3> L_SVR_A<2> L_SVR_A<1> L_SVR_A<0>
L_PIX_DATA<31> L_PIX_DATA<30> L_PIX_DATA<29> L_PIX_DATA<28> L_PIX_DATA<27> L_PIX_DATA<26> L_PIX_DATA<25> L_PIX_DATA<24> L_PIX_DATA<23> L_PIX_DATA<22> L_PIX_DATA<21> L_PIX_DATA<20> L_PIX_DATA<19> L_PIX_DATA<18> L_PIX_DATA<17> L_PIX_DATA<16>
L_DISPLAY_DATA<31> L_DISPLAY_DATA<30> L_DISPLAY_DATA<29> L_DISPLAY_DATA<28> L_DISPLAY_DATA<27> L_DISPLAY_DATA<26> L_DISPLAY_DATA<25> L_DISPLAY_DATA<24> L_DISPLAY_DATA<23> L_DISPLAY_DATA<22> L_DISPLAY_DATA<21> L_DISPLAY_DATA<20> L_DISPLAY_DATA<19> L_DISPLAY_DATA<18> L_DISPLAY_DATA<17> L_DISPLAY_DATA<16>

U22 VRAM 256KX16
U24 VRAM 256KX16

L_SVR_SCLK_EN*
L_SVR_SCLK
L_SVR_DSF
L_SVR_DTOE*
L_SVR_QSF

L_DISPLAY_DATA<31..0>

DRAWING
LAST_MODIFIED=Thu May 21 11:15:31 1998

OEC MEDICAL SYSTEMS, INC.

SIZE	DWG NO.	REV
D	00-878955	A
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RIGHT CHANNEL MASTER SLAVE FRAME BUFFER

R_SVR_RAS*
R_SVR_CAS*
R_SVR_WE<4>*
R_SVR_WE<3>*
R_SVR_WE<2>*
R_SVR_WE<1>*

R_MVR_RAS*
R_MVR_CAS*
R_MVR_WE<4>*
R_MVR_WE<3>*
R_MVR_WE<2>*
R_MVR_WE<1>*
R_MVR_SCLK
R_MVR_SCLK_EN*
R_MVR_DSF
R_MVR_DTOE*
R_FIFO_MBA
R_FIFO_ENA
R_FIFO_AEA*
R_FIFO_EFA*
R_FIFO_AFA*
R_FIFO_FFA*
R_FIFO_A_W/R*
R_FIFO_CSA*
R_FIFO_RESET*
RT_MUXED_CLK_A

VCC
R156 2K
R150 2K

U31
FIFO 64X36X2 BMBS
SPEED=20_NS

R_FIFO_SIZE1
R_FIFO_SIZE0
R_FIFO_CSB*
R_FIFO_B_W/R*
R_FIFO_ENB

R_FIFO_FFB*
R_FIFO_AFB*
R_FIFO_EFB*
R_FIFO_AEB*

PLX_LD<31..0>

RT_PIX_WE*

RT_PIX_DATA<7..0>
R_MVR_A<8..0>
R_SVR_A<8..0>

RIGHT MASTER

U27 VRAM 256KX16
U28 VRAM 256KX16

R_PIX_DATA<31..0>

RIGHT SLAVE

U29 VRAM 256KX16
U30 VRAM 256KX16

R_SVR_SCLK_EN*
R_SVR_SCLK
R_SVR_DSF
R_SVR_DTOE*
R_SVR_QSF

R_DISPLAY_DATA<31..0>

DRAWING
LAST_MODIFIED=Thu May 21 12:27:48 1998

OEC MEDICAL SYSTEMS, INC.

SIZE	DWG NO.	REV
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05-017-9/93

EXPANSION ROM, STATUS LEDS, REVISION JUMPERS, VGA INPUT, AND EPP PRINTER PORT

U35 27C256 EPROM 32768x8 — VPP, PGM, CS & OE, EN, A14–A0, D7–D0

EXP_ROM_CS*, EXP_ROM_OE*

PLX_8BIT_LA<14..0>, PLX_LD<7..0>

EPP_IOCHRDY* TP33 WHT, EPP_IRQ* TP50 WHT, EPP_RESET TP49 WHT

REVISION CONTROL

TO SET REVISION NUMBER,
FORM BINARY NUMERIC EQUIVALENT
BY REMOVING 15 OHM RESISTORS.
ALL RESISTORS PRESENT = 0
ALL RESISTORS REMOVED = 255

R46 10K

R141 128, R142 64, R143 32, R144 16, R145 8, R146 4, R147 2, R148 1 — 15

U13 74FCT244 — EN 2, EN 1, A3–A0, Y3–Y0

PLX_LD<31..0>, PCB_CFG_RD*, PLX_8BIT_LA<14..0>, EPP_IOCHRDY*, EPP_IRQ*, LPT_RESET, PLX_LRD*, PLX_LWR*, PLX_CS2*

U34 ST78C36 — CLOCK, RESET, IOR, IOW, AEN, CS, DACK, TC, IRQ, IOCHRDY, DRQ, PDIR

R164 2K

24MHZ Y1 — CLK, VCC, EN

R153 2K, C321 0.1, C320 0.01, FL2 EMI FL 7A 50V

ENHANCED PARALLEL PORT

PE, ACK*, BUSY, SLCT, ERROR*, SLCTI*, INIT, AFDXT*, STROBE* → P11 - 12, P11 - 10, P11 - 11, P11 - 13, P11 - 15, P11 - 17, P11 - 16, P11 - 14, P11 - 1

PLX_8BIT_LA<10>, PLX_8BIT_LA<2>, PLX_8BIT_LA<1>, PLX_8BIT_LA<0>

PLX_LD<7..0> → D7–D0 / PD7–PD0

PACK_TYPE=PLCC

R51, R49, R53, R52, R165, R50, R63, R62 33.2

PD7 → P11 - 9, PD6 → P11 - 8, PD5 → P11 - 7, PD4 → P11 - 6, PD3 → P11 - 5, PD2 → P11 - 4, PD1 → P11 - 3, PD0 → P11 - 2

C463, C466, C465, C464, C467, C468, C498, C499 180P → P11 - 18, P11 - 19, P11 - 20, P11 - 21, P11 - 22, P11 - 23, P11 - 24, P11 - 25

VGA INPUT CONNECTOR

RED	P15 - 1	← N.C.
GREEN	P15 - 2	← VGA_GREEN
BLUE	P15 - 3	← VGA_BLUE
N.C.	P15 - 4	← N.C.
DIGITAL GND	P15 - 5	
RED RETURN	P15 - 6	← N.C.
GREEN RETURN	P15 - 7	← GREEN_RETURN
BLUE RETURN	P15 - 8	← BLUE_RETURN
N.C.	P15 - 9	← N.C.
DIGITAL GND	P15 - 10	
N.C.	P15 - 11	← N.C.
N.C.	P15 - 12	← N.C.
H. DRIVE	P15 - 13	
V. DRIVE	P15 - 14	
N.C.	P15 - 15	← N.C.

E1 → COMP_VGA_VIDEO

R41 75, R45 75, R43 1K, CR3 BAT54C, N.C.

U20 CA3246 ×4

R40 475, R39 200, R42 1K, R44 200 → -5V

VGA_XIN1, VGA_XIN2, VGA_XOUT

U18 74ABT240 — OE 2, OE 1, A3–A0, Y3–Y0

PLX_LOAD_OK*, L_UNBLANK_LED*, L_IP_ACTIVE_LED*, L_VIDEO_ACTIVE_LED*, TV_CONF_DONE, R_UNBLANK_LED*, R_IP_ACTIVE_LED*, R_VIDEO_ACTIVE_LED*

LEFT CHANNEL CONF_STATUS INDICATORS — DS1 → PLX LOAD OK, UNBLANK, IP, VIDEO

RIGHT CHANNEL CONF_STATUS INDICATORS — DS2 → ALTERA LOAD OK, UNBLANK, IP, VIDEO

R69 475

_DRAWING

LAST_MODIFIED=Thu May 21 12:28:25 1998

OEC MEDICAL SYSTEMS, INC.

SIZE	DWG NO.	REV
D	00-878955	A

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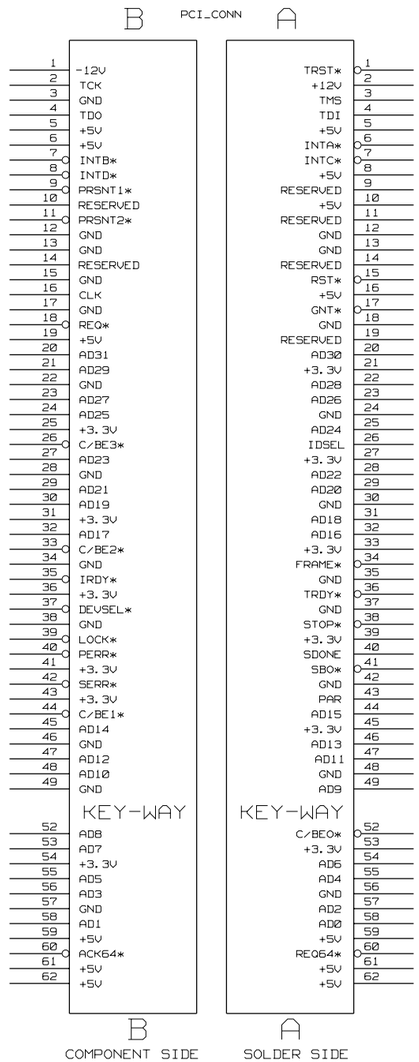
PCI-BUS CONNECTOR DETAILS



DRAWING

LAST_MODIFIED=Thu May 21 12:29:10 1998

OEC MEDICAL SYSTEMS, INC.

SIZE	DWG NO.	REV
D	00-878955	A

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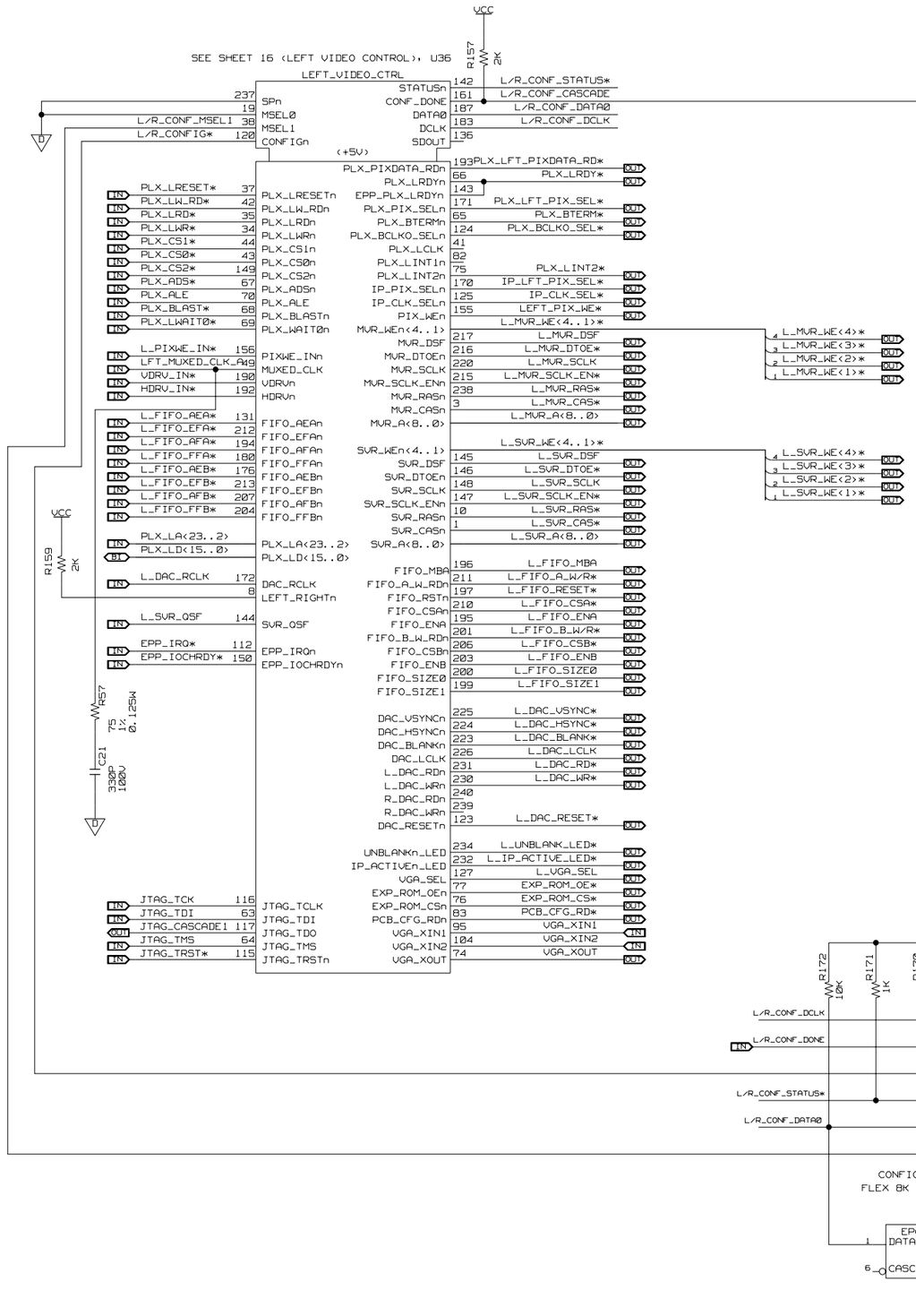

DRAWING
LAST_MODIFIED=Thu May 21 12:30:05 1998

OEC MEDICAL SYSTEMS, INC.

SIZE	DWG NO.	REV
D	00-878955	A

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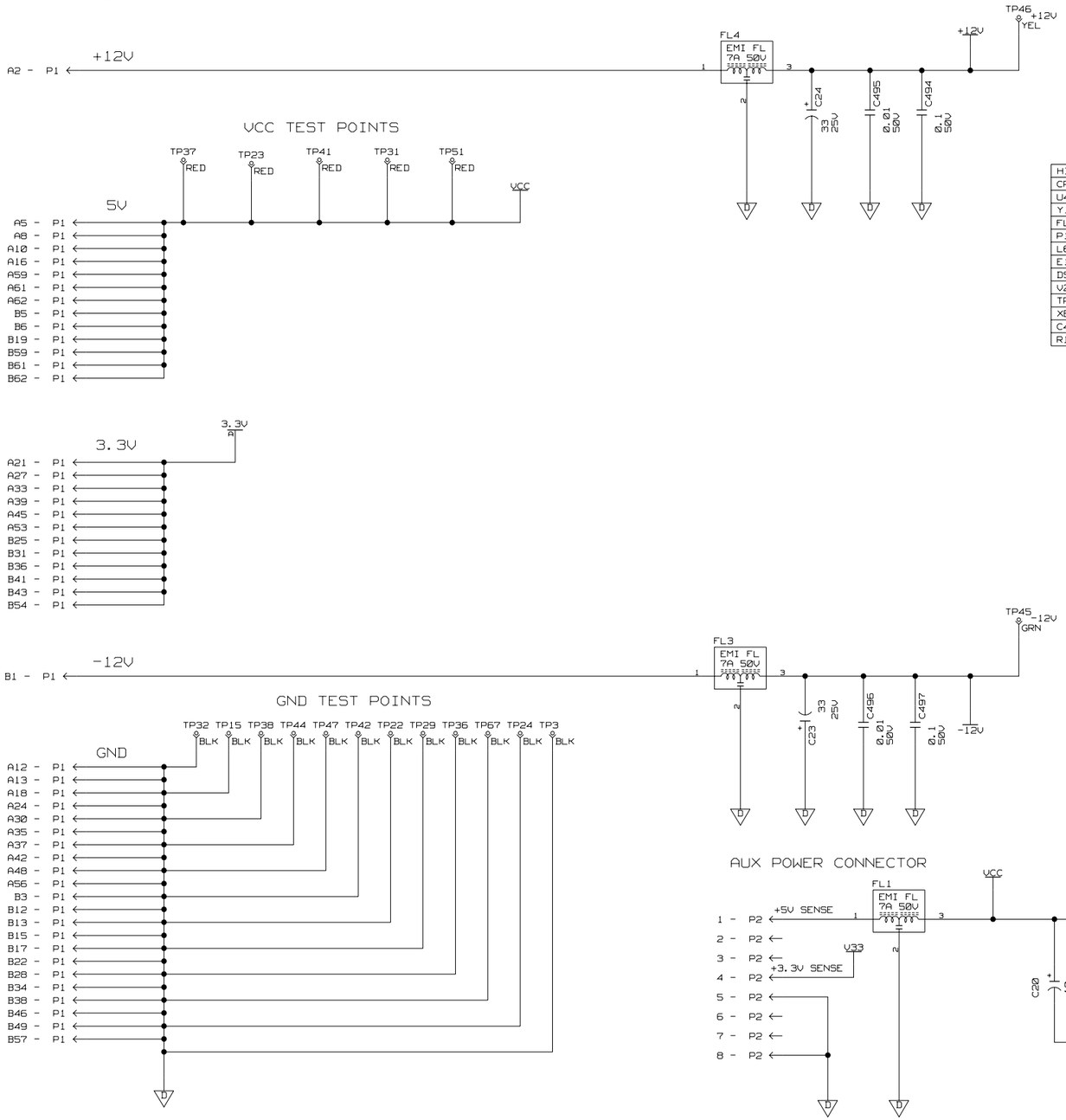
POWER ENTRY, BYPASS, AND FILTERING

PCI BUS CONNECTOR



REFERENCE DESIGNATIONS

HIGHEST	UNUSED
CR12	
U44	
Y1	
FL4	
P16	
L6	
E1	
DS2	
V2	
TP67	
XE2	
C499	
R173	

REF DES	DEVICE	GND	+5V	-5V	-12V	+12V	3.3V
U35	27C256	14	28				
U2,8,10	49FCT806	5,8,16	1,20				
U18	74ABT240	10	20				
U15,20	74FCT16224ST	4,10,15,	7,18,				
		21,28,	31,42				
		34,39,45					
U13	74FCT244	10	20				
U12,14,16,17	74FCT574	10	20				
U1	7805	2				1	
U11,25	78L05	2,3,6,7				8	
U3	7905	1			2		
U19,41	EPC1PC8	5	7,8				
U5,6,7	MAX499	2,4,9,	6,15,17	7,14,19			
		11,24					
U42	NM93CS46N	5	8				
U4,9	TVP3030	27,28,68,	29,30,				
		89,93,95,	67,90,				
		97,99,	153,174				
		108,109,					
		110,111,					
		154,172,					
		173					
U21,22,23,24,	VRAM	3,13,23,	1,8,18,				
27,28,29,30		33,42,	32,47,				
		52,62	57				
U43	PCI9050	9,26,40,	1,10,27,				
		51,65,	41,50,				
		80,104,	66,81,				
		120,147,	103,121,				
		160	146				
U26,31	74ABT3614	1,7,8,18,	11,29,				
		24,33,40,	36,51,				
		47,55,63,	59,75,				
		57,71,79,	83,98,				
		94,101,	105,123				
		110,116,					
		126					
U34	ST78C36	23,30	44				
U36,37	EPF81500AQC240	6,7,	18,40,				
	(+5V)	28,29,50,	60,62,				
		51,71,85,	91,114,				
		92,101,	129,151,				
		118,119,	173,209,				
		140,141,	236,17,				
		162,163,	39,61,78,				
		184,185,	94,108,				
		186,198,	130,152,				
		208,214,	174,191,				
		228	205,221,				
			235				
U33	LT1086	1	3				
U44	405506	11,34	14,31				
U32	BT121VCC	4,5,16, 17,27, 28,29, 30,31	32,33				
U38,39	SDRAM_1MX16	4,10,26, 41,47,50					1,7,13,25, 38,44
U40	EPF81500AQC240 (+3.3V)	6,7,28, 29,50, 51,71, 85,92, 101,118, 119,140, 141,152, 163,184, 185,186, 198,208, 214,228	18,40, 60,62, 91,114, 129,151, 173,209, 236				17,39,61,78, 94,108,130, 152,174,191, 205,221,235

DRAWING
LAST_MODIFIED=Thu May 21 12:30:39 1998

OEC MEDICAL SYSTEMS, INC.

SIZE	DWG NO.	REV
D	00-878955	A

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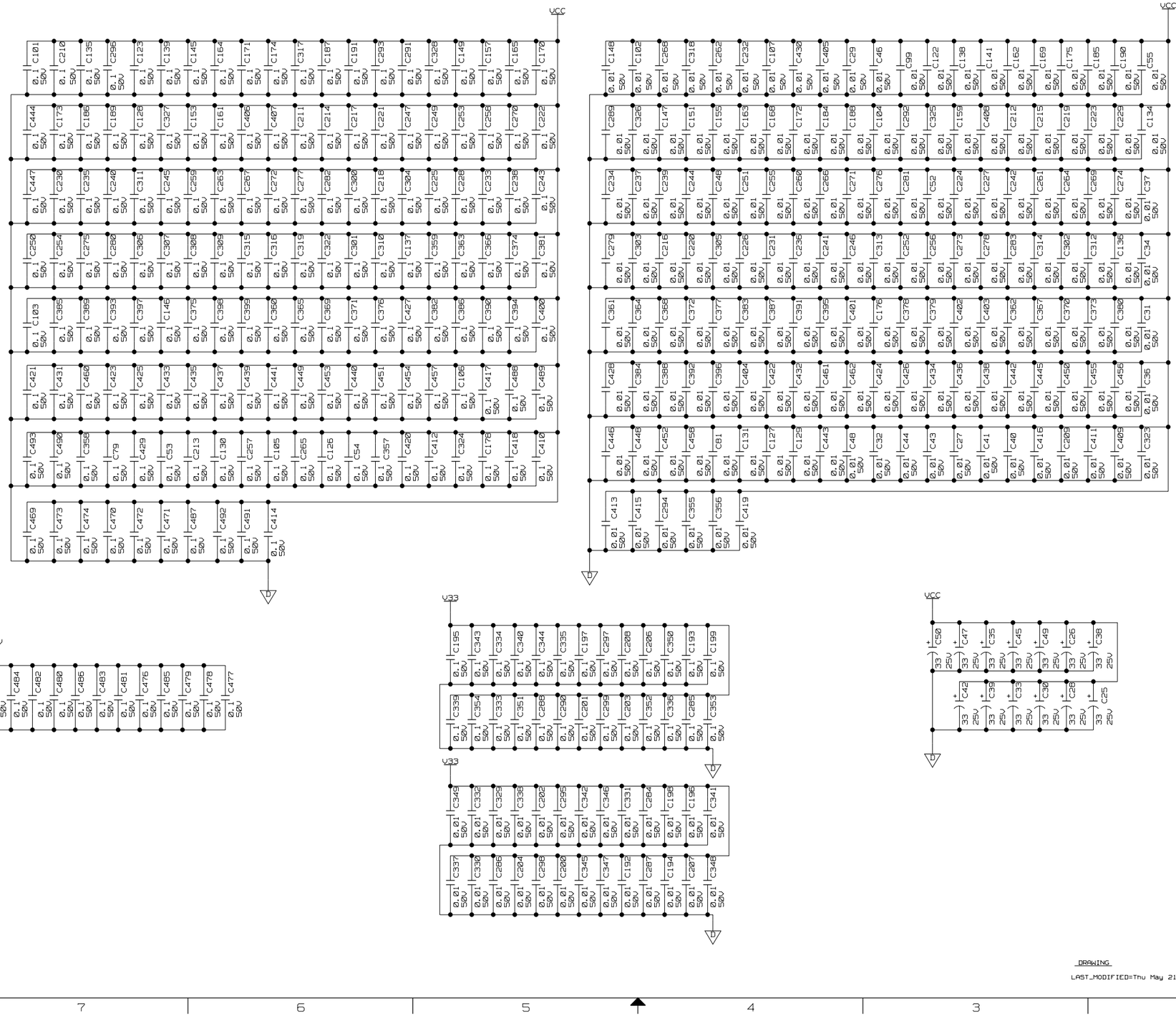

DRAWING

LAST_MODIFIED=Thu May 21 12:31:33 1998

OEC MEDICAL SYSTEMS, INC.		
SIZE D	DWG NO. 00-878955	REV A
SCALE:		SHEET 11 OF 22

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TV VIDEO CONTROL & OUTPUT

BIT BLASTER CONNECTOR

DCLK 1 - P16
GND 2 - P16
CONF_DONE 3 - P16
VCC 4 - P16
CONFIG* 5 - P16
BBVCC 6 - P16
STATUS* 7 - P16
BBGND 8 - P16
DATA0 9 - P16
GND 10 - P16

CONFIGURED FOR FLEX 8K PROGRAMMING

U19 EPC1 DCLK DATA OE CS CASC PACK_TYPE=DIP

R64 1K, R65 1K, R66 1K, R67 1K, R68 10K, R138 2K, R154 1K

TV_CONF_DCLK
TV_CONF_DONE
TV_CONFIG*
TV_CONF_STATUS*
TV_CONF_DATA0
TV_CONF_MSEL1

SEE SHEET 18 (TV VIDEO_CONTROL), U40

TV_VIDEO_CTRL
SPn, CONFIGn, MSEL0, MSEL1 (+3.3V)
DCLK, CONF_DONE, STATUSn, DATA0, SDOUT
CLK, RESETn, PLX_LWR_RDn, PLX_LWRn, PLX_CS1n, PLX_CS0n, PLX_LRDYn, CHIP_HIZn
RAM1_CKE, RAM1_CSn, RAM1_RASn, RAM1_CASn, RAM1_WEn, RAM1_DQM
PLX_LA<23..2>, PLX_LD<15..0>, IP_HSn, IP_VSn, IP_VID<7..0>, IP_AUX_PIX_SELn, RSTRn, RSTWn
RAM1_A<11..0>, RAM1_DQ<15..0>, DAC_CSn, DAC_CBn, DAC_VID<7..0>
TEST POINTS
field_index, ip_horz_active, ip_vert_active, read_1, read_2, sync_reset, tv_horz_active, tv_vert_active
RAM2_CKE, RAM2_CSn, RAM2_RASn, RAM2_CASn, RAM2_WEn, RAM2_DQM
DEL_VID<7..0>, IP_VID_OUT<7..0>
JTAG_TCLK, JTAG_TDI, JTAG_TDO, JTAG_TMS, JTAG_TRSTn
RAM2_A<11..0>, RAM2_DQ<15..0>

MUXED_CLK
PLX_LRESET*
PLX_LW_RD*
PLX_LWR*
PLX_CS1*
PLX_CS0*
PLX_LRDY*
PLX_LA<23..2>
PLX_LD<15..0>
HDRV_IN*
VDRV_IN*
AUX_PIX_DATA<7..0>
IP_AUX_PIX_SEL*

U44 485506 WCK RSTW WE MD RCK RSTR RE OE
DIN15..DIN0 DOUT15..DOUT0 PACK_TYPE=TSOPII

U38 SDRAM_1MX16 SPEED=12_NS
CLK CKE CS RAS CAS WE UDQM LDQM
A11 A10 A09 A08 A07 A06 A05 A04 A03 A02 A01 A00
DQ15..DQ00 PACK_TYPE=TSOPII

U39 SDRAM_1MX16 SPEED=12_NS
CLK CKE CS RAS CAS WE UDQM LDQM
A11 A10 A09 A08 A07 A06 A05 A04 A03 A02 A01 A00
DQ15..DQ00 PACK_TYPE=TSOPII

R155 475

JTAG_TCK
JTAG_CASCADE2
JTAG_TDO
JTAG_TMS
JTAG_TRST*

U32 BT121 PACK_TYPE=PLCC
VAA1 VAA0 GND7 GND6 GND5 GND4 GND3 GND2 GND1 GND0 GNDB
CLK SYNC BLANK VREF FS_ADJ COMP
R7 R6 R5 R4 R3 R2 R1 R0 G7 G6 G5 G4 G3 G2 G1 G0 B7 B6 B5 B4 B3 B2 B1 B0
IOR IOG IOB

C143 0.01, C144 0.1, C142 0.1, C140 0.01, C205 0.1, R140 15, R149 511, R116 1K

U6 MAX499
CS EN LE A0
IN3B IN3A IN2B IN2A IN1B IN1A GND OUT3 OUT2 OUT1
R15 475, R14 475
C8 0.01, C9 0.01, C110 0.01, C177 0.01

R13 0, R115 0, R121 0, R117 0

CR7 P12, CR8 P13, CR9 P14

R120 75, R11 75, R112 75, R119 75, R118 75, R12 75, R122 75

+5V, -5V

DRAWING
LAST_MODIFIED=Thu May 21 12:32:18 1998

OEC MEDICAL SYSTEMS, INC.
SIZE D | DWG NO. 00-878955 | REV A
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C/BE<3..0>*\I

U43

SPEED=33_MHZ

PCI9050_32BIT

PACK_TYPE=SQFP

160	GND	IDSEL\I	
159	IDSEL	C/BE<3>*\I	3
158	C/BE3n	AD<24>\I	24
157	AD24	AD<25>\I	25
156	AD25	AD<26>\I	26
155	AD26	AD<27>\I	27
154	AD27	AD<28>\I	28
153	AD28	AD<29>\I	29
152	AD29	AD<30>\I	30
151	AD30	AD<31>\I	31
150	AD31	CLK\I	
149	CLK	RST*\I	
148	RST		
147	GND		
146	VCC		
145	EEDI	EEDI\I	
144	EESK	EESK\I	
143	EEDO	EEDO\I	
142	EECS	EECS\I	
141	USER3/CS3n	CS3*\I	
140	USER2/CS2n	CS2*\I	
139	USER1/LOCKOn	LLOCK*\I	
138	USER0/WAITOn	WAITO*\I	
137	LINTI1	LINTI1\I	
136	LINTI2	LINT2\I	
135	LCLK	LCLK\I	
134	LHOLD	LHOLD\I	
133	LHOLDA	LHOLDA\I	
132	LRESET	LRESET\I	
131	CS1	CS1*\I	
130	CS0	CS0*\I	
129	BTERM	BTERM*\I	
128	LRDYI	LRDYI*\I	
127	LW/Rn	LW*\I	
126	RD	RD*\I	
125	WR	WR*\I	
124	BLAST	BLAST*\I	
123	ADS	ADS*\I	
122	LA27		
121	VCC		

1	VCC		
2	AD23	AD<23>\I	23
3	AD22	AD<22>\I	22
4	AD21	AD<21>\I	21
5	AD20	AD<20>\I	20
6	AD19	AD<19>\I	19
7	AD18	AD<18>\I	18
8	AD17	AD<17>\I	17
9	GND		
10	VCC		
11	AD16	AD<16>\I	16
12	C/BE2n	C/BE<2>*\I	2
13	FRAME	FRAME*\I	
14	IRDY	IRDY*\I	
15	TRDY	TRDY*\I	
16	DEVSEL	DEVSEL*\I	
17	STOP	STOP*\I	
18	LOCK	LOCK*\I	
19	PERR	PERR*\I	
20	SERR	SERR*\I	
21	PAR	PAR\I	
22	C/BE1n	C/BE<1>*\I	1
23	AD15	AD<15>\I	15
24	AD14	AD<14>\I	14
25	AD13	AD<13>\I	13
26	GND		
27	VCC		
28	AD12	AD<12>\I	12
29	AD11	AD<11>\I	11
30	AD10	AD<10>\I	10
31	AD9	AD<9>\I	9
32	AD8	AD<8>\I	8
33	C/BE0n	C/BE<0>*\I	0
34	AD7	AD<7>\I	7
35	AD6	AD<6>\I	6
36	AD5	AD<5>\I	5
37	AD4	AD<4>\I	4
38	AD3	AD<3>\I	3
39	AD2	AD<2>\I	2
40	GND		

41	VCC		
42	AD1	AD<1>\I	1
43	AD0	AD<0>\I	0
44	INTA	INTA*\I	
45	NO_CONNECT		
46	QLBE3	LBE<3>*\I	3
47	QLBE2	LBE<2>*\I	2
48	QLBE1	LBE<1>*\I	1
49	QLBE0	LBE<0>*\I	0
50	VCC		
51	GND		
52	LAD31	LAD<31>\I	31
53	LAD30	LAD<30>\I	30
54	LAD29	LAD<29>\I	29
55	LAD28	LAD<28>\I	28
56	LAD27	LAD<27>\I	27
57	LAD26	LAD<26>\I	26
58	LAD25	LAD<25>\I	25
59	LAD24	LAD<24>\I	24
60	LAD23	LAD<23>\I	23
61	LAD22	LAD<22>\I	22
62	LAD21	LAD<21>\I	21
63	BCLKO	BCLKO\I	
64	ALE	ALE\I	
65	GND		
66	VCC		
67	NO_CONNECT		
68	MODE	MODE\I	
69	LAD20	LAD<20>\I	20
70	LAD19	LAD<19>\I	19
71	LAD18	LAD<18>\I	18
72	LAD17	LAD<17>\I	17
73	LAD16	LAD<16>\I	16
74	LAD15	LAD<15>\I	15
75	LAD14	LAD<14>\I	14
76	LAD13	LAD<13>\I	13
77	LAD12	LAD<12>\I	12
78	LAD11	LAD<11>\I	11
79	LAD10	LAD<10>\I	10
80	GND		

120	GND	LA<27>\I	27
119	LA26	LA<26>\I	26
118	LA25	LA<25>\I	25
117	LA24	LA<24>\I	24
116	LA23	LA<23>\I	23
115	LA22	LA<22>\I	22
114	LA21	LA<21>\I	21
113	LA20	LA<20>\I	20
112	LA19	LA<19>\I	19
111	LA18	LA<18>\I	18
110	LA17	LA<17>\I	17
109	LA16	LA<16>\I	16
108	LA15	LA<15>\I	15
107	LA14	LA<14>\I	14
106	LA13	LA<13>\I	13
105	LA12	LA<12>\I	12
104	GND		
103	VCC		
102	LA11	LA<11>\I	11
101	LA10	LA<10>\I	10
100	LA9	LA<9>\I	9
99	TEST	TEST\I	
98	LA8	LA<8>\I	8
97	LA7	LA<7>\I	7
96	LA6	LA<6>\I	6
95	LA5	LA<5>\I	5
94	LA4	LA<4>\I	4
93	LA3	LA<3>\I	3
92	LA2	LA<2>\I	2
91	LAD0	LAD<0>\I	0
90	LAD1	LAD<1>\I	1
89	LAD2	LAD<2>\I	2
88	LAD3	LAD<3>\I	3
87	LAD4	LAD<4>\I	4
86	LAD5	LAD<5>\I	5
85	LAD6	LAD<6>\I	6
84	LAD7	LAD<7>\I	7
83	LAD8	LAD<8>\I	8
82	LAD9	LAD<9>\I	9
81	VCC		

LA<27..2>\I

LAD<31..0>\I

AD<31..0>\I

LBE<3..0>*\I

PLX9050

DRAWING

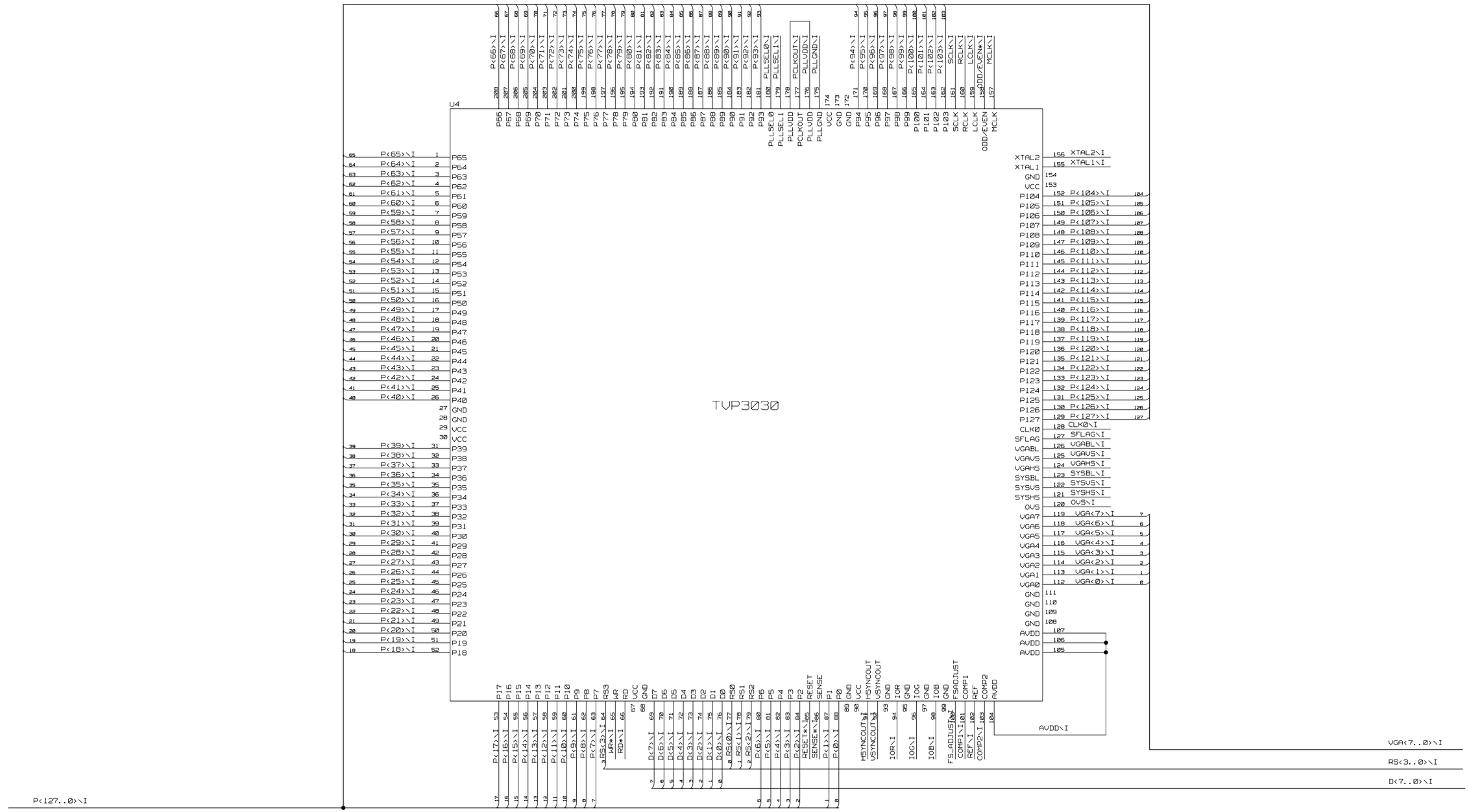
LAST_MODIFIED=Thu May 21 12:43:02 1998

OEC MEDICAL SYSTEMS, INC.

SIZE	DWG NO.	REV
D	00-878955	A

SCALE: | SHEET 13 OF 22

05-017-9/93

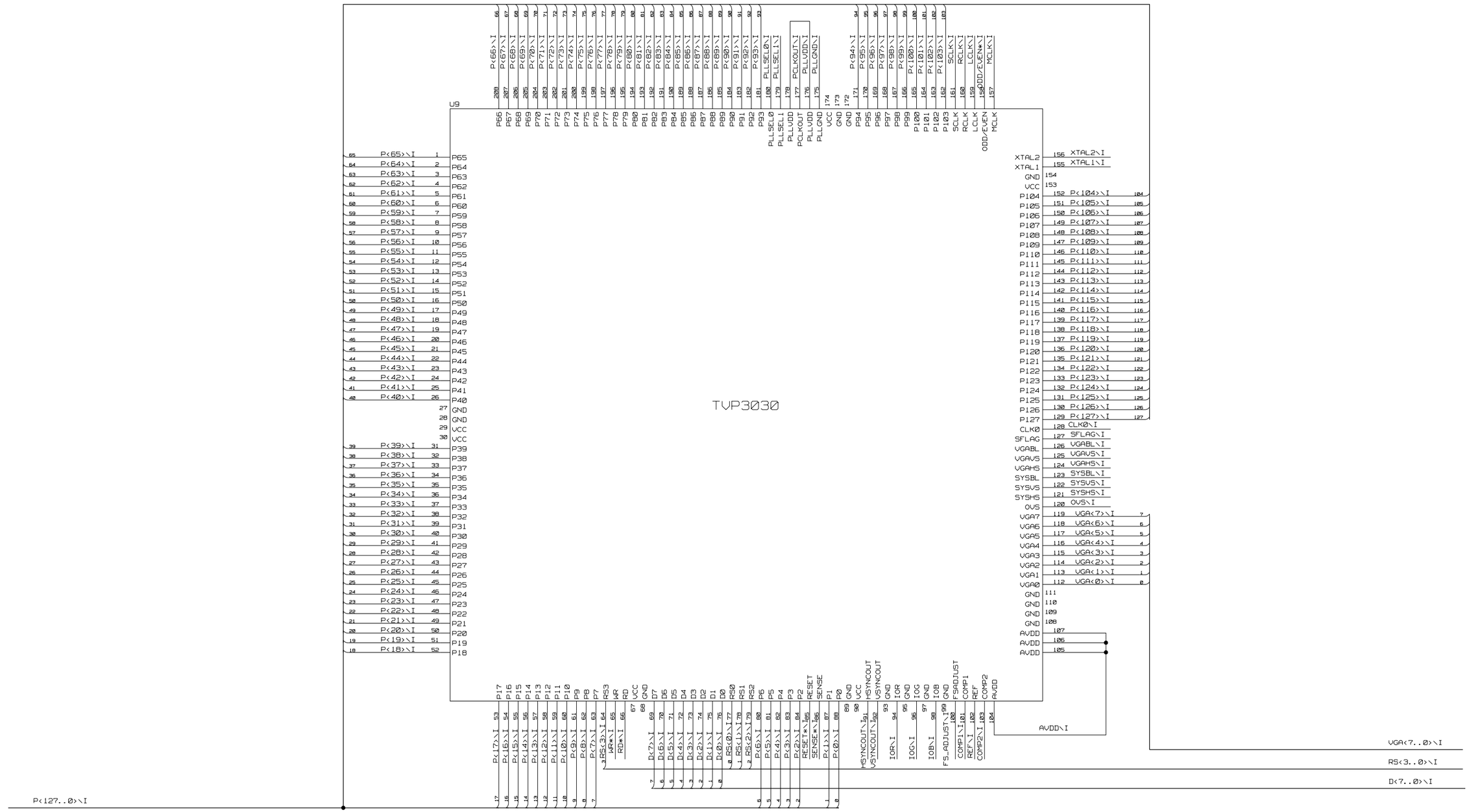


DRAWING

LAST_MODIFIED=Thu May 21 12:43:46 1998

OEC MEDICAL SYSTEMS, INC.		
SIZE D	DWG NO. 00-878955	REV A
SCALE:		SHEET 14 OF 22

05-017-9/93



RAMDAC4

DRAWING

LAST_MODIFIED=Thu May 21 12:44:30 1998

OEC MEDICAL SYSTEMS, INC.

SIZE	DWG NO.	REV
D	00-878955	A

SCALE: | SHEET 15 OF 22

05-017-9/93

PLX_LA<23..2>\I
23 PLX_LA<23>\I
22 PLX_LA<22>\I
21 PLX_LA<21>\I
20 PLX_LA<20>\I
19 PLX_LA<19>\I
18 PLX_LA<18>\I
17 PLX_LA<17>\I
16 PLX_LA<16>\I
15 PLX_LA<15>\I
14 PLX_LA<14>\I
13 PLX_LA<13>\I
12 PLX_LA<12>\I
11 PLX_LA<11>\I
10 PLX_LA<10>\I
9 PLX_LA<9>\I
8 PLX_LA<8>\I
7 PLX_LA<7>\I
6 PLX_LA<6>\I
5 PLX_LA<5>\I
4 PLX_LA<4>\I
3 PLX_LA<3>\I
2 PLX_LA<2>\I

PLX_LD<15..0>\I
15 PLX_LD<15>\I
14 PLX_LD<14>\I
13 PLX_LD<13>\I
12 PLX_LD<12>\I
11 PLX_LD<11>\I
10 PLX_LD<10>\I
9 PLX_LD<9>\I
8 PLX_LD<8>\I
7 PLX_LD<7>\I
6 PLX_LD<6>\I
5 PLX_LD<5>\I
4 PLX_LD<4>\I
3 PLX_LD<3>\I
2 PLX_LD<2>\I
1 PLX_LD<1>\I
0 PLX_LD<0>\I

SVR_WEN<4..1>\I
4 SVR_WEN<4>\I
3 SVR_WEN<3>\I
2 SVR_WEN<2>\I
1 SVR_WEN<1>\I

MVR_A<8..0>\I
8 MVR_A<8>\I
7 MVR_A<7>\I
6 MVR_A<6>\I
5 MVR_A<5>\I
4 MVR_A<4>\I
3 MVR_A<3>\I
2 MVR_A<2>\I
1 MVR_A<1>\I
0 MVR_A<0>\I

MVR_WEN<4..1>\I
4 MVR_WEN<4>\I
3 MVR_WEN<3>\I
2 MVR_WEN<2>\I
1 MVR_WEN<1>\I

SVR_A<8..0>\I
8 SVR_A<8>\I
7 SVR_A<7>\I
6 SVR_A<6>\I
5 SVR_A<5>\I
4 SVR_A<4>\I
3 SVR_A<3>\I
2 SVR_A<2>\I
1 SVR_A<1>\I
0 SVR_A<0>\I

TP61 L_TPA WHT
TP62 L_TPB WHT
TP63 L_TPC WHT

U36

EPF81500AQC240

SPEED=A_4

NOTE:

THIS COMPONENT BODY DRAWING IS NOT INTENDED FOR PRODUCTION SCHEMATIC USE.

PACK_TYPE=SQFP

SVR_CASn\I	1	P1	
SVR_A<0>\I	2	P2	
MVR_CASn\I	3	P3	
PLX_LD<2>\I	4	P4	
SVR_WEN<1>\I	5	P5	
	6	GND	
	7	GND	
LEFT_RIGHTn\I	8	P8	
SVR_WEN<2>\I	9	P9	
SVR_RASn\I	10	P10	
SVR_WEN<4>\I	11	P11	
SVR_WEN<3>\I	12	P12	
MVR_A<3>\I	13	P13	
MVR_A<2>\I	14	P14	
MVR_A<1>\I	15	P15	
MVR_A<0>\I	16	P16	
	17	VCCIO	
	18	VCC	
MSEL0\I	19	MSEL0	
MVR_A<5>\I	20	P20	
MVR_A<4>\I	21	P21	
MVR_A<6>\I	22	P22	
MVR_A<7>\I	23	P23	
PLX_LA<15>\I	24	P24	
PLX_LA<16>\I	25	P25	
PLX_LA<17>\I	26	P26	
PLX_LA<18>\I	27	P27	
	28	GND	
	29	GND	
PLX_LA<19>\I	30	P30	
PLX_LA<20>\I	31	P31	
PLX_LA<21>\I	32	P32	
PLX_LA<22>\I	33	P33	
PLX_LWRn\I	34	P34	
PLX_LRDn\I	35	P35	
PLX_LA<23>\I	36	P36	
PLX_LRESETn\I	37	P37	
MSEL1\I	38	MSEL1	
	39	VCCIO	
	40	VCC	
PLX_LCLK\I	41	P41	
PLX_LW_RDn\I	42	P42	
PLX_CS0n\I	43	P43	
PLX_CS1n\I	44	P44	
PLX_LD<4>\I	45	P45	
PLX_LD<5>\I	46	P46	
PLX_LD<6>\I	47	P47	
PLX_LD<7>\I	48	P48	
MUXED_CLK\I	49	P49	
	50	GND	
	51	GND	
PLX_LD<8>\I	52	P52	
PLX_LD<9>\I	53	P53	
PLX_LD<10>\I	54	P54	
PLX_LD<11>\I	55	P55	
PLX_LD<12>\I	56	P56	
PLX_LD<13>\I	57	P57	
PLX_LD<14>\I	58	P58	
PLX_LD<15>\I	59	P59	
	60	VCC	

	61	VCCIO	
	62	VCC	
JTAG_TDI\I	63	TDI	
JTAG_TMS\I	64	TMS	
PLX_BTERMn\I	65	P65	
PLX_LRDYn\I	66	P66	
PLX_ADSn\I	67	P67	
PLX_BLASTn\I	68	P68	
PLX_WAIT0n\I	69	P69	
PLX_ALE\I	70	P70	
	71	GND	
	72	P72	
	73	P73	
VGA_XOUT\I	74	P74	
PLX_LINT2n\I	75	P75	
EXP_ROM_CSn\I	76	P76	
EXP_ROM_OEn\I	77	P77	
	78	VCCIO	
PLX_LD<1>\I	79	P79	
PLX_LD<0>\I	80	P80	
	81	P81	
PLX_LINT1n\I	82	P82	
PCB_CFG_RDn\I	83	P83	
	84	P84	
	85	GND	
PLX_LA<6>\I	86	P86	
PLX_LA<4>\I	87	P87	
PLX_LA<3>\I	88	P88	
PLX_LD<3>\I	89	P89	
PLX_LA<5>\I	90	P90	
	91	VCC	
	92	GND	
	93	P93	
	94	VCCIO	
	95	P95	
VGA_XIN1\I	96	P96	
	97	P97	
	98	P98	
	99	P99	
	100	P100	
	101	GND	
	102	P102	
VGA_XIN2\I	103	P103	
	104	P104	
	105	P105	
	106	P106	
	107	P107	
	108	VCCIO	
L_TPA	109	P109	
L_TPB	110	P110	
L_TPC	111	P111	
EPP_IRQn\I	112	P112	
	113	P113	
	114	VCC	
JTAG_TRSTn\I	115	nTRST	
JTAG_TCLK\I	116	TCLK	
JTAG_TDO\I	117	TDO	
	118	GND	
CONFIG\I	119	GND	
	120	nCONFIG	

	240	P240	
	239	P239	
	238	P238	
	237	nSP	
	236	VCC	
	235	VCCIO	
	234	P234	
	233	P233	
	232	P232	
	231	P231	
	230	P230	
	229	P229	
	228	GND	
	227	P227	
	226	P226	
	225	P225	
	224	P224	
	223	P223	
	222	P222	
	221	VCCIO	
	220	P220	
	219	P219	
	218	P218	
	217	P217	
	216	P216	
	215	P215	
	214	GND	
	213	P213	
	212	P212	
	211	P211	
	210	P210	
	209	VCC	
	208	GND	
	207	P207	
	206	P206	
	205	VCCIO	
	204	P204	
	203	P203	
	202	P202	
	201	P201	
	200	P200	
	199	P199	
	198	GND	
	197	P197	
	196	P196	
	195	P195	
	194	P194	
	193	P193	
	192	P192	
	191	VCCIO	
	190	P190	
	189	P189	
	188	P188	
	187	P187	
	186	GND	
	185	GND	
	184	GND	
	183	DCLK	
	182	P182	
	181	P181	

	180	P180	FIFO_FFAn\I
	179	P179	
	178	P178	
	177	P177	
	176	P176	FIFO_AEBn\I
	175	P175	
	174	VCCIO	
	173	VCC	
DAC_RCLK\I	172	P172	
PLX_PIX_SELn\I	171	P171	
IP_PIX_SELn\I	170	P170	
PLX_LA<10>\I	169	P169	
PLX_LA<9>\I	168	P168	
PLX_LA<11>\I	167	P167	
PLX_LA<12>\I	166	P166	
PLX_LA<13>\I	165	P165	
PLX_LA<14>\I	164	P164	
	163	GND	
	162	GND	
CONF_DONE\I	161	CONF_DONE	
MVR_WEN<2>\I	160	P160	
MVR_WEN<3>\I	159	P159	
MVR_WEN<4>\I	158	P158	
	157	P157	
PIXWE_INn\I	156	P156	
PIX_WEn\I	155	P155	
PLX_LA<2>\I	154	P154	
MVR_WEN<1>\I	153	P153	
	152	VCCIO	
	151	VCC	
EPP_IOCHRDYn\I	150	P150	
PLX_CS2n\I	149	P149	
SVR_SCLK\I	148	P148	
SVR_SCLK_ENn\I	147	P147	
SVR_DTOEn\I	146	P146	
SVR_DSF\I	145	P145	
SVR_QSF\I	144	P144	
EPP_PLX_LRDYn\I	143	P143	
STATUSn\I	142	nSTATUS	
	141	GND	
	140	GND	
SVR_A<2>\I	139	P139	
SVR_A<3>\I	138	P138	
SVR_A<1>\I	137	P137	
SDOUT\I	136	P136	
SVR_A<7>\I	135	P135	
SVR_A<6>\I	134	P134	
SVR_A<8>\I	133	P133	
SVR_A<4>\I	132	P132	
FIFO_AEAn\I	131	P131	
	130	VCCIO	
	129	VCC	
SVR_A<5>\I	128	P128	
VGA_SEL\I	127	P127	
	126	P126	
IP_CLK_SELn\I	125	P125	
PLX_BCLKO_SELn\I	124	P124	
DAC_RESETn\I	123	P123	
	122	P122	
	121	P121	

	240	P240	
	239	P239	
	238	P238	
	237	nSP	
	236	VCC	
	235	VCCIO	
	234	P234	
	233	P233	
	232	P232	
	231	P231	
	230	P230	
	229	P229	
	228	GND	
	227	P227	
	226	P226	
	225	P225	
	224	P224	
	223	P223	
	222	P222	
	221	VCCIO	
	220	P220	
	219	P219	
	218	P218	
	217	P217	
	216	P216	
	215	P215	
	214	GND	
	213	P213	
	212	P212	
	211	P211	
	210	P210	
	209	VCC	
	208	GND	
	207	P207	
	206	P206	
	205	VCCIO	
	204	P204	
	203	P203	
	202	P202	
	201	P201	
	200	P200	
	199	P199	
	198	GND	
	197	P197	
	196	P196	
	195	P195	
	194	P194	
	193	P193	
	192	P192	
	191	VCCIO	
	190	P190	
	189	P189	
	188	P188	
	187	P187	
	186	GND	
	185	GND	
	184	GND	
	183	DCLK	
	182	P182	
	181	P181	

MVR_RASn\I
SPn\I
UNBLANKn_LED\I
IP_ACTIVEn_LED\I
L_DAC_RDn\I
L_DAC_WRn\I
DAC_LCLK\I
DAC_VSYNCn\I
DAC_HSYNCn\I
DAC_BLANKn\I
MVR_SCLK\I
MVR_A<8>\I
MVR_DSF\I
MVR_DTOEn\I
MVR_SCLK_ENn\I
FIFO_EFBn\I
FIFO_EFAn\I
FIFO_A_M_RDn\I
FIFO_CSAn\I
FIFO_AFBn\I
FIFO_CSBn\I
FIFO_FFBn\I
FIFO_ENBn\I
FIFO_B_W_RDn\I
FIFO_SIZE0\I
FIFO_SIZE1\I
FIFO_RSTn\I
FIFO_MBA\I
FIFO_ENA\I
FIFO_AFA\I
PLX_PIXDATA_RDn\I
MDRVn\I
VDRVn\I
DATA0\I
DCLK\I
PLX_LA<7>\I
PLX_LA<8>\I

LEFT VIDEO CONTROL

DRAWING

LAST_MODIFIED=Thu May 21 12:42:16 1998

PLX_LA<23..2>\I
- 23 PLX_LA<23>\I
- 22 PLX_LA<22>\I
- 21 PLX_LA<21>\I
- 20 PLX_LA<20>\I
- 19 PLX_LA<19>\I
- 18 PLX_LA<18>\I
- 17 PLX_LA<17>\I
- 16 PLX_LA<16>\I
- 15 PLX_LA<15>\I
- 14 PLX_LA<14>\I
- 13 PLX_LA<13>\I
- 12 PLX_LA<12>\I
- 11 PLX_LA<11>\I
- 10 PLX_LA<10>\I
- 9 PLX_LA<9>\I
- 8 PLX_LA<8>\I
- 7 PLX_LA<7>\I
- 6 PLX_LA<6>\I
- 5 PLX_LA<5>\I
- 4 PLX_LA<4>\I
- 3 PLX_LA<3>\I
- 2 PLX_LA<2>\I

PLX_LD<15..0>\I
- 15 PLX_LD<15>\I
- 14 PLX_LD<14>\I
- 13 PLX_LD<13>\I
- 12 PLX_LD<12>\I
- 11 PLX_LD<11>\I
- 10 PLX_LD<10>\I
- 9 PLX_LD<9>\I
- 8 PLX_LD<8>\I
- 7 PLX_LD<7>\I
- 6 PLX_LD<6>\I
- 5 PLX_LD<5>\I
- 4 PLX_LD<4>\I
- 3 PLX_LD<3>\I
- 2 PLX_LD<2>\I
- 1 PLX_LD<1>\I
- 0 PLX_LD<0>\I

SVR_WEN<4..1>\I
- 4 SVR_WEN<4>\I
- 3 SVR_WEN<3>\I
- 2 SVR_WEN<2>\I
- 1 SVR_WEN<1>\I

MVR_A<8..0>\I
- 8 MVR_A<8>\I
- 7 MVR_A<7>\I
- 6 MVR_A<6>\I
- 5 MVR_A<5>\I
- 4 MVR_A<4>\I
- 3 MVR_A<3>\I
- 2 MVR_A<2>\I
- 1 MVR_A<1>\I
- 0 MVR_A<0>\I

MVR_WEN<4..1>\I
- 4 MVR_WEN<4>\I
- 3 MVR_WEN<3>\I
- 2 MVR_WEN<2>\I
- 1 MVR_WEN<1>\I

SVR_A<8..0>\I
- 8 SVR_A<8>\I
- 7 SVR_A<7>\I
- 6 SVR_A<6>\I
- 5 SVR_A<5>\I
- 4 SVR_A<4>\I
- 3 SVR_A<3>\I
- 2 SVR_A<2>\I
- 1 SVR_A<1>\I
- 0 SVR_A<0>\I

TP64 R_TPA WHT
TP65 R_TPB WHT
TP66 R_TPC WHT

U37

EPF81500AQC240

SPEED=A_4

NOTE:

THIS COMPONENT BODY DRAWING IS NOT INTENDED FOR PRODUCTION SCHEMATIC USE.

PACK_TYPE=SQFP

		P240	R_DAC_RDn\I
		P239	R_DAC_WRn\I
		P238	MVR_RASn\I
		nSP	SPn\I
		VCC	
		VCCIO	UNBLANKn_LED\I
		P234	
		P233	IP_ACTIVEn_LED\I
		P232	
		P231	
		P230	
		P229	
		GND	
		P227	
		P226	DAC_LCLK\I
		P225	DAC_VSYNCn\I
		P224	DAC_HSYNCn\I
		P223	DAC_BLANKn\I
		P222	
		VCCIO	
		P220	MVR_SCLK\I
		P219	
		P218	MVR_A<8>\I
		P217	MVR_DSF\I
		P216	MVR_DTOEn\I
		P215	MVR_SCLK_ENn\I
		GND	
		P213	FIFO_EFBn\I
		P212	FIFO_EFAn\I
		P211	FIFO_A_W_RDn\I
		P210	FIFO_CSAn\I
		VCC	
		GND	
		P207	FIFO_AFBn\I
		P206	FIFO_CSBn\I
		P205	
		VCCIO	
		P204	FIFO_FFBn\I
		P203	FIFO_ENBn\I
		P202	
		P201	FIFO_B_W_RDn\I
		P200	FIFO_SIZE0\I
		P199	FIFO_SIZE1\I
		GND	
		P197	FIFO_RSTn\I
		P196	FIFO_MBA\I
		P195	FIFO_ENA\I
		P194	FIFO_AFA\I
		P193	PLX_PIXDATA_RDn\I
		P192	MRVn\I
		VCCIO	
		P190	VIRVn\I
		P189	
		P188	DATA0\I
		P187	
		GND	
		GND	
		GND	
		DCLK	DCLK\I
		P182	PLX_LA<7>\I
		P181	PLX_LA<6>\I

SVR_CASn\I	1	P1	
SVR_A<0>\I	2	P2	
MVR_CASn\I	3	P3	
PLX_LD<2>\I	4	P4	
SVR_WEN<1>\I	5	P5	
	6	GND	
	7	GND	
LEFT_RIGHTn\I	8	P8	
SVR_WEN<2>\I	9	P9	
SVR_RASn\I	10	P10	
SVR_WEN<4>\I	11	P11	
SVR_WEN<3>\I	12	P12	
MVR_A<3>\I	13	P13	
MVR_A<2>\I	14	P14	
MVR_A<1>\I	15	P15	
MVR_A<0>\I	16	P16	
	17	VCCIO	
	18	VCC	
MSEL0\I	19	MSEL0	
MVR_A<5>\I	20	P20	
MVR_A<4>\I	21	P21	
MVR_A<6>\I	22	P22	
MVR_A<7>\I	23	P23	
PLX_LA<15>\I	24	P24	
PLX_LA<16>\I	25	P25	
PLX_LA<17>\I	26	P26	
PLX_LA<18>\I	27	P27	
	28	GND	
	29	GND	
PLX_LA<19>\I	30	P30	
PLX_LA<20>\I	31	P31	
PLX_LA<21>\I	32	P32	
PLX_LA<22>\I	33	P33	
PLX_LWRn\I	34	P34	
PLX_LRDn\I	35	P35	
PLX_LA<23>\I	36	P36	
PLX_LRESETn\I	37	P37	
MSEL1\I	38	MSEL1	
	39	VCCIO	
	40	VCC	
PLX_LCLK\I	41	P41	
PLX_LW_RDn\I	42	P42	
PLX_CS0n\I	43	P43	
PLX_CS1n\I	44	P44	
PLX_LD<4>\I	45	P45	
PLX_LD<5>\I	46	P46	
PLX_LD<6>\I	47	P47	
PLX_LD<7>\I	48	P48	
MUXED_CLK\I	49	P49	
	50	GND	
	51	GND	
PLX_LD<8>\I	52	P52	
PLX_LD<9>\I	53	P53	
PLX_LD<10>\I	54	P54	
PLX_LD<11>\I	55	P55	
PLX_LD<12>\I	56	P56	
PLX_LD<13>\I	57	P57	
PLX_LD<14>\I	58	P58	
PLX_LD<15>\I	59	P59	
	60	VCC	

		P180	180 FIFO_FFAn\I
		P179	179
		P178	178
		P177	177
		P176	176 FIFO_AEBn\I
		P175	175
		VCCIO	174
		VCC	173
		P172	172 DAC_RCLK\I
		P171	171 PLX_PIX_SELn\I
		P170	170 IP_PIX_SELn\I
		P169	169 PLX_LA<10>\I
		P168	168 PLX_LA<9>\I
		P167	167 PLX_LA<11>\I
		P166	166 PLX_LA<12>\I
		P165	165 PLX_LA<13>\I
		P164	164 PLX_LA<14>\I
		GND	163
		GND	162
		CONF_DONE	161 CONF_DONE\I
		P160	160 MVR_WEN<2>\I
		P159	159 MVR_WEN<3>\I
		P158	158 MVR_WEN<4>\I
		P157	157
		P156	156 PIXWE_INn\I
		P155	155 PIX_WEn\I
		P154	154 PLX_LA<2>\I
		P153	153 MVR_WEN<1>\I
		VCCIO	152
		VCC	151
		P150	150 EPP_IOCHRDYn\I
		P149	149 PLX_CS2n\I
		P148	148 SVR_SCLK\I
		P147	147 SVR_SCLK_ENn\I
		P146	146 SVR_DTOEn\I
		P145	145 SVR_DSF\I
		P144	144 SVR_QSF\I
		P143	143 EPP_PLX_LRDYn\I
		nSTATUS	142 STATUSn\I
		GND	141
		GND	140
		P139	139 SVR_A<2>\I
		P138	138 SVR_A<3>\I
		P137	137 SVR_A<1>\I
		P136	136 SDOUT\I
		P135	135 SVR_A<7>\I
		P134	134 SVR_A<6>\I
		P133	133 SVR_A<8>\I
		P132	132 SVR_A<4>\I
		P131	131 FIFO_AEAn\I
		VCCIO	130
		VCC	129
		P128	128 SVR_A<5>\I
		P127	127 VGA_SEL\I
		P126	126
		P125	125 IP_CLK_SELn\I
		P124	124 PLX_BCLKO_SELn\I
		P123	123 DAC_RESETn\I
		P122	122
		P121	121

		VCCIO	61
		VCC	62
JTAG_TDI\I		TDI	63
JTAG_TMS\I		TMS	64
PLX_BTERMn\I		P65	65
PLX_LRDYn\I		P66	66
PLX_ADSn\I		P67	67
PLX_BLASTn\I		P68	68
PLX_WAITOn\I		P69	69
PLX_ALE\I		P70	70
		GND	71
		P72	72
		P73	73
VGA_XOUT\I		P74	74
PLX_LINT2n\I		P75	75
EXP_ROM_CSn\I		P76	76
EXP_ROM_OEn\I		P77	77
		VCCIO	78
PLX_LD<1>\I		P79	79
PLX_LD<0>\I		P80	80
		P81	81
PLX_LINT1n\I		P82	82
PCB_CFG_RDn\I		P83	83
		P84	84
		GND	85
		P86	86
PLX_LA<6>\I		P87	87
PLX_LA<4>\I		P88	88
PLX_LA<3>\I		P89	89
PLX_LD<3>\I		P90	90
PLX_LA<5>\I		VCC	91
		GND	92
		P93	93
		VCCIO	94
VGA_XIN1\I		P95	95
		P96	96
		P97	97
		P98	98
		P99	99
		P100	100
		GND	101
		P102	102
VGA_XIN2\I		P103	103
		P104	104
		P105	105
		P106	106
		P107	107
		VCCIO	108
R_TPA		P109	109
R_TPB		P110	110
R_TPC		P111	111
EPP_IRQn\I		P112	112
		P113	113
		VCC	114
JTAG_TRSTn\I		nTRST	115
JTAG_TCLK\I		TCLK	116
JTAG_TDO\I		TDO	117
		GND	118
CONFIG\I		GND	119
		nCONFIG	120

RIGHT VIDEO CONTROL

DRAWING

LAST_MODIFIED=Thu May 21 12:45:13 1998

OEC MEDICAL SYSTEMS, INC.

SIZE	DWG NO.	REV
D	00-878955	A

SCALE: | SHEET 17 OF 22

05-017-9/93

PLX_LA<23..2>\I

23 PLX_LA<23>\I
22 PLX_LA<22>\I
21 PLX_LA<21>\I
20 PLX_LA<20>\I
19 PLX_LA<19>\I
18 PLX_LA<18>\I
17 PLX_LA<17>\I
16 PLX_LA<16>\I
15 PLX_LA<15>\I
14 PLX_LA<14>\I
13 PLX_LA<13>\I
12 PLX_LA<12>\I
11 PLX_LA<11>\I
10 PLX_LA<10>\I
9 PLX_LA<9>\I
8 PLX_LA<8>\I
7 PLX_LA<7>\I
6 PLX_LA<6>\I
5 PLX_LA<5>\I
4 PLX_LA<4>\I
3 PLX_LA<3>\I
2 PLX_LA<2>\I

IP_VID<7..0>\I

7 IP_VID<7>\I
6 IP_VID<6>\I
5 IP_VID<5>\I
4 IP_VID<4>\I
3 IP_VID<3>\I
2 IP_VID<2>\I
1 IP_VID<1>\I
0 IP_VID<0>\I

IP_VID_OUT<7..0>\I

7 IP_VID_OUT<7>\I
6 IP_VID_OUT<6>\I
5 IP_VID_OUT<5>\I
4 IP_VID_OUT<4>\I
3 IP_VID_OUT<3>\I
2 IP_VID_OUT<2>\I
1 IP_VID_OUT<1>\I
0 IP_VID_OUT<0>\I

PLX_LD<15..0>\I

15 PLX_LD<15>\I
14 PLX_LD<14>\I
13 PLX_LD<13>\I
12 PLX_LD<12>\I
11 PLX_LD<11>\I
10 PLX_LD<10>\I
9 PLX_LD<9>\I
8 PLX_LD<8>\I
7 PLX_LD<7>\I
6 PLX_LD<6>\I
5 PLX_LD<5>\I
4 PLX_LD<4>\I
3 PLX_LD<3>\I
2 PLX_LD<2>\I
1 PLX_LD<1>\I
0 PLX_LD<0>\I

DAC_VID<7..0>\I

7 DAC_VID<7>\I
6 DAC_VID<6>\I
5 DAC_VID<5>\I
4 DAC_VID<4>\I
3 DAC_VID<3>\I
2 DAC_VID<2>\I
1 DAC_VID<1>\I
0 DAC_VID<0>\I

DEL_VID<7..0>\I

7 DEL_VID<7>\I
6 DEL_VID<6>\I
5 DEL_VID<5>\I
4 DEL_VID<4>\I
3 DEL_VID<3>\I
2 DEL_VID<2>\I
1 DEL_VID<1>\I
0 DEL_VID<0>\I

RAM1_DQ<15..0>\I

15 RAM1_DQ<15>\I
14 RAM1_DQ<14>\I
13 RAM1_DQ<13>\I
12 RAM1_DQ<12>\I
11 RAM1_DQ<11>\I
10 RAM1_DQ<10>\I
9 RAM1_DQ<9>\I
8 RAM1_DQ<8>\I
7 RAM1_DQ<7>\I
6 RAM1_DQ<6>\I
5 RAM1_DQ<5>\I
4 RAM1_DQ<4>\I
3 RAM1_DQ<3>\I
2 RAM1_DQ<2>\I
1 RAM1_DQ<1>\I
0 RAM1_DQ<0>\I

RAM1_A<9..0>\I

9 RAM1_A<9>\I
8 RAM1_A<8>\I
7 RAM1_A<7>\I
6 RAM1_A<6>\I
5 RAM1_A<5>\I
4 RAM1_A<4>\I
3 RAM1_A<3>\I
2 RAM1_A<2>\I
1 RAM1_A<1>\I
0 RAM1_A<0>\I

RAM2_DQ<15..0>\I

15 RAM2_DQ<15>\I
14 RAM2_DQ<14>\I
13 RAM2_DQ<13>\I
12 RAM2_DQ<12>\I
11 RAM2_DQ<11>\I
10 RAM2_DQ<10>\I
9 RAM2_DQ<9>\I
8 RAM2_DQ<8>\I
7 RAM2_DQ<7>\I
6 RAM2_DQ<6>\I
5 RAM2_DQ<5>\I
4 RAM2_DQ<4>\I
3 RAM2_DQ<3>\I
2 RAM2_DQ<2>\I
1 RAM2_DQ<1>\I
0 RAM2_DQ<0>\I

RAM2_A<9..0>\I

9 RAM2_A<9>\I
8 RAM2_A<8>\I
7 RAM2_A<7>\I
6 RAM2_A<6>\I
5 RAM2_A<5>\I
4 RAM2_A<4>\I
3 RAM2_A<3>\I
2 RAM2_A<2>\I
1 RAM2_A<1>\I
0 RAM2_A<0>\I

U40

RAM1_A<4>\I 240 P240
DAC_VID<5>\I 239 P239
DAC_VID<1>\I 238 P238
SPI\I 237 nSP
236 VCC
235 VCCIO
RAM1_CASn\I 234 P234
RAM1_A<6>\I 233 P233
DAC_VID<7>\I 232 P232
IP_VID<6>\I 231 P231
RAM1_DQ<8>\I 230 P230
RAM1_A<10>\I 229 P229
228 GND
IP_VID_OUT<3>\I 227 P227
IP_VID_OUT<1>\I 226 P226
RAM2_DQ<10>\I 225 P225
DEL_VID<6>\I 224 P224
PLX_LA<10>\I 223 P223
222 P222
VCCIO 221
PLX_LA<11>\I 220 P220
IP_VID<5>\I 219 P219
RAM2_DQ<0>\I 218 P218
RAM2_DQ<6>\I 217 P217
RAM2_DQ<2>\I 216 P216
PLX_LD<0>\I 215 P215
214 GND
RAM2_DQ<12>\I 213 P213
PLX_LA<13>\I 212 P212
211 P211
RAM2_DQ<3>\I 210 P210
209 VCC
208 GND
PLX_LA<5>\I 207 P207
RAM2_DQ<5>\I 206 P206
205 VCCIO
RAM1_DQ<5>\I 204 P204
DEL_VID<5>\I 203 P203
RAM2_DQ<4>\I 202 P202
PLX_LA<12>\I 201 P201
PLX_LA<8>\I 200 P200
PLX_LA<7>\I 199 P199
198 GND
IP_VID<1>\I 197 P197
DEL_VID<7>\I 196 P196
195 P195
PLX_LD<5>\I 194 P194
193 P193
192 P192
VCCIO 191
PLX_LA<21>\I 190 P190
PLX_LD<7>\I 189 P189
RAM2_DQ<7>\I 188 P188
DATA0\I 187 P187
186 GND
185 GND
184 GND
DCLK\I 183 DCLK
IP_HSn\I 182 P182
RAM2_A<1>\I 181 P181

RAM1_DQM\I 1 P1
RAM2_CKE\I 2 P2
RAM2_DQM\I 3 P3
sync_reset\I 4 P4
IP_VID_OUT<7>\I 5 P5
6 GND
7 GND
CLK\I 8 P8
PLX_LD<15>\I 9 P9
PLX_LD<11>\I 10 P10
PLX_LD<9>\I 11 P11
PLX_LD<10>\I 12 P12
PLX_LD<1>\I 13 P13
PLX_LD<2>\I 14 P14
RAM2_DQ<13>\I 15 P15
PLX_LD<3>\I 16 P16
17 VCCIO
18 VCC
MSEL0\I 19 MSEL0
PLX_LA<19>\I 20 P20
RAM2_A<2>\I 21 P21
read_1\I 22 P22
RAM2_A<7>\I 23 P23
24 P24
RAM2_A<6>\I 25 P25
RAM2_A<5>\I 26 P26
field_index\I 27 P27
28 GND
29 GND
IP_VSn\I 30 P30
RAM2_A<10>\I 31 P31
tv_vert_active\I 32 P32
RSTRn\I 33 P33
RAM2_WEn\I 34 P34
RAM1_A<11>\I 35 P35
TV_HORZ_ACTIVE\I 36 P36
RAM1_CSn\I 37 P37
MSEL1\I 38 MSEL1
39 VCCIO
40 VCC
RAM1_DQ<2>\I 41 P41
IP_VID_OUT<4>\I 42 P42
RAM1_DQ<12>\I 43 P43
RAM1_DQ<7>\I 44 P44
RAM1_DQ<13>\I 45 P45
RAM1_DQ<10>\I 46 P46
RAM1_DQ<14>\I 47 P47
RAM1_DQ<9>\I 48 P48
RESETn\I 49 P49
50 GND
51 GND
PLX_LA<20>\I 52 P52
DAC_VID<0>\I 53 P53
DAC_CSn\I 54 P54
55 P55
IP_AUX_PIX_SELn\I 56 P56
57 P57
DAC_VID<3>\I 58 P58
RAM2_A<4>\I 59 P59
60 VCC

P180 180 RAM1_A<8>\I
P179 179 RAM2_A<11>\I
P178 178 IP_VID_OUT<2>\I
P177 177 IP_VID_OUT<6>\I
P176 176 RAM2_CASn\I
P175 175 DAC_VID<2>\I
VCCIO 174
VCC 173
P172 172 PLX_LA<2>\I
P171 171 RAM1_CKE\I
P170 170 PLX_LD<8>\I
P169 169 read_2\I
P168 168 PLX_LD<6>\I
P167 167 PLX_LD<12>\I
P166 166 PLX_LD<4>\I
P165 165 PLX_LD<14>\I
P164 164 PLX_LD<13>\I
GND 163
GND 162
CONF_DONE 161 CONF_DONE\I
P160 160
P159 159 RAM1_A<7>\I
P158 158 ip_vert_active\I
P157 157 RAM2_A<9>\I
P156 156 RAM1_A<1>\I
P155 155 RAM2_A<0>\I
P154 154 RAM1_A<2>\I
P153 153 RAM2_A<8>\I
VCCIO 152
VCC 151
P150 150 PLX_LRDYn\I
P149 149 RAM1_A<5>\I
P148 148 RAM2_RASn\I
P147 147 RAM1_RASn\I
P146 146 RAM1_WEN\I
P145 145 RSTWn\I
P144 144 ip_horz_active\I
P143 143 IP_VID_OUT<0>\I
nSTATUS 142 STATUSn\I
GND 141
GND 140
P139 139 IP_VID_OUT<5>\I
P138 138 DAC_VID<6>\I
P137 137 RAM1_DQ<6>\I
P136 136 SDOUT\I
P135 135 RAM1_DQ<0>\I
P134 134 RAM1_DQ<3>\I
P133 133 RAM1_DQ<1>\I
P132 132 RAM1_DQ<4>\I
P131 131 CHIP_HIZn\I
VCCIO 130
VCC 129
P128 128 DAC_VID<4>\I
P127 127 RAM1_A<9>\I
P126 126 DAC_CBn\I
P125 125 RAM2_CSn\I
P124 124
P123 123
P122 122 RAM1_A<0>\I
P121 121 RAM1_A<3>\I

EPF81500AQC240

SPEED=A_4

NOTE:

THIS COMPONENT BODY DRAWING IS NOT INTENDED FOR PRODUCTION SCHEMATIC USE.

PACK_TYPE=SQFPU33

61 VCCIO
62 VCC
JTAG_TDI\I 63 TDI
JTAG_TMS\I 64 TMS
RAM2_A<3>\I 65 P65
RAM1_DQ<11>\I 66 P66
67 P67
68 P68
69 P69
RAM1_DQ<15>\I 70 P70
71 GND
72 P72
PLX_LA<4>\I 73 P73
DEL_VID<3>\I 74 P74
PLX_LA<15>\I 75 P75
RAM2_DQ<15>\I 76 P76
77 P77
78 VCCIO
PLX_LA<18>\I 79 P79
PLX_LA<22>\I 80 P80
PLX_CS1n\I 81 P81
DEL_VID<0>\I 82 P82
IP_VID<4>\I 83 P83
RAM2_DQ<1>\I 84 P84
85 GND
RAM2_DQ<8>\I 86 P86
RAM2_DQ<9>\I 87 P87
88 P88
RAM2_DQ<14>\I 89 P89
PLX_LWRn\I 90 P90
91 VCC
92 GND
93 P93
RAM2_DQ<11>\I 94 VCCIO
PLX_LA<9>\I 95 P95
PLX_CS0n\I 96 P96
DEL_VID<1>\I 97 P97
DEL_VID<4>\I 98 P98
99 P99
IP_VID<2>\I 100 P100
101 GND
PLX_LA<6>\I 102 P102
PLX_LA<3>\I 103 P103
PLX_LA<17>\I 104 P104
IP_VID<7>\I 105 P105
IP_VID<0>\I 106 P106
PLX_LA<23>\I 107 P107
108 VCCIO
PLX_LA<16>\I 109 P109
PLX_LA<20>\I 110 P110
PLX_LA<14>\I 111 P111
IP_VID<3>\I 112 P112
DEL_VID<2>\I 113 P113
114 VCC
JTAG_TRSTn\I 115 nTRST
JTAG_TCLK\I 116 TCLK
JTAG_TDO\I 117 TDO
118 GND
CONFIGn\I 119 GND
120 nCONFIG

TV VIDEO CONTROL

DRAWING

LAST_MODIFIED=Thu May 21 12:45:56 1998

OEC MEDICAL SYSTEMS, INC.

SIZE	DWG NO.	REV
D	00-878955	A

SCALE: | SHEET 18 OF 22

05-017-9/93

*** Signal Cross-Reference ***
--- for the entire design --

```
ACK *            7B2
AD <31..0>       1A8 1B8 1C8 1C7
AD_D0            2B5
AD_D1            2B5
AD_D2            2B5
AD_D3            2B5
AD_D4            2B5
AD_D5            2B5
AD_D6            2B5
AD_D7            2B5
AD_WREN *        2A5
AFDXT *          7B2
AUX_PIXWE_IN *   2A1
AUX_PIX_DATA <7..0> 2B1 2B3 12C8
BUSY             7B2
C/BE <3..0> *    1C8 1C7
CLK              1D8
COMP_VGA_VIDEO   7B5 3A1 4A1
DAC_VID <7..0>   12B5 12C4
DC_HDRV *        2A5
DC_VDRV *        2A5
DEL_VID <7..0>   12B7
DEVSEL *         1C8
EPP_IOCHRDY *    7C7 9B8
EPP_IRQ *        7C7 1D1 9B8
ERROR *          7B2
EXP_ROM_CS *     9B6 7D7
EXP_ROM_OE *     9B6 7D7
FRAME *          1C8
HDRV_IN *        2A1 9C4 9C8 12C8
IDSEL            1C8
INIT             7B2
INTA *           1C8
IP_AUX_PIX_SEL * 12C8 2D1
IP_CLK_SEL *     9C6 2D6
IP_DATA_TAG *    2A1
IP_DIS_PIXCLK    2D6
IP_LFT_PIX_SEL * 9D6 2D1
IP_RT_PIX_SEL *  9D2 2D1
IP_VID_OUT <7..0> 12A7 12B8
IRDY *           1C8
JTAG_CASCADE1    9B8 9B4
JTAG_CASCADE2    9B4 12A8
JTAG_TCK         1D6 9B4 9B8 12A8
JTAG_TDI         1D6 9B8
JTAG_TDO         12A8 1D6
JTAG_TMS         1D6 9B4 9B8 12A8
JTAG_TRST *      1D6 9B4 9B8 12A8
L/R_CONFIG *     9D8
L/R_CONF_CASCADE 9D6
L/R_CONF_DATA0   9A6 9D2 9D6
L/R_CONF_DCLK    9A6 9D2 9D6
L/R_CONF_DONE    9D2 9A6
L/R_CONF_MSEL1   9D8
L/R_CONF_STATUS * 9A6 9D6
LD_D0            2C5
LD_D1            2C5
LD_D2            2C5
LD_D3            2C5
LD_D4            2C5
LD_D5            2C5
LD_D6            2C5
LD_D7            2C5
LD_WREN *        2A5
LEFT_PIX_DATA <7..0> 1A1 1B2 2C1 2C3 5A7 5A8
LEFT_PIX_WE *    9C6 5A8
LFT_MUXED_CLK_A  2D1 5C8 9C8
LFT_MUXED_CLK_B  2D1 3A8
LOCK *           1C8
LPT_RESET        1C1 7C7
```

```
L_AVDD           3C5
L_DAC_BLANK *    9B6 3A8
L_DAC_HSYNC *    9B6 3A8
L_DAC_LCLK       9B6 3B8
L_DAC_RCLK       3A8 9C8
L_DAC_RD *       9B6 3B8
L_DAC_RESET *    9B6 3B8
L_DAC_VSYNC *    9B6 3A8
L_DAC_WR *       9B6 3B8
L_DISPLAY_DATA <127..0> 5A1 5A2 5A4 5B2 5B4 5C2 5C4
                 5D2 5D4 3B6 3B7 3B8
L_FIFO_AEA *     5D8 9C8
L_FIFO_AEB *     5B8 9C8
L_FIFO_AFA *     5C8 9C8
L_FIFO_AFB *     5C8 9C8
L_FIFO_A_W/R *   9C6 5C8
L_FIFO_B_W/R *   9C6 5C8
L_FIFO_CSA *     9C6 5C8
L_FIFO_CSB *     9B6 5C8
L_FIFO_EFA *     5D8 9C8
L_FIFO_EFB *     5B8 9C8
L_FIFO_ENA       9C6 5D8
L_FIFO_ENB       9B6 5C8
L_FIFO_FFA *     5C8 9C8
L_FIFO_FFB *     5C8 9C8
L_FIFO_MBA       9C6 5D8
L_FIFO_RESET *   9C6 5C8
L_FIFO_SIZE0     9B6 5C8
L_FIFO_SIZE1     9B6 5C8
L_IP_ACTIVE_LED * 9B6 7A7
L_MVR_A <8..0>   9C6 5A8 5B5 5C5 5D5
L_MVR_CAS *      9C6 5D8
L_MVR_DSF        9C6 5D8
L_MVR_DTOE *     9C6 5D8
L_MVR_RAS *      9C6 5D8
L_MVR_SCLK       9C6 5D8
L_MVR_SCLK_EN *  9C6 5D8
L_MVR_WE <4..1> * 9C5 5D8 9C6
L_PIXWE_IN *     2A1 9C8
L_PIX_DATA <31..0> 5A2 5A5 5A6 5B2 5B5 5B6 5C2 5C5
                 5A5
L_SVR_A <8..0>   9C6 5A8 5B3 5C3 5D3
L_SVR_CAS *      9C6 5D8
L_SVR_DSF        9C6 5B1
L_SVR_DTOE *     9C6 5B1
L_SVR_QSF        5B1 9C8
L_SVR_RAS *      9C6 5D8
L_SVR_SCLK       9C6 5C1
L_SVR_SCLK_EN *  9C6 5C1
L_SVR_WE <4..1> * 9C5 5D8 9C6
L_UNBLANK_LED *  9B6 7A7
L_VGA <7..0>     3A5
L_VGA_SEL        9B6 3A1
L_VIDEO_ACTIVE_LED * 3A8 7A7
MUXED_CLK        2D1 1D1 12C8
PAR              1C8
PCB_CFG_RD *     9B6 7C7
PD0              7B2
PD1              7B2
PD2              7B2
PD3              7B2
PD4              7B2
PD5              7B2
PD6              7B2
PD7              7B2
PE               7B2
PERR *           1C8
PLX_8BIT_LA <14..0> 1B1 7B4 3B8 4B8 7B4 7C7 7D7
PLX_ADS *        1C1 9D4 9D8
PLX_ALE          1C1 9C8 9D4
PLX_BCLKO        1D1 2D6
PLX_BCLKO_SEL *  9D6 2D6
PLX_BLAST *      1C1 9C8 9D4
```

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PLX_BTERM *      9D2 9D6 1C1
PLX_CS0 *        1C1 9D4 9D8 12C8
PLX_CS1 *        1C1 9D4 9D8 12C8
PLX_CS2 *        1C1 7C7 9D8
PLX_CS3 *        1C1
PLX_LA <27..2>   1C1 1B2 9C4 9C8 12C8
PLX_LBE <3..0>   1C1 1B2
PLX_LD <31..0>   1A4 1A5 1A6 1C1 3B8 4B8 5A7 5B7 5B8
                 6A7 6B7 6B8 7B4 7C3 7C7 7D3 7D6 9C4
                 9C8 12C8 1A3 1B3
PLX_LFT_PIXDATA_RD * 9D6 1B1
PLX_LFT_PIX_SEL * 9D6 1B1
PLX_LINT1        1D1
PLX_LINT2 *      9D6 1D1
PLX_LOAD_OK *    1B1 7A7
PLX_LRD *        1D1 7C7 9D4 9D8
PLX_LRDY *       9D2 9D6 12C8 1C1
PLX_LRESET *     1D1 9D4 9D8 12C8
PLX_LWAIT0 *     1C1 9C8 9D4
PLX_LWR *        1D1 7C7 9D4 9D8 12C8
PLX_LW_RD *      1D1 9D4 9D8 12C8
PLX_RT_PIXDATA_RD * 9D2 1B1
PLX_RT_PIX_SEL * 9D2 1B1
PRSNT2 *         1D8
RAM1_A <11..0>   12C5
RAM1_DQ <15..0>  12C4 12C5
RAM2_A <11..0>   12A5 12B5
RAM2_DQ <15..0>  12A4 12B4 12A5
RD_D0            2B5
RD_D1            2B5
RD_D2            2C5
RD_D3            2C5
RD_D4            2C5
RD_D5            2C5
RD_D6            2C5
RD_D7            2C5
RD_WREN *        2A5
RST *            1D8
RT_MUXED_CLK_A   2D1 6C8 9C4
RT_MUXED_CLK_B   2D1 4A8
RT_PIX_DATA <7..0> 1A1 1A2 2B1 2B3 2C3 6A7 6A8
RT_PIX_WE *      9D2 6A8
R_AVDD           4C5
R_DAC_BLANK *    9B2 4A8
R_DAC_HSYNC *    9B2 4A8
R_DAC_LCLK       9B2 4B8
R_DAC_RCLK       4A8 9C4
R_DAC_RD *       9B2 4B8
R_DAC_RESET *    9B2 4B8
R_DAC_VSYNC *    9B2 4A8
R_DAC_WR *       9B2 4B8
R_DISPLAY_DATA <127..0> 6A1 6A2 6A4 6B2 6B4 6C2 6C4
                 6D2 6D4 4B6 4B7 4B8
R_FIFO_AEA *     6D8 9C4
R_FIFO_AEB *     6B8 9C4
R_FIFO_AFA *     6C8 9C4
R_FIFO_AFB *     6C8 9C4
R_FIFO_A_W/R *   9C2 6C8
R_FIFO_B_W/R *   9C2 6C8
R_FIFO_CSA *     9C2 6C8
R_FIFO_CSB *     9C2 6C8
R_FIFO_EFA *     6D8 9C4
R_FIFO_EFB *     6B8 9C4
R_FIFO_ENA       9C2 6D8
R_FIFO_ENB       9C2 6C8
R_FIFO_FFA *     6C8 9C4
R_FIFO_FFB *     6C8 9C4
R_FIFO_MBA       9C2 6D8
R_FIFO_RESET *   9C2 6C8
R_FIFO_SIZE0     9C2 6C8
R_FIFO_SIZE1     9B2 6C8
R_IP_ACTIVE_LED * 9B2 7A7
R_MVR_A <8..0>   9C2 6A8 6B5 6C5 6D5
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R_MVR_CAS *      9C2 6D8
R_MVR_DSF        9C2 6D8
R_MVR_DTOE *     9C2 6D8
R_MVR_RAS *      9C2 6D8
R_MVR_SCLK       9C2 6D8
R_MVR_SCLK_EN *  9C2 6D8
R_MVR_WE <4..1> * 9C1 6D8 9D2
R_PIXWE_IN *     2A1 9C4
R_PIX_DATA <31..0> 6A3 6A5 6A6 6B3 6B5 6B6 6C3 6C5
                 6A5
R_SVR_A <8..0>   9C2 6A8 6B3 6C3 6D3
R_SVR_CAS *      9C2 6D8
R_SVR_DSF        9C2 6B1
R_SVR_DTOE *     9C2 6B1
R_SVR_QSF        6B1 9C4
R_SVR_RAS *      9C2 6D8
R_SVR_SCLK       9C2 6C1
R_SVR_SCLK_EN *  9C2 6C1
R_SVR_WE <4..1> * 9C1 6D8 9C2
R_UNBLANK_LED *  9B2 7A7
R_VGA <7..0>     4A5
R_VGA_SEL        9B2 4A1
R_VIDEO_ACTIVE_LED * 4A8 7A7
SERR *           1C8
SLCT             7B2
SLCTI *          7B2
STOP *           1C8
STROBE *         7B2
TAG *            2A5
TRDY *           1C8
TV_CONFIG *      12D7
TV_CONF_DATA0    12D7
TV_CONF_DCLK     12D7
TV_CONF_DONE     12D7 7A7
TV_CONF_MSEL1    12D7
TV_CONF_STATUS * 12D7
VDRV_IN *        2A1 9C4 9C8 12C8
VGA_XIN1         7B7 9B6
VGA_XIN2         7B7 9B6
VGA_XOUT         9B6 7A7
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OEC MEDICAL SYSTEMS, INC.

SIZE	DWG NO.	REV
D	00-878955	A
SCALE:		SHEET 19 OF 22

05-017-9/93

*** Unit Cross-Reference ***
--- for the entire design --

C1	CERR_2X2U_41206990	3C1
C2	TASMT_7343	3C3
C3	TASMT_6032	3C2
C4	TASMT_7343	3C6
C5	CERR_0X22U_41207011	3C4
C6	CERSMT_1206	3C3
C7	CERSMT_1206	3C3
C8	CERSMT_1206	12C2
C9	CERSMT_1206	12C1
C10	CERSMT_1206	4C3
C11	CERSMT_1206	4C3
C12	TASMT_7343	4C3
C13	TASMT_6032	4C2
C14	TASMT_7343	4C6
C15	TASMT_7343	4C5
C16	CERR_0X22U_41207011	4C4
C17	CERR_0X22U_41207011	3C4
C18	TASMT_7343	3C5
C19	TASMT_7343	10A4
C20	TASMT_7343	10A4
C21	CERSMT_1206	9B8
C22	CERSMT_1206	9B4
C23	TASMT_7343	10B5
C24	TASMT_7343	10D5
C25	TASMT_7343	11B2
C26	TASMT_7343	11B3
C27	CERSMT_1206	11B3
C28	TASMT_7343	11B3
C29	CERSMT_1206	11D4
C30	TASMT_7343	11B3
C31	CERSMT_1206	11C2
C32	CERSMT_1206	11B3
C33	TASMT_7343	11B3
C34	CERSMT_1206	11C2
C35	TASMT_7343	11B3
C36	CERSMT_1206	11C2
C37	CERSMT_1206	11C2
C38	TASMT_7343	11B2
C39	TASMT_7343	11B3
C40	CERSMT_1206	11B3
C41	CERSMT_1206	11B3
C42	TASMT_7343	11B3
C43	CERSMT_1206	11B3
C44	CERSMT_1206	11B3
C45	TASMT_7343	11B3
C46	CERSMT_1206	11D3
C47	TASMT_7343	11B3
C48	CERSMT_1206	11B4
C49	TASMT_7343	11B3
C50	TASMT_7343	11B3
C51	CERSMT_1206	3C2
C52	CERSMT_1206	11C3
C53	CERSMT_1206	11B7
C54	CERSMT_1206	11B6
C55	CERSMT_1206	11D2
C56	CERSMT_1206	2B5
C57	CERSMT_1206	2B5
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C93	CERSMT_1206	4C5
C94	CERSMT_1206	4C5
C95	CERSMT_1206	4C2
C96	CERSMT_1206	4A5
C97	CERSMT_1206	4C2
C98	CERSMT_1206	4C3
C99	CERSMT_1206	11D3
C100	CERSMT_1206	4C3
C101	CERSMT_1206	11D7
C102	CERSMT_1206	11D4
C103	CERSMT_1206	11C7
C104	CERSMT_1206	11D3
C105	CERSMT_1206	11B6
C106	CERSMT_1206	11C5
C107	CERSMT_1206	11D4
C108	CERSMT_1206	4C2
C109	CERSMT_1206	4C2
C110	CERSMT_1206	12C1
C111	CERSMT_1206	3C2
C112	CERSMT_1206	3C2
C113	CERSMT_1206	3C5
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C115	CERSMT_1206	3C5
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C118	CERSMT_1206	3C5
C119	CERSMT_1206	3C5
C120	CERSMT_1206	3C5
C121	CERSMT_1206	3A5
C122	CERSMT_1206	11D3
C123	CERSMT_1206	11D7
C124	CERSMT_1206	3C2
C125	CERSMT_1206	3C1
C126	CERSMT_1206	11B6
C127	CERSMT_1206	11B4
C128	CERSMT_1206	11D7
C129	CERSMT_1206	11B4
C130	CERSMT_1206	11B6
C131	CERSMT_1206	11B4
C132	CERSMT_1206	3C3
C133	CERSMT_1206	3C3
C134	CERSMT_1206	11D2
C135	CERSMT_1206	11D7
C136	CERSMT_1206	11C2
C137	CERSMT_1206	11C6
C138	CERSMT_1206	11D3
C139	CERSMT_1206	11D7
C140	CERSMT_1206	2A5
C141	CERSMT_1206	11D3
C142	CERSMT_1206	12C2
C143	CERSMT_1206	12C3
C144	CERSMT_1206	12C2
C145	CERSMT_1206	11D6
C146	CERSMT_1206	11C7
C147	CERSMT_1206	11D4
C148	CERSMT_1206	11D5
C149	CERSMT_1206	11D5
C150	CERSMT_1206	2A5
C151	CERSMT_1206	11D4
C152	CERSMT_1206	2A5
C153	CERSMT_1206	11D6
C154	CERSMT_1206	2A6
C155	CERSMT_1206	11D4
C156	CERSMT_1206	2A6
C157	CERSMT_1206	11D5
C158	CERSMT_1206	2A6
C159	CERSMT_1206	11D3
C160	CERSMT_1206	2A6
C161	CERSMT_1206	11D6
C162	CERSMT_1206	11D3
C163	CERSMT_1206	11D4
C164	CERSMT_1206	11D6
C165	CERSMT_1206	11D5
C166	CERSMT_1206	4C4
C167	CERSMT_1206	4C4
C168	CERSMT_1206	11D4
C169	CERSMT_1206	11D3
C170	CERSMT_1206	11D5
C171	CERSMT_1206	11D6
C172	CERSMT_1206	11D4
C173	CERSMT_1206	11D7
C174	CERSMT_1206	11D6
C175	CERSMT_1206	11D3
C176	CERSMT_1206	11C3
C177	CERSMT_1206	12C1
C178	CERSMT_1206	11B5
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C180	CERSMT_1206	3C4
C181	CERSMT_1206	3C4
C182	CERSMT_1206	3C6
C183	CERSMT_1206	3C4
C184	CERSMT_1206	11D4
C185	CERSMT_1206	11D2
C186	CERSMT_1206	11D7
C187	CERSMT_1206	11D6
C188	CERSMT_1206	11D4
C189	CERSMT_1206	11D7
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C193	CERSMT_1206	11B4
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C195	CERSMT_1206	11B5
C196	CERSMT_1206	11A4
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C198	CERSMT_1206	11A4
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C200	CERSMT_1206	11A5
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C203	CERSMT_1206	11B5
C204	CERSMT_1206	11A5
C205	CERSMT_1206	12C3
C206	CERSMT_1206	11B4
C207	CERSMT_1206	11A4
C208	CERSMT_1206	11B5
C209	CERSMT_1206	11B3
C210	CERSMT_1206	11D7
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C212	CERSMT_1206	11D3
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C283	CERSMT_1206	11C3
C284	CERSMT_1206	11A4
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C290	CERSMT_1206	11B5
C291	CERSMT_1206	11D6
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C302	CERSMT_1206	11C3
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C309	CERSMT_1206	11C6
C310	CERSMT_1206	11C6
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C313	CERSMT_1206	11C3
C314	CERSMT_1206	11C3
C315	CERSMT_1206	11C6
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C317	CERSMT_1206	11D6
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C321	CERSMT_1206	7C2
C322	CERSMT_1206	11C6
C323	CERSMT_1206	11B2
C324	CERSMT_1206	11B5
C325	CERSMT_1206	11D3
C326	CERSMT_1206	11D4
C327	CERSMT_1206	11D7
C328	CERSMT_1206	11D5
C329	CERSMT_1206	11A5
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C358	CERSMT_1206	11B7
C359	CERSMT_1206	11C5
C360	CERSMT_1206	11C6
C361	CERSMT_1206	11C5
C362	CERSMT_1206	11C3

C363	CERSMT_1206	11C5
C364	CERSMT_1206	11C4
C365	CERSMT_1206	11C6
C366	CERSMT_1206	11C5
C367	CERSMT_1206	11C3
C368	CERSMT_1206	11C4
C369	CERSMT_1206	11C6
C370	CERSMT_1206	11C3
C371	CERSMT_1206	11C6
C372	CERSMT_1206	11C4
C373	CERSMT_1206	11C2
C374	CERSMT_1206	11C5
C375	CERSMT_1206	11C6
C376	CERSMT_1206	11C6
C377	CERSMT_1206	11C4
C378	CERSMT_1206	11C3
C379	CERSMT_1206	11C3
C380	CERSMT_1206	11C2
C381	CERSMT_1206	11C5
C382	CERSMT_1206	11C5
C383	CERSMT_1206	11C4
C384	CERSMT_1206	11C4
C385	CERSMT_1206	11C7
C386	CERSMT_1206	11C5
C387	CERSMT_1206	11C4
C388	CERSMT_1206	11C4
C389	CERSMT_1206	11C7
C390	CERSMT_1206	11C5
C391	CERSMT_1206	11C4
C392	CERSMT_1206	11C4
C393	CERSMT_1206	11C7
C394	CERSMT_1206	11C5
C395	CERSMT_1206	11C4
C396	CERSMT_1206	11C4
C397	CERSMT_1206	11C7
C398	CERSMT_1206	11C6
C399	CERSMT_1206	11C6
C400	CERSMT_1206	11C5
C401	CERSMT_1206	11C4
C402	CERSMT_1206	11C3
C403	CERSMT_1206	11C3
C404	CERSMT_1206	11C4
C405	CERSMT_1206	11D4
C406	CERSMT_1206	11D6
C407	CERSMT_1206	11D6
C408	CERSMT_1206	11D3
C409	CERSMT_1206	11B2
C410	CERSMT_1206	11B5
C411	CERSMT_1206	11B2
C412	CERSMT_1206	11B5
C413	CERSMT_1206	11B5
C414	CERSMT_1206	11B6
C415	CERSMT_1206	11B4
C416	CERSMT_1206	11B3
C417	CERSMT_1206	11C5
C418	CERSMT_1206	11B5
C419	CERSMT_1206	11B4
C420	CERSMT_1206	11B6
C421	CERSMT_1206	11C7
C422	CERSMT_1206	11C4
C423	CERSMT_1206	11C7
C424	CERSMT_1206	11C3
C425	CERSMT_1206	11C7
C426	CERSMT_1206	11C3
C427	CERSMT_1206	11C6
C428	CERSMT_1206	11C5
C429	CERSMT_1206	11B7
C430	CERSMT_1206	11D4
C431	CERSMT_1206	11C7
C432	CERSMT_1206	11C4
C433	CERSMT_1206	11C7
C434	CERSMT_1206	11C3
C435	CERSMT_1206	11C6

C436	CERSMT_1206	11C3
C437	CERSMT_1206	11C6
C438	CERSMT_1206	11C3
C439	CERSMT_1206	11C6
C440	CERSMT_1206	11C6
C441	CERSMT_1206	11C6
C442	CERSMT_1206	11C3
C443	CERSMT_1206	11B4
C444	CERSMT_1206	11D7
C445	CERSMT_1206	11C3
C446	CERSMT_1206	11B5
C447	CERSMT_1206	11C7
C448	CERSMT_1206	11B4
C449	CERSMT_1206	11C6
C450	CERSMT_1206	11C3
C451	CERSMT_1206	11C6
C452	CERSMT_1206	11B4
C453	CERSMT_1206	11C6
C454	CERSMT_1206	11C6
C455	CERSMT_1206	11C2
C456	CERSMT_1206	11C2
C457	CERSMT_1206	11C5
C458	CERSMT_1206	11B4
C459	CERSMT_1206	1D6
C460	CERSMT_1206	11C7
C461	CERSMT_1206	11C4
C462	CERSMT_1206	11C4
C463	CERSMT_1206	7B3
C464	CERSMT_1206	7B3
C465	CERSMT_1206	7B3
C466	CERSMT_1206	7B3
C467	CERSMT_1206	7B3
C468	CERSMT_1206	7B3
C469	CERSMT_1206	11B7
C470	CERSMT_1206	11B7
C471	CERSMT_1206	11B7
C472	CERSMT_1206	11B7
C473	CERSMT_1206	11B7
C474	CERSMT_1206	11B7
C475	CERSMT_1206	11B7
C476	CERSMT_1206	11B7
C477	CERSMT_1206	11B6
C478	CERSMT_1206	11B6
C479	CERSMT_1206	11B7
C480	CERSMT_1206	11B7
C481	CERSMT_1206	11B7
C482	CERSMT_1206	11B7
C483	CERSMT_1206	11B7
C484	CERSMT_1206	11B7
C485	CERSMT_1206	11B7
C486	CERSMT_1206	11B7
C487	CERSMT_1206	11B6
C488	CERSMT_1206	11C5
C489	CERSMT_1206	11C5
C490	CERSMT_1206	11B7
C491	CERSMT_1206	11B6
C492	CERSMT_1206	11B6
C493	CERSMT_1206	11B7
C494	CERSMT_1206	10D5
C495	CERSMT_1206	10D5
C496	CERSMT_1206	10B5
C497	CERSMT_1206	10B5
C498	CERSMT_1206	7B3
C499	CERSMT_1206	7B2
CR1	1N4005	3C5
CR2	1N4005	4C5
CR3	SCHOTTKY_SMT_BAT54C	7B6
CR4	DIO_SMT_BAV99	4B2
CR5	DIO_SMT_BAV99	4B2
CR6	DIO_SMT_BAV99	4B2
CR7	DIO_SMT_BAV99	12C1
CR8	DIO_SMT_BAV99	12C1
CR9	DIO_SMT_BAV99	12C1

CR10	DIO_SMT_BAV99	3B2
CR11	DIO_SMT_BAV99	3B2
CR12	DIO_SMT_BAV99	3B2
DS1	LED4_67480200	7A6
DS2	LED4_67480200	7A5
E1	JMPST_1X3_90012601	7B5
FL1	EMI_FLTR_43600000	10A5
FL2	EMI_FLTR_43600000	7C2
FL3	EMI_FLTR_43600000	10B5
FL4	EMI_FLTR_43600000	10D5
L1	FR_BD_SMT_43610000	4C4
L2	FR_BD_SMT_43610000	4C4
L3	FR_BD_SMT_43610000	4C6
L4	FR_BD_SMT_43610000	3C6
L5	FR_BD_SMT_43610000	3C4
L6	FR_BD_SMT_43610000	3C4
P1	CONN_EDGE_PCI_124_5V	1A7 1A8 1A8 1A8 1B7 1B7 1B7 1B8 1B8 1B8 1B8 1C8 1D8 1D8 1D8 1D8 10A8 10B8 10B8 10C8 10C8 10D8
P2	MINJRRA_2X4_51411109	10A5
P3	CONN_SMBH_AG_58019880	3B1
P4	CONN_SMBH_AG_58019880	3B1
P5	CONN_SMBH_AG_58019880	3B1
P6	CONN_SMBH_AG_58019880	4B1
P7	CONN_SMBH_AG_58019880	4B1
P8	CONN_SMBH_AG_58019880	4B1
P9	D50RA_80P_51180008	2A6 2A6 2A6 2B6 2B6 2B6 2B6 2B7 2B7 2B7 2B7 2C6 2C6 2C6 2C7 2C7 2C7 2C7 2C7 2C7 2D7
P10	HDRIBST_2X5_51190165	9A4
P11	DSUBRA_25_CHAS_51109724	7A2 7A2 7A2 7B2 7B2 7B2 7B2
P12	CONN_SMBH_AG_58019880	12C1
P13	CONN_SMBH_AG_58019880	12C1
P14	CONN_SMBH_AG_58019880	12B1
P15	DSUBRA_15_HD_NC_51970020	7B7
P16	HDBKST_2X5_90012602	12D8
R1	RESSMT_1206	3B3
R2	RESSMT_1206	3B4
R3	RESSMT_1206	3C4
R4	RESSMT_1206	3C4
R5	RES10SIP9X	3C7
R6	RESSMT_1206	3B2
R7	RESSMT_1206	3B3
R8	RESSMT_1206	3C3
R9	RESSMT_1206	3B3
R10	RESSMT_1206	3B3
R11	RESSMT_1206	12B1
R12	RESSMT_1206	12B2
R13	RESSMT_1206	12D1
R14	RESSMT_1206	12C2
R15	RESSMT_1206	12C2
R16	RESSMT_1206	4B3
R17	RESSMT_1206	4C3
R18	RESSMT_1206	4B2
R19	RESSMT_1206	4B3
R20	RESSMT_1206	4B3
R21	RESSMT_1206	4B2
R22	RES10SIP9X	4C7
R23	RESSMT_1206	4B3
R24	RESSMT_1206	4B4
R25	RESSMT_1206	4B4
R26	RESSMT_1206	2D6
R27	RESSMT_1206	2D5
R28	RESSMT_1206	2D4
R29	RESSMT_1206	2D4
R30	RESSMT_1206	2D4
R31	RESSMT_1206	2A6
R32	RESSMT_1206	2A6
R33	RESSMT_1206	2A6
R34	RESSMT_1206	2A6
R35	RESSMT_1206	2A6
R36	RESSMT_1206	2A5

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D	00-878955	A
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R37	RESSMT_1206	2A5
R38	RESSMT_1206	2D5
R39	RESSMT_1206	7B6
R40	RESSMT_1206	7B7
R41	RESSMT_1206	7B6
R42	RESSMT_1206	7B6
R43	RESSMT_1206	7B7
R44	RESSMT_1206	7B6
R45	RESSMT_1206	7B6
R46	RES11SIP10X	7D4
R47	RES10SIP9X	1B5
R48	RES10SIP9X	1B4
R49	RESSMT_1206	7B3
R50	RESSMT_1206	7B3
R51	RESSMT_1206	7B3
R52	RESSMT_1206	7B3
R53	RESSMT_1206	7B3
R54	RES10SIP9X	1D3
R55	RES10SIP9X	1D4
R56	RESSMT_1206	1D6
R57	RESSMT_1206	9B8
R58	RES10SIP9X	1D5
R59	RES10SIP9X	1B5
R60	RES10SIP9X	1B6
R61	RESSMT_1206	9B4
R62	RESSMT_1206	7B3
R63	RESSMT_1206	7B3
R64	RESSMT_1206	12D8
R65	RESSMT_1206	12D7
R66	RESSMT_1206	12D7
R67	RESSMT_1206	12D7
R68	RESSMT_1206	12D7
R69	RESSMT_1206	7A7
R70	RESSMT_1206	2B5
R71	RESSMT_1206	2B5
R72	RESSMT_1206	2B5
R73	RESSMT_1206	2B6
R74	RESSMT_1206	2B6
R75	RESSMT_1206	2B6
R76	RESSMT_1206	2B6
R77	RESSMT_1206	2B6
R78	RESSMT_1206	2B5
R79	RESSMT_1206	2B5
R80	RESSMT_1206	2B5
R81	RESSMT_1206	2B6
R82	RESSMT_1206	2B6
R83	RESSMT_1206	2B6
R84	RESSMT_1206	2B6
R85	RESSMT_1206	2B6
R86	RESSMT_1206	2C5
R87	RESSMT_1206	2C5
R88	RESSMT_1206	2C5
R89	RESSMT_1206	2C6
R90	RESSMT_1206	2C6
R91	RESSMT_1206	2C6
R92	RESSMT_1206	2C6
R93	RESSMT_1206	2C6
R94	RESSMT_1206	2D4
R95	RESSMT_1206	2D4
R96	RESSMT_1206	2D6
R97	RESSMT_1206	2D5
R98	RESSMT_1206	2D5
R99	RESSMT_1206	4C6
R100	RESSMT_1206	4C4
R101	RESSMT_1206	4C4
R102	RESSMT_1206	4B4
R103	RESSMT_1206	4A5
R104	RESSMT_1206	4A4
R105	RESSMT_1206	4A3
R106	RESSMT_1206	4A4
R107	RESSMT_1206	4B2
R108	RESSMT_1206	4B3
R109	RESSMT_1206	4C3

R110	RESSMT_1206	4B3
R111	RESSMT_1206	4C2
R112	RESSMT_1206	12B1
R113	RESSMT_1206	4C2
R114	RESSMT_1206	4B3
R115	RESSMT_1206	12C1
R116	RESSMT_1206	12C2
R117	RESSMT_1206	12C1
R118	RESSMT_1206	12B2
R119	RESSMT_1206	12B2
R120	RESSMT_1206	12B1
R121	RESSMT_1206	12C1
R122	RESSMT_1206	12B2
R123	RESSMT_1206	3B3
R124	RESSMT_1206	3C3
R125	RESSMT_1206	3B3
R126	RESSMT_1206	3C2
R127	RESSMT_1206	3C2
R128	RESSMT_1206	3B3
R129	RESSMT_1206	3B2
R130	RESSMT_1206	3B2
R131	RESSMT_1206	3C6
R132	RESSMT_1206	3B4
R133	RESSMT_1206	3B4
R134	RESSMT_1206	3A5
R135	RESSMT_1206	3A3
R136	RESSMT_1206	3A4
R137	RESSMT_1206	3A4
R138	RESSMT_1206	12C8
R139	RESSMT_1206	2A5
R140	RESSMT_1206	12C3
R141	RESSMT_1206	7D4
R142	RESSMT_1206	7D4
R143	RESSMT_1206	7C4
R144	RESSMT_1206	7C4
R145	RESSMT_1206	7C4
R146	RESSMT_1206	7C4
R147	RESSMT_1206	7C4
R148	RESSMT_1206	7C4
R149	RESSMT_1206	12C3
R150	RESSMT_1206	6C6
R151	RESSMT_1206	5C6
R152	RESSMT_1206	5C7
R153	RESSMT_1206	7C2
R154	RESSMT_1206	12C7
R155	RESSMT_1206	9D3
R156	RESSMT_1206	6C7
R157	RESSMT_1206	9D7
R158	RESSMT_1206	9D4
R159	RESSMT_1206	9C8
R160	RESSMT_1206	1B6
R161	RESSMT_1206	1D6
R162	RESSMT_1206	9A5
R163	RESSMT_1206	9B5
R164	RESSMT_1206	7C4
R165	RESSMT_1206	7B3
R166	RESSMT_1206	12A8
R167	RESSMT_1206	1B6
R168	RESSMT_1206	1B6
R169	RESSMT_1206	1B6
R170	RESSMT_1206	9B5
R171	RESSMT_1206	9B5
R172	RESSMT_1206	9B5
R173	RESSMT_1206	9B5
TP1	TEST_POINT_COLOR	3C1
TP2	TEST_POINT_COLOR	3D3
TP3	TEST_POINT_COLOR	10B6
TP4	TEST_POINT_COLOR	3B5
TP5	TEST_POINT_COLOR	3B3
TP6	TEST_POINT_COLOR	3D3
TP7	TEST_POINT_COLOR	3D3
TP8	TEST_POINT_COLOR	3B4
TP9	TEST_POINT_COLOR	3B4

TP10	TEST_POINT_COLOR	3D6
TP11	TEST_POINT_COLOR	4B3
TP12	TEST_POINT_COLOR	4A6
TP13	TEST_POINT_COLOR	4C1
TP14	TEST_POINT_COLOR	4D6
TP15	TEST_POINT_COLOR	10B7
TP16	TEST_POINT_COLOR	4B4
TP17	TEST_POINT_COLOR	4B4
TP18	TEST_POINT_COLOR	2D5
TP19	TEST_POINT_COLOR	2D5
TP20	TEST_POINT_COLOR	4D5
TP21	TEST_POINT_COLOR	4D5
TP22	TEST_POINT_COLOR	10B7
TP23	TEST_POINT_COLOR	10D7
TP24	TEST_POINT_COLOR	10B6
TP25	TEST_POINT_COLOR	3D5
TP26	TEST_POINT_COLOR	3D5
TP27	TEST_POINT_COLOR	3C8
TP28	TEST_POINT_COLOR	2D3
TP29	TEST_POINT_COLOR	10B6
TP30	TEST_POINT_COLOR	4C7
TP31	TEST_POINT_COLOR	10D7
TP32	TEST_POINT_COLOR	10B7
TP33	TEST_POINT_COLOR	7C7
TP34	TEST_POINT_COLOR	3B7
TP35	TEST_POINT_COLOR	3C7
TP36	TEST_POINT_COLOR	10B6
TP37	TEST_POINT_COLOR	10D7
TP38	TEST_POINT_COLOR	10B7
TP39	TEST_POINT_COLOR	4C8
TP40	TEST_POINT_COLOR	4B7
TP41	TEST_POINT_COLOR	10D7
TP42	TEST_POINT_COLOR	10B7
TP43	TEST_POINT_COLOR	2D3
TP44	TEST_POINT_COLOR	10B7
TP45	TEST_POINT_COLOR	10B4
TP46	TEST_POINT_COLOR	10D4
TP47	TEST_POINT_COLOR	10B7
TP48	TEST_POINT_COLOR	1D3
TP49	TEST_POINT_COLOR	7C6
TP50	TEST_POINT_COLOR	7C6
TP51	TEST_POINT_COLOR	10D6
TP52	TEST_POINT_COLOR	1D4
TP53	TEST_POINT_COLOR	1D4
TP54	TEST_POINT_COLOR	1D4
TP55	TEST_POINT_COLOR	1D5
TP56	TEST_POINT_COLOR	1D6
TP57	TEST_POINT_COLOR	1D6
TP58	TEST_POINT_COLOR	1D6
TP59	TEST_POINT_COLOR	1D6
TP60	TEST_POINT_COLOR	1D3
TP67	TEST_POINT_COLOR	10B6
U1	7805	3C3
U2	49FCT806T	3B4
U3	7905	3C2
U5	MAX499	3C3
U6	MAX499	12C2
U7	MAX499	4C3
U8	49FCT806T	4B4
U10	49FCT806T	2D5
U11	78L05	4C4
U12	74FCT574A	2D4
U13	74FCT244	7D3
U14	74FCT574A	2A4
U15	74FCT162245T	1B3
U16	74FCT574A	2C4
U17	74FCT574A	2B4
U18	74ABT240	7A7
U19	EPC1	12D7
U20	CA3246	7B6
U21	VRAM_256KX16	5D4
U22	VRAM_256KX16	5B4
U23	VRAM_256KX16	5D2

U24	VRAM_256KX16	5B2
U25	78L05	3C4
U26	FIFO_64X36X2_BMBS	5C7
U27	VRAM_256KX16	6D4
U28	VRAM_256KX16	6B4
U29	VRAM_256KX16	6D2
U30	VRAM_256KX16	6B2
U31	FIFO_64X36X2_BMBS	6C7
U32	BT121VCC	12D3
U33	LT1086	10A4
U34	ST78C36	7C4
U35	27C256_150	7D6
U38	SDRAM_1MX16	12D5
U39	SDRAM_1MX16	12B5
U41	EPC1	9A5
U42	NM93CS46	1B6
U44	485506	12C7
V1	LM285_1X2V	3C6
V2	LM285_1X2V	4C6
XE1	SHORT_PC_X1	3C4
XE2	SHORT_PC_X1	7B5
Y1	OSC_8P_EN_VCC_10TTL	7C3

OEC MEDICAL SYSTEMS, INC.

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D	00-878955	A

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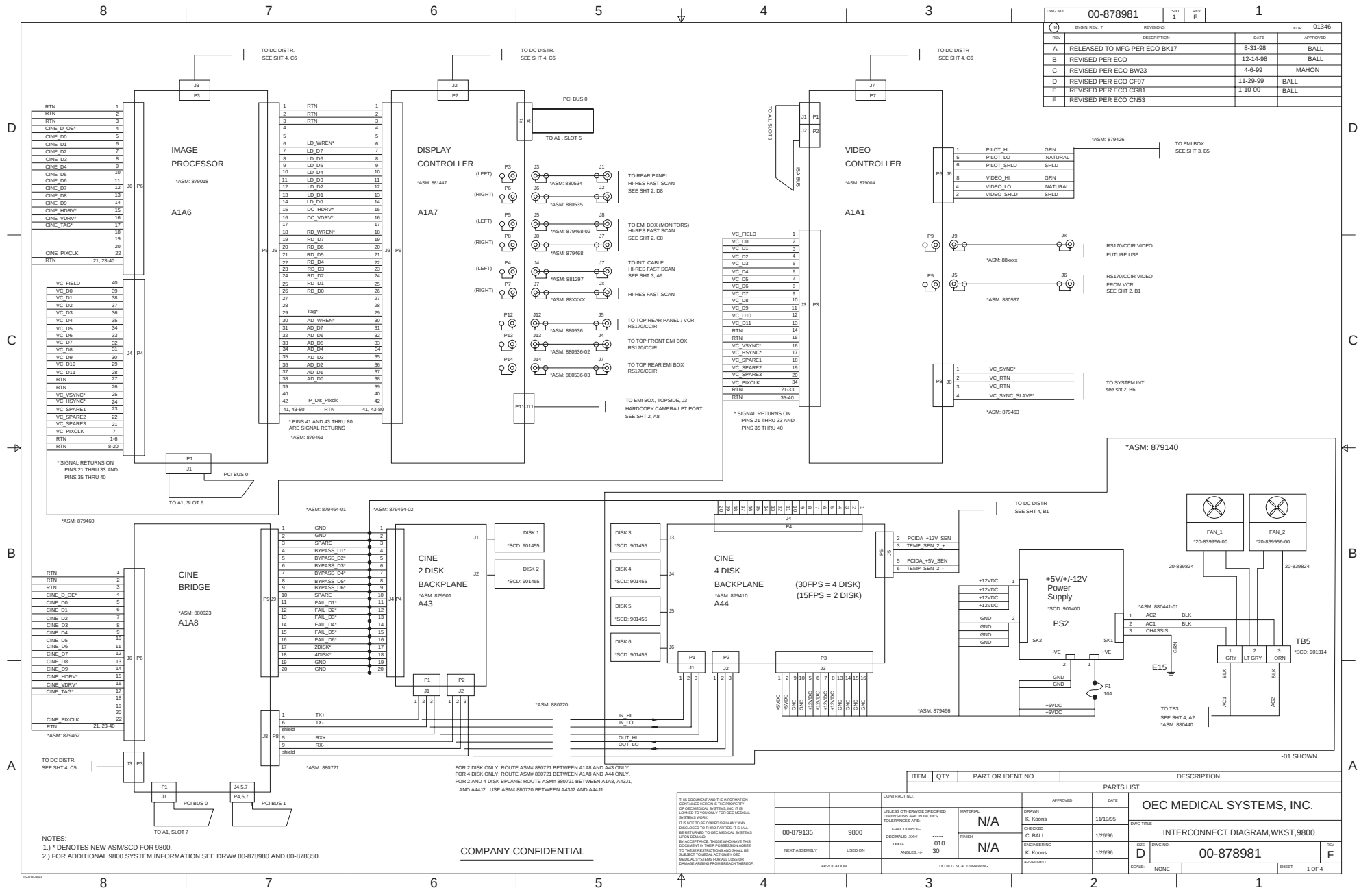

DWG NO.	SHT	REV
00-878981	1	F

ENGN. REV. 7 REVISIONS EDR 01346

REV	DESCRIPTION	DATE	APPROVED
A	RELEASED TO MFG PER ECO BK17	8-31-98	BALL
B	REVISED PER ECO	12-14-98	BALL
C	REVISED PER ECO BW23	4-6-99	MAHON
D	REVISED PER ECO CF97	11-29-99	BALL
E	REVISED PER ECO CG81	1-10-00	BALL
F	REVISED PER ECO CN53		

NOTES:
1.) * DENOTES NEW ASM/SCD FOR 9800.
2.) FOR ADDITIONAL 9800 SYSTEM INFORMATION SEE DRW# 00-878980 AND 00-878350.

FOR 2 DISK ONLY: ROUTE ASM# 880721 BETWEEN A1A8 AND A43 ONLY.
FOR 4 DISK ONLY: ROUTE ASM# 880721 BETWEEN A1A8 AND A44 ONLY.
FOR 2 AND 4 DISK BPLANE: ROUTE ASM# 880721 BETWEEN A1A8, A43J1, AND A44J2. USE ASM# 880720 BETWEEN A43J2 AND A44J1.

COMPANY CONFIDENTIAL

ITEM	QTY.	PART OR IDENT NO.	DESCRIPTION

PARTS LIST

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00-879135	9800
NEXT ASSEMBLY	USED ON
APPLICATION	

CONTRACT NO.
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE:
FRACTIONS +/- -----
DECIMALS: .XX+/- -----
.XXX+/- .010
ANGLES: +/- 30'
MATERIAL N/A
FINISH N/A
DO NOT SCALE DRAWING

	APPROVED	DATE
DRAWN	K. Koons	11/10/95
CHECKED	C. BALL	1/26/96
ENGINEERING	K. Koons	1/26/96
APPROVED		

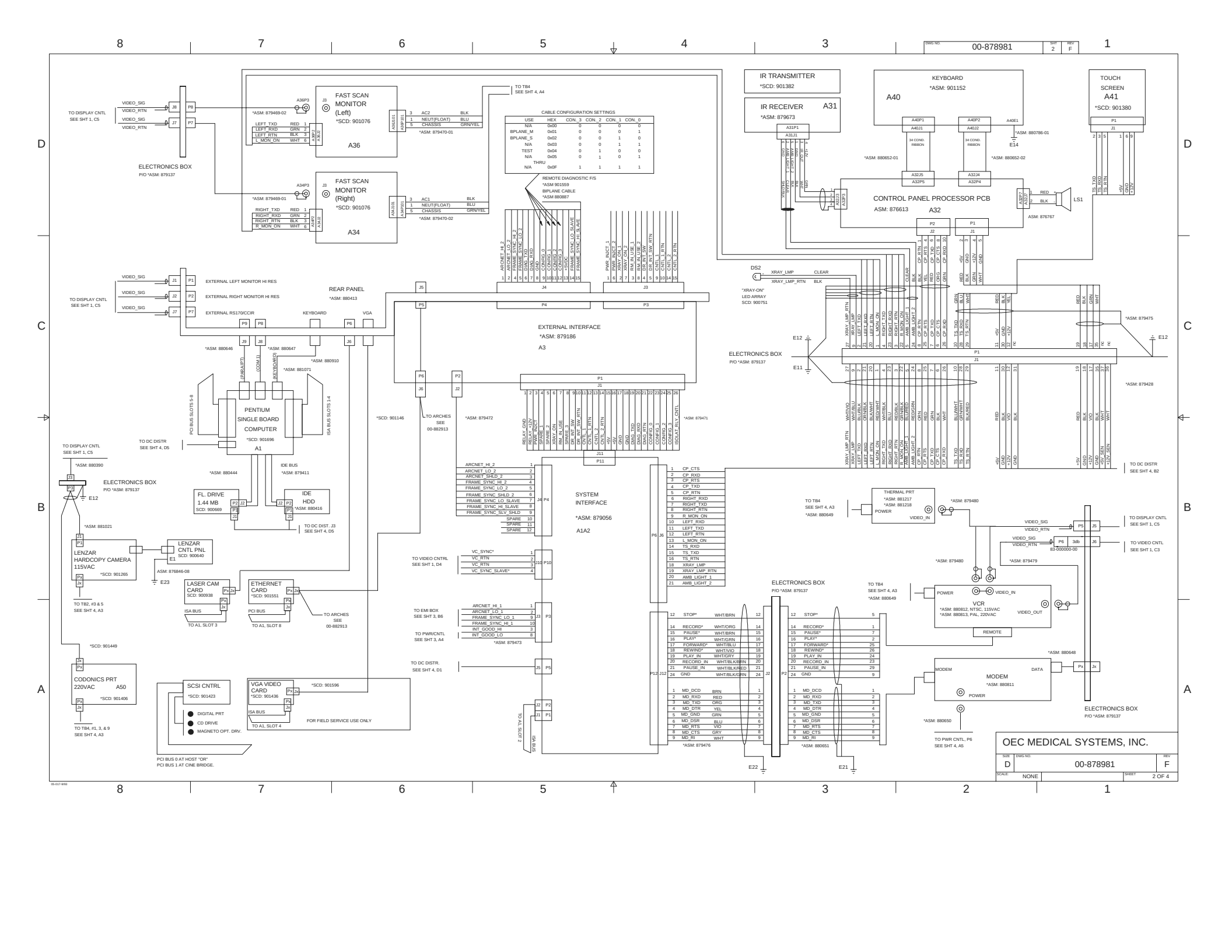
OEC MEDICAL SYSTEMS, INC.

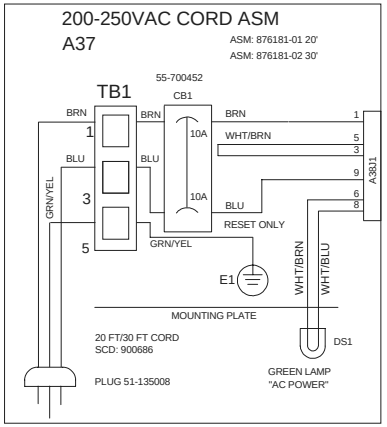
DWG TITLE: INTERCONNECT DIAGRAM,WKST,9800

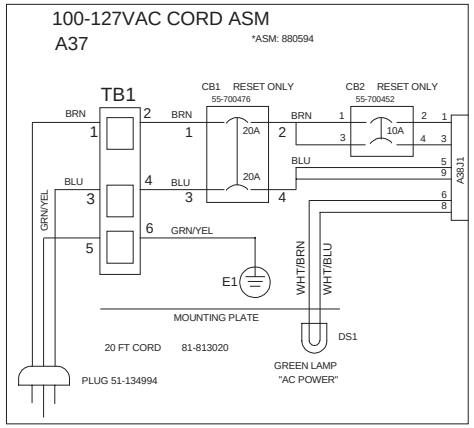
SIZE D | DWG NO. 00-878981 | REV F

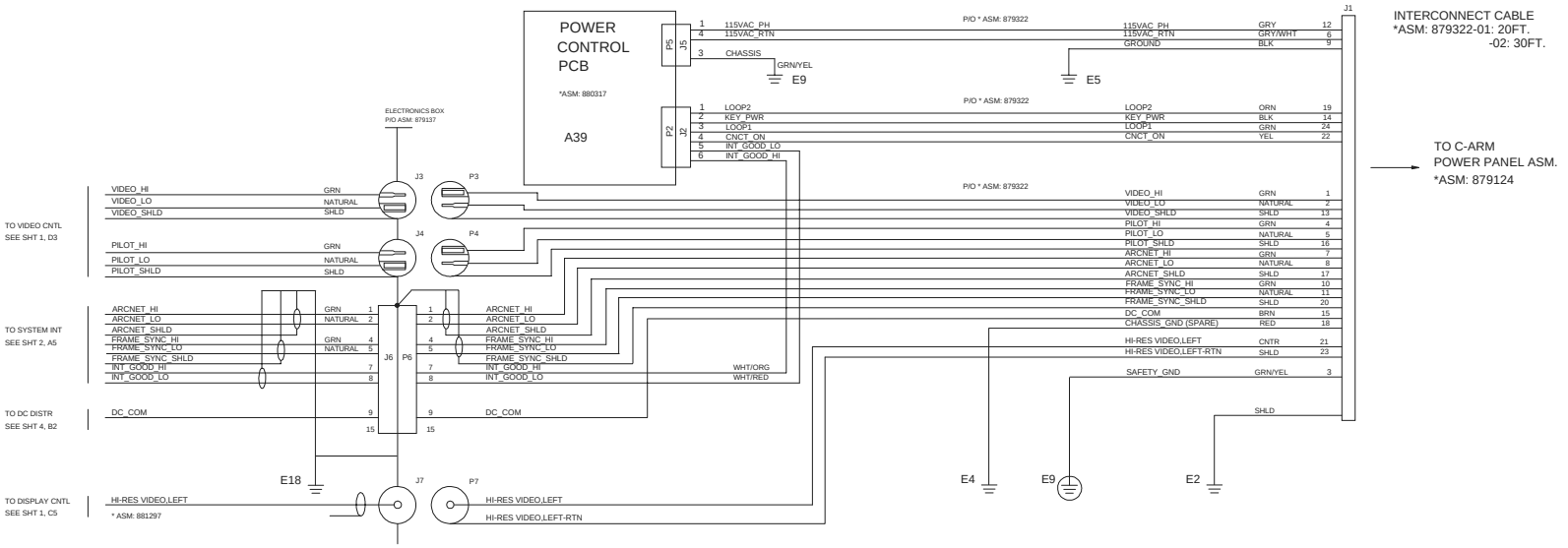
SCALE: NONE | SHEET 1 OF 4

05-016-9/93


00-878981
SHT 2
REV F
ELECTRONICS BOX
P/O *ASM: 879137
FAST SCAN MONITOR (Left)
*SCD: 901076
A36
FAST SCAN MONITOR (Right)
*SCD: 901076
A34
IR TRANSMITTER
*SCD: 901382
IR RECEIVER
*ASM: 879673
A31
KEYBOARD
*ASM: 901152
A40
TOUCH SCREEN
A41
*SCD: 901380
CONTROL PANEL PROCESSOR PCB
ASM: 876613
A32
LS1
ASM: 876767
CABLE CONFIGURATION SETTINGS
REMOTE DIAGNOSTIC F/S
*ASM 901559
BIPLANE CABLE
*ASM 880887
EXTERNAL INTERFACE
*ASM: 879186
A3
REAR PANEL
*ASM: 880413
PENTIUM SINGLE BOARD COMPUTER
*SCD: 901696
A1
SYSTEM INTERFACE
*ASM: 879056
A1A2
FL. DRIVE 1.44 MB
SCD: 900669
IDE HDD
*ASM: 880416
LENZAR HARDCOPY CAMERA 115VAC
*SCD: 901265
LENZAR CNTL PNL
SCD: 900640
LASER CAM CARD
SCD: 900938
ETHERNET CARD
*SCD: 901551
CODONICS PRT 220VAC A50
*SCD: 901406
SCSI CNTRL
*SCD: 901423
VGA VIDEO CARD
*SCD: 901436
*SCD: 901596
FOR FIELD SERVICE USE ONLY
THERMAL PRT
*ASM: 881217
*ASM: 881218
VCR
*ASM: 880812, NTSC, 115VAC
*ASM: 880813, PAL, 220VAC
REMOTE
MODEM
*ASM: 880811
*ASM: 880648
*ASM: 880650
OEC MEDICAL SYSTEMS, INC.
SIZE D
DWG NO. 00-878981
REV F
SCALE: NONE
SHEET 2 OF 4





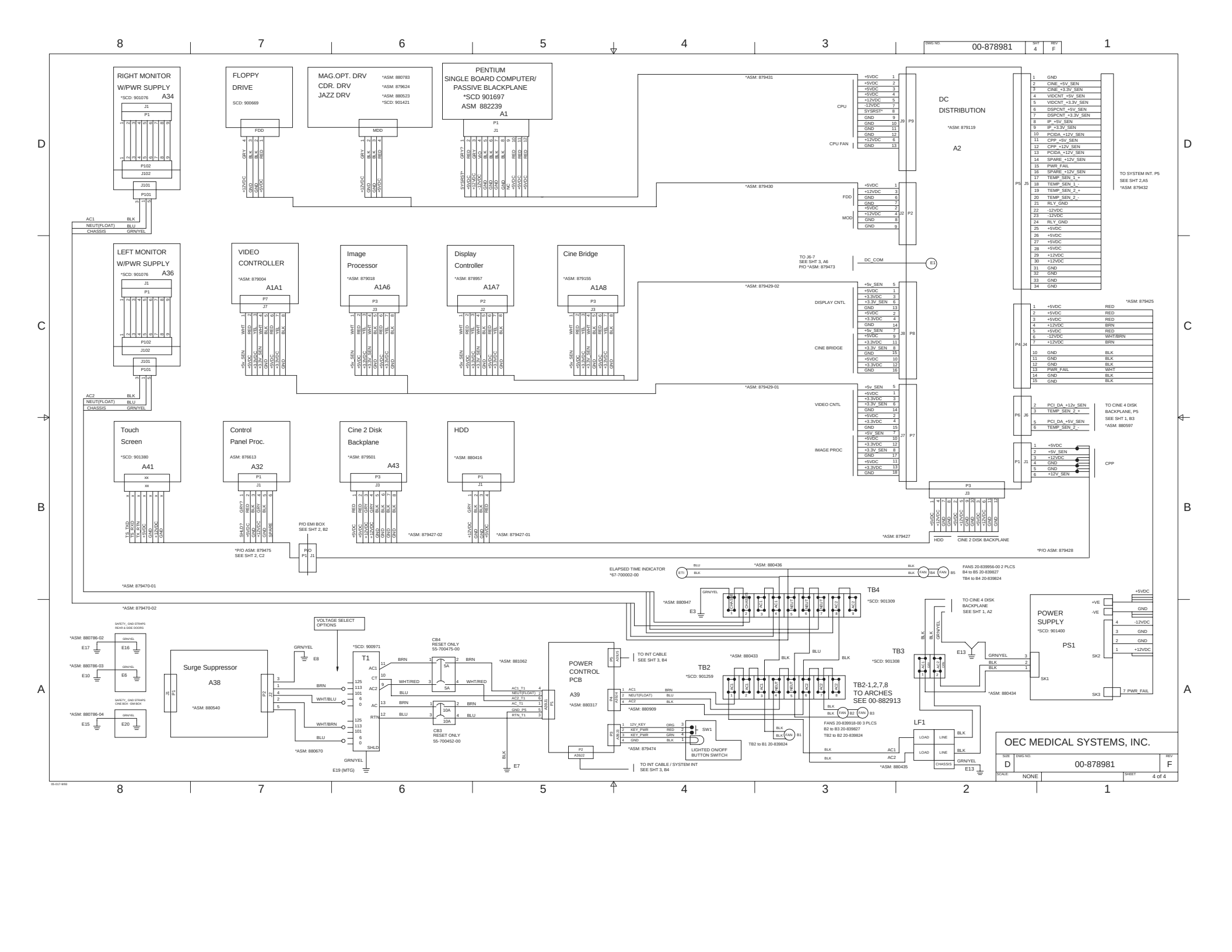


OEC MEDICAL SYSTEMS, INC.

SIZE	DWG NO.	REV
D	00-878981	F

SCALE: NONE SHEET 3 of 4

05-017-9/93


RIGHT MONITOR W/PWR SUPPLY
*SCD: 901076
A34
FLOPPY DRIVE
SCD: 900669
MAG.OPT. DRV
CDR. DRV
JAZZ DRV
*ASM: 880783
*ASM: 879624
*ASM: 880523
*SCD: 901421
PENTIUM SINGLE BOARD COMPUTER/ PASSIVE BLACKPLANE
*SCD 901697
ASM 882239
A1
*ASM: 879431
CPU
CPU FAN
DC DISTRIBUTION
*ASM: 879119
A2
*ASM: 879430
FDD
MOD
TO SYSTEM INT. P5
SEE SHT 2,A5
*ASM: 879432
LEFT MONITOR W/PWR SUPPLY
*SCD: 901076
A36
VIDEO CONTROLLER
*ASM: 879004
A1A1
Image Processor
*ASM: 879018
A1A6
Display Controller
*ASM: 878957
A1A7
Cine Bridge
*ASM: 879155
A1A8
TO J6-7
SEE SHT 3, A6
P/O *ASM: 879473
DC_COM
*ASM: 879429-02
DISPLAY CNTL
CINE BRIDGE
*ASM: 879429-01
VIDEO CNTL
IMAGE PROC
*ASM: 879425
TO CINE 4 DISK BACKPLANE, P5
SEE SHT 1, B3
*ASM: 880597
Touch Screen
*SCD: 901380
A41
Control Panel Proc.
ASM: 876613
A32
Cine 2 Disk Backplane
*ASM: 879501
A43
HDD
*ASM: 880416
P/O EMI BOX
SEE SHT 2, B2
*P/O ASM: 879475
SEE SHT 2, C2
*ASM: 879427-02
*ASM: 879427-01
*ASM: 879427
HDD
CINE 2 DISK BACKPLANE
*P/O ASM: 879428
CPP
*ASM: 879470-01
*ASM: 879470-02
ELAPSED TIME INDICATOR
*67-700002-00
*ASM: 880436
FANS 20-839956-00 2 PLCS
B4 to B5 20-839827
TB4 to B4 20-839824
*ASM: 880947
TB4
*SCD: 901309
TO CINE 4 DISK BACKPLANE
SEE SHT 1, A2
POWER SUPPLY
*SCD: 901400
PS1
+VE
-VE
+5VDC
GND
-12VDC
GND
+12VDC
7 PWR_FAIL
SK1
SK2
SK3
*ASM: 880786-02
*ASM: 880786-03
*ASM: 880786-04
Surge Suppressor
A38
*ASM: 880540
VOLTAGE SELECT OPTIONS
*SCD: 900971
T1
CB4
RESET ONLY
55-700475-00
*ASM: 881062
CB3
RESET ONLY
55-700452-00
*ASM: 880670
POWER CONTROL PCB
A39
*ASM: 880317
TO INT CABLE
SEE SHT 3, B4
TB2
*SCD: 901259
*ASM: 880433
*ASM: 880909
*ASM: 879474
SW1
LIGHTED ON/OFF BUTTON SWITCH
TO INT CABLE / SYSTEM INT
SEE SHT 3, B4
TB3
*SCD: 901308
*ASM: 880434
TB2-1,2,7,8
TO ARCHES
SEE 00-882913
FANS 20-839918-00 3 PLCS
B2 to B3 20-839827
TB2 to B2 20-839824
TB2 to B1 20-839824
LF1
*ASM: 880435
OEC MEDICAL SYSTEMS, INC.
00-878981
SCALE: NONE
SHEET 4 of 4

SYNC GENERATOR

DWG NO.	SHT	REV
00-879002	1	B6

(M) ENGIN. REV. 3.3 REVISIONS — EDR 01346

REV	DESCRIPTION	DATE	APPROVED
A	RELEASE TO MFG PER ECO AY96	3-26-98	C. BALL
A1	REVISED PER ECO BG67	6-30-98	C. BALL
A2	REVISED PER ECO BK20	9-01-98	C. BALL
B	REVISED PER ECO BP01	1-22-98	C. BALL
B1	REVISED PER ECO CA47	5-18-99	C. BALL
B2	REVISED PER ECO CC10	7-13-99	C. BALL
B3	REVISED PER ECO CF62	11-10-99	C. BALL
B4	REVISED PER ECO CJ58	2-24-00	C. BALL
B5	REVISED PER ECO CK28	4-24-00	M. SARGENT
B6	REVISED PER ECO CK91		

SIGNAL TEST POINT COLORS ARE WHITE

TEST OUTPUTS

FIRST FPGA IN CONFIGURATION SERIAL PATH

-01 SHOWN

DRAWING
LAST_MODIFIED=Mon Apr 24 16:28:00 2000
ACTIVE_BOMS=-22,-25

ITEM	QTY.	PART OR IDENT NO.	DESCRIPTION

PARTS LIST

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		CONTRACT NO.		APPROVED	DATE
		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS: +/- DECIMALS: .XX+/- .XXX+/- ANGLES: +/-	MATERIAL	DRAWN ART MICHAELSON	12/21/97
00-879004	9800		FINISH	CHECKED MARC UHREY	2/22/98
NEXT ASSEMBLY	USED ON			ENGINEERING ART MICHAELSON	2/22/98
APPLICATION		DO NOT SCALE DRAWING		APPROVED	

OEC MEDICAL SYSTEMS, INC.

DWG TITLE: SCHEM, VIDEO CONTROL

SIZE D | DWG NO. 00-879002 | REV B6

SCALE: | SHEET 1 OF 16

05-016-9/93

TEST PORT FOR DIGITIZED DATA

HORIZONTAL ANTI-VIGNETTING

VERTICAL ANTI-VIGNETTING

U58 +2.5V REFERENCE

TO SYSTEMS INTERFACE PCB

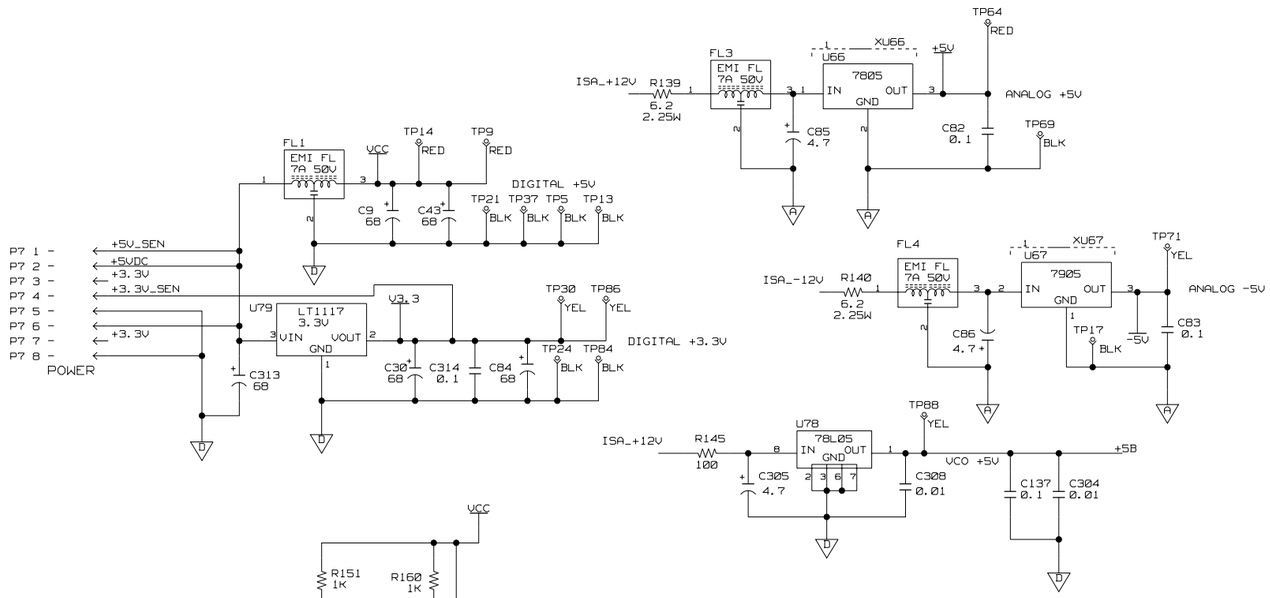
TO IMAGE PROCESSOR

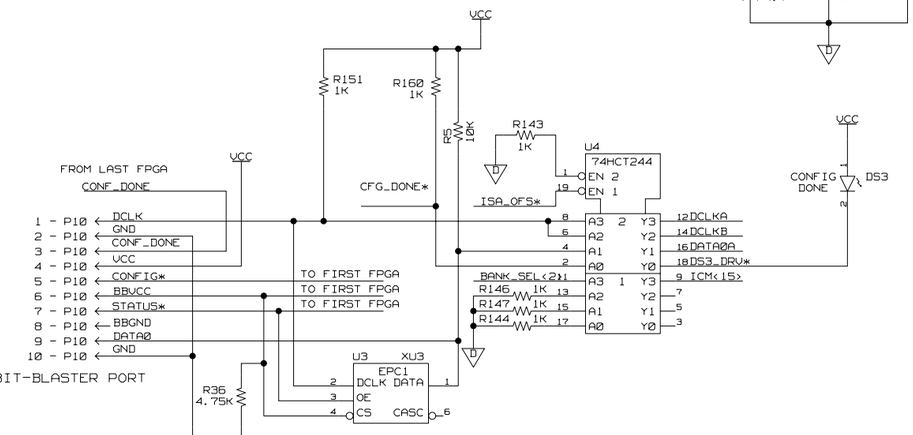
JUMPER P12-39 TO P12-40 TO DISABLE A/D LATCHES (U44 & U45) FOR TESTING.

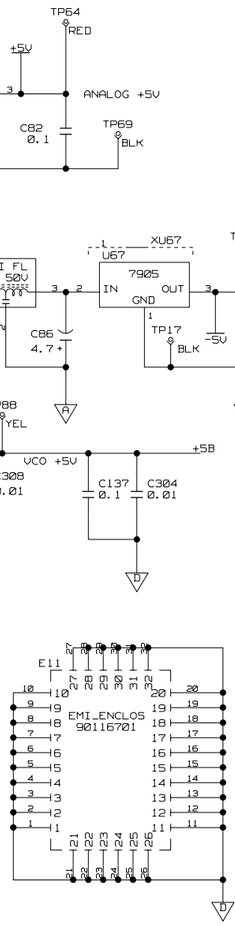
DIGITIZED DATA TO CRCT PLD

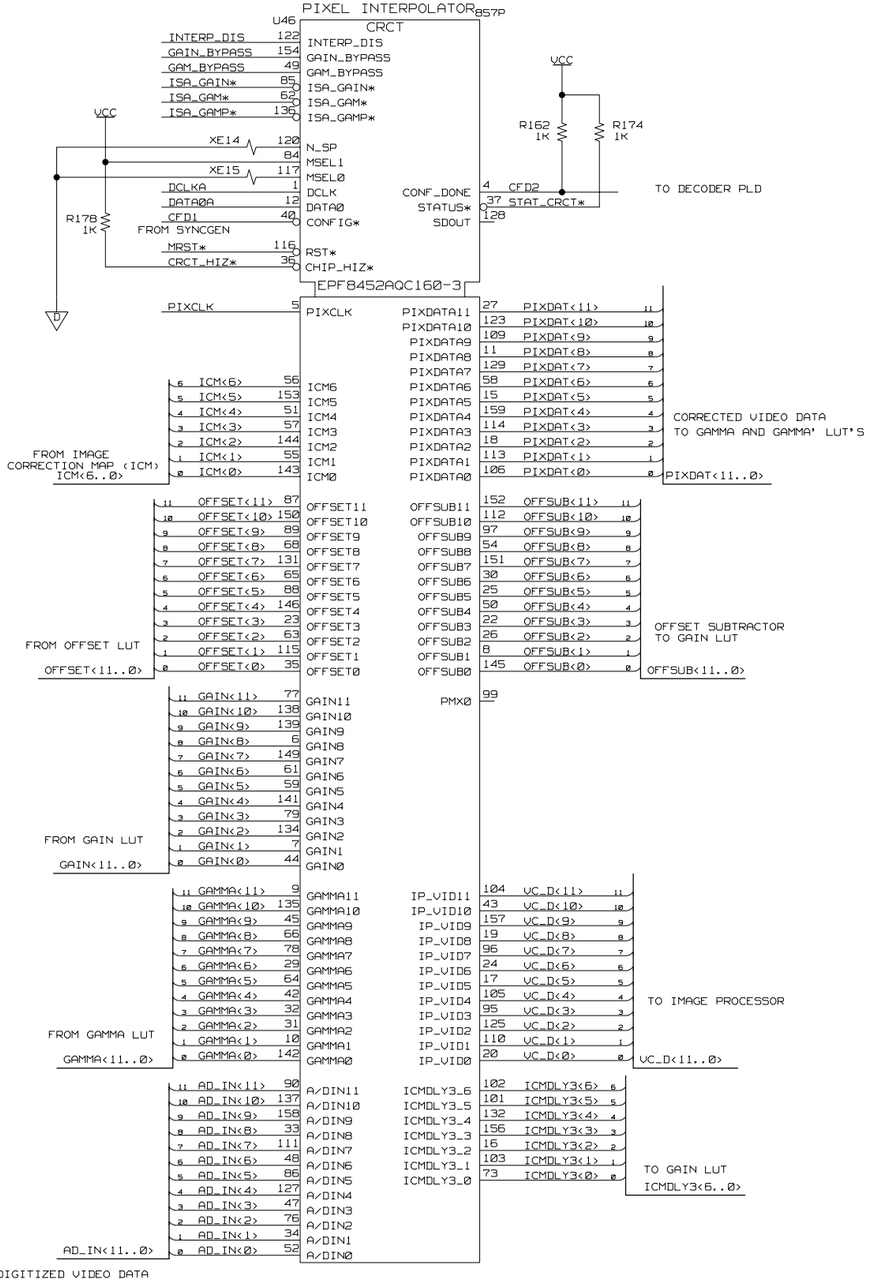
NOTE: B1 IS MSB, B12 IS LSB ON OUTPUT OF ADS800.

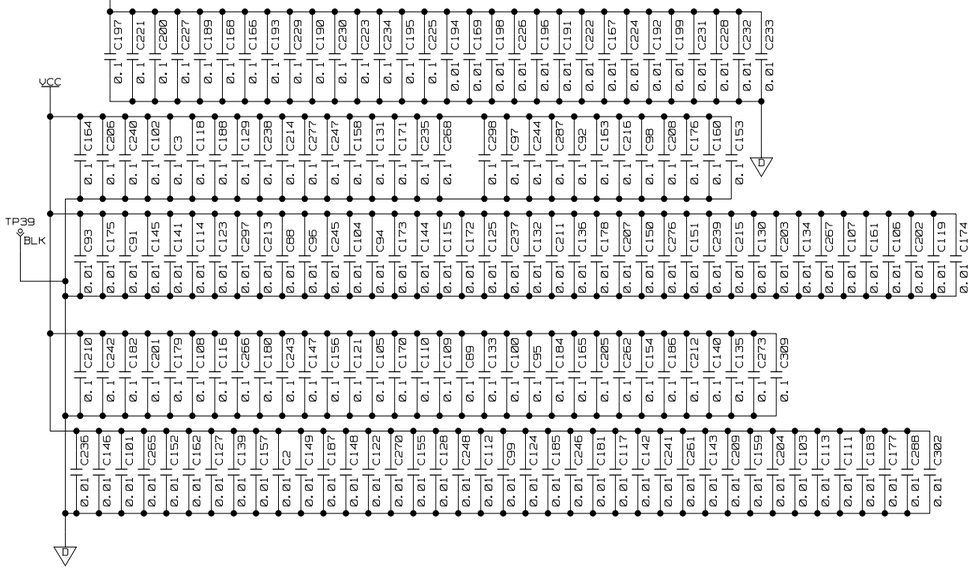
TO I.P.











DRAWING
LAST_MODIFIED=Mon Apr 24 12:33:02 2000

OEC MEDICAL SYSTEMS, INC.			
SIZE D	DWG NO. 00-879002		REV B6
SCALE:		SHEET 3 OF 16	

05-017-9/93

ISA BUS INTERFACE EDGE CONNECTOR

P1 - A1 ← IOCHK*
P1 - A2 ← SD<7>
P1 - A3 ← SD<6>
P1 - A4 ← SD<5>
P1 - A5 ← SD<4>
P1 - A6 ← SD<3>
P1 - A7 ← SD<2>
P1 - A8 ← SD<1>
P1 - A9 ← SD<0>
P1 -A10 ← IOCHRDY
P1 -A11 ← AEN
P1 -A12 ← SA<19>
P1 -A13 ← SA<18>
P1 -A14 ← SA<17>
P1 -A15 ← SA<16>
P1 -A16 ← SA<15>
P1 -A17 ← SA<14>
P1 -A18 ← SA<13>
P1 -A19 ← SA<12>
P1 -A20 ← SA<11>
P1 -A21 ← SA<10>
P1 -A22 ← SA<9>
P1 -A23 ← SA<8>
P1 -A24 ← SA<7>
P1 -A25 ← SA<6>
P1 -A26 ← SA<5>
P1 -A27 ← SA<4>
P1 -A28 ← SA<3>
P1 -A29 ← SA<2>
P1 -A30 ← SA<1>
P1 -A31 ← SA<0>

P1 - B1 ← ISA_GND
P1 - B2 ← ISARESET
P1 - B3 ←
P1 - B4 ← IRQ9
P1 - B5 ← ISA_-5V
P1 - B6 ← DRQ2
P1 - B7 ← ISA_-12V
P1 - B8 ← SRDY*
P1 - B9 ← ISA_+12V
P1 -B10 ← ISA_GND
P1 -B11 ← SMEMW*
P1 -B12 ← SMEMR*
P1 -B13 ← IOW*
P1 -B14 ← IOR*
P1 -B15 ← DACK3*
P1 -B16 ← DRQ3
P1 -B17 ← DACK1*
P1 -B18 ← DRQ1
P1 -B19 ← REFRESH*
P1 -B20 ← SYSCLK
P1 -B21 ← IRQ7
P1 -B22 ← IRQ6
P1 -B23 ← IRQ5
P1 -B24 ← IRQ4
P1 -B25 ← IRQ3
P1 -B26 ← DACK2*
P1 -B27 ← TC
P1 -B28 ← BALE
P1 -B29 ←
P1 -B30 ← OSC
P1 -B31 ← ISA_GND

C301 100P

P2 - C1 ← SBHE*
P2 - C2 ← LA<23>
P2 - C3 ← LA<22>
P2 - C4 ← LA<21>
P2 - C5 ← LA<20>
P2 - C6 ← LA19
P2 - C7 ← LA18
P2 - C8 ← LA17
P2 - C9 ← MEMR*
P2 -C10 ← MEMW*
P2 -C11 ← SD<8>
P2 -C12 ← SD<9>
P2 -C13 ← SD<10>
P2 -C14 ← SD<11>
P2 -C15 ← SD<12>
P2 -C16 ← SD<13>
P2 -C17 ← SD<14>
P2 -C18 ← SD<15>

P2 - D1 ← MEMCS16*
P2 - D2 ← IOCH16*
P2 - D3 ← IRQ10
P2 - D4 ← IRQ11
P2 - D5 ← IRQ12
P2 - D6 ← IRQ15
P2 - D7 ← IRQ14
P2 - D8 ← DACK0*
P2 - D9 ← DRQ0
P2 -D10 ← DACK5*
P2 -D11 ← DRQ5
P2 -D12 ← DACK6*
P2 -D13 ← DRQ6
P2 -D14 ← DACK7*
P2 -D15 ← DRQ7
P2 -D16 ←
P2 -D17 ← MASTER*
P2 -D18 ← ISA_GND

TP85 RED
TP66 BLK
C87 68
+5VMB

50 mil trace required on pcb to connect gnd's together.

ISA ADDRESS BUFFERS

U72 74HCT244
U75 74HCT244
U74 74HCT244
U73 74HCT244
EN 2, EN 1, VCC, A3 2 Y3, A2 Y2, A1 Y1, A0 Y0, A3 1 Y3, A2 Y2, A1 Y1, A0 Y0

R187 1K
R186 1K
R183 1K
R184 1K
R185 1K
+5VMB
C286 0.01
C283 0.01
C284 0.01
C285 0.01
TP74 TP73 TP82 TP76 TP77 TP45 TP46

SLAV_SYNC*
AEN 6
ISARESET 4
BALE 2
LA<23> 11
LA<22> 13
LA<21> 15
LA<20> 17

IOR* 8
IOW* 6
SMEMR* 4
SMEMW* 2

SA<19> 11
SA<18> 13
SA<17> 15
SA<16> 17
SA<15> 8
SA<14> 6
SA<13> 4
SA<12> 2
SA<11> 11
SA<10> 13
SA<9> 15
SA<8> 17
SA<7> 8
SA<6> 6
SA<5> 4
SA<4> 2
SA<3> 11
SA<2> 13
SA<1> 15
SA<0> 17

BP_VSYNC* 12
ISA_AEN 14
ISA_RESET 16
ISA_BALE 18
ISA_LA<23> 9
ISA_LA<22> 7
ISA_LA<21> 5
ISA_LA<20> 3
ISA_IORD* 12
ISA_IOWR* 14
ISA_SMEMR* 16
ISA_SMEMW* 18
ISA_A<19> 9
ISA_A<18> 7
ISA_A<17> 5
ISA_A<16> 3
ISA_A<15> 12
ISA_A<14> 14
ISA_A<13> 16
ISA_A<12> 18
ISA_A<11> 9
ISA_A<10> 7
ISA_A<9> 5
ISA_A<8> 3
ISA_A<7> 12
ISA_A<6> 14
ISA_A<5> 16
ISA_A<4> 18
ISA_A<3> 9
ISA_A<2> 7
ISA_A<1> 5
ISA_A<0> 3

SA<19..0>
ISA_A<19..0>

JTAG TEST PORT

1 - P11 ← TDI
2 - P11 ← TMS
3 - P11 ← TCLK
4 - P11 ← TRST*
5 - P11 ←
6 - P11 ←
7 - P11 ←
8 - P11 ← TDO
9 - P11 ←
10 - P11 ←

ISA DATA BUFFERS

+5VMB
R142 1K
TP72 TP89
ISA_VIDCTRL*
VC_RD*
U70 74HCT245
U76 74HCT245
G3, 3 EN1 [BA], 3 EN2 [AB], VCC
C269 0.01
C282 0.01

SD<15> 9
SD<14> 8
SD<13> 7
SD<12> 6
SD<11> 5
SD<10> 4
SD<9> 3
SD<8> 2
SD<7> 9
SD<6> 8
SD<5> 7
SD<4> 6
SD<3> 5
SD<2> 4
SD<1> 3
SD<0> 2

ISA_D<15> 11
ISA_D<14> 12
ISA_D<13> 13
ISA_D<12> 14
ISA_D<11> 15
ISA_D<10> 16
ISA_D<9> 17
ISA_D<8> 18
ISA_D<7> 11
ISA_D<6> 12
ISA_D<5> 13
ISA_D<4> 14
ISA_D<3> 15
ISA_D<2> 16
ISA_D<1> 17
ISA_D<0> 18

SD<15..0>
ISA_D<15..0>

ISA ADDRESS DECODER

U65 381P DECODER
EPF8636AQC208-4

TDI 72
TMS 76
TCLK 74
TRST* 54
N_SP 207
MSEL1 49
MSEL0 4
DCLKB 158
DATA0A 147
CFD2 103
ISA_RESET 9
RST* 161
DEC_HIZ* 150
PIXCLK 7

+5VMB
+POWER
+IO_POWER
TDO 120 TDO1 TO ICM PLD
CONF_DONE 153 CFD3 TO ICM PLD
STATUS* 108 DEC_STAT*
SDOUT 198
MRST* 197 MRST*
TP58
R168 1K
R163 1K
VCC
XE16
XE17
R170 1K
R159 10K
E10
C120 0.01

10K RESISTORS INSTALLED
R180 10K
R171 10K
R165 10K
R164 10K
R165 75
R175 75
R176 75
R179 75
REF
REV<3> 129
REV<2> 166
REV<1> 168
REV<0> 22
R7_3
R7_2
R7_1
R7_0

ISA_BALE 162
ISA_AEN 65
ISA_SMEMW* 81
ISA_SMEMR* 77
ISA_IOWR* 145
ISA_IORD* 112
BALE
AEN*
SMEMWR*
SMEMRD*
IO_WR*
IO_RD*

VMSK_WREN 99
VMSK_WREN

TP79
PILOT_OK 88
CFG_DONE* 201
PHASE_LOCK 59
VSYNC* 84
R182 10K
R7_7
R7_6
R7_5
R7_4

ISA_LA<23> 48
ISA_LA<22> 203
ISA_LA<21> 57
ISA_LA<20> 202
ISA_A<19> 97
ISA_A<18> 95
ISA_A<17> 100
ISA_A<16> 62
ISA_A<15> 167
ISA_A<14> 98
ISA_A<13> 192
ISA_A<12> 83
ISA_A<11> 13
ISA_A<10> 15
ISA_A<9> 11
ISA_A<8> 196
ISA_A<7> 14
ISA_A<6> 142
ISA_A<5> 101
ISA_A<4> 194
ISA_A<3> 12
ISA_A<2> 61
ISA_A<1> 204
ISA_A<0> 45
LA23
LA22
LA21
LA20
ISA_A19
ISA_A18
ISA_A17
ISA_A16
ISA_A15
ISA_A14
ISA_A13
ISA_A12
ISA_A11
ISA_A10
ISA_A9
ISA_A8
ISA_A7
ISA_A6
ISA_A5
ISA_A4
ISA_A3
ISA_A2
ISA_A1
ISA_A0
ISA_A<19..0>

ISA_D<7> 63
ISA_D<6> 119
ISA_D<5> 118
ISA_D<4> 117
ISA_D<3> 92
ISA_D<2> 113
ISA_D<1> 174
ISA_D<0> 133
ISA_D7
ISA_D6
ISA_D5
ISA_D4
ISA_D3
ISA_D2
ISA_D1
ISA_D0
ISA_D<15..0>

R6_0 143 GAM_SEL<0>
R6_1 136 GAM_SEL<1>
R6_2 41 GAM_SEL<2>
R6_3 144 SPARE2
R6_4 148 GAMP_SEL<0>
R6_5 160 GAMP_SEL<1>
R6_6 40 GAMP_SEL<2>
R6_7 146 SPARE3
TP42
TP29
MEMCS16* 180 MEMCS16*
MEM_ACS 205 SRDY
ISA_VIDCTRL* 163 ISA_VIDCTRL*
VC_IO_DEC 58 VC_IO_DEC (NO CONNECT)
VC_RD* 172 VC_RD*
VC_IO_RD 176 VC_IO_RD
ISA_ICM* 29 ISA_ICM*
ICM_CE* 178 ICM_CE*
ISA_GAM* 10 ISA_GAM*
GAM_CE* 31 GAM_CE*
GAM_WR* 181 GAM_WR*
GAM_OE* 8 GAM_OE*
ISA_GAMP* 179 ISA_GAMP*
GAMP_CE* 184 GAMP_CE*
GAMP_WR* 93 GAMP_WR*
GAMP_OE* 152 GAMP_OE*
ISA_VMSK* 80 ISA_VMSK*
VMSK_CE* 75 VMSK_CE*
VMSK_WR* 86 VMSK_WR*
VMSK_OE* 169 VMSK_OE*
ISA_GAIN* 195 ISA_GAIN*
GAIN_CE* 39 GAIN_CE*
GAIN_WR* 56 GAIN_WR*
GAIN_OE* 199 GAIN_OE*
ISA_OFS* 64 ISA_OFS*
OFS_CE* 28 OFS_CE*
OFS_WR* 79 OFS_WR*
OFS_OE* 183 OFS_OE*

R0_0 94 BANK_SEL<0>
R0_1 30 BANK_SEL<1>
R0_2 38 BANK_SEL<2>
R0_3 90 BANK_SEL<3>
R0_4 42 BANK_SEL<4>
R0_5 43 BANK_SEL<5>
R0_6 170 BANK_SEL<6> (NO CONNECT)
R0_7 24 BANK_SEL<7> (NO CONNECT)
R1_0 149 RST_ACC
R1_1 87 RST_PEAK
R1_2 70 RST_FLTR
R1_3 189 AUTO_RST_EN
R1_4 175 INTERP_DIS
R1_5 177 RECURSEL
R1_6 191 RECURS_BYPASS
R1_7 188 VLI_EN_ALL
DAC_WR* 66 DAC_WR*
DAC_LCH* 68 DAC_LCH*
R2_0 23 VMSK_BANK0
R2_1 173 VMSK_BANK1
R2_2 190 VMSK_BANK2
R2_3 71 VMSK_BANK3
R2_4 116 SPARE1
R2_5 185 GAIN_BYPASS
R2_6 44 GAM_BYPASS
R2_7 135 AVG_BYPASS
TP41
R3_0 186 CAM_GAIN<0>
R3_1 73 CAM_GAIN<1>
R3_2 115 CAM_GAIN<2>
R3_3 187 CAM_GAIN<3>
R3_4 114 CAM_GAIN<4>
R3_5 128 CAM_GAIN<5>
R3_6 37 CAM_GAIN<6>
R3_7 21 CAM_GAIN<7>
TP40 TP59 TP78 TP80 TP83 TP28 TP36 TP22
R4_0 134 BP_EN*
R4_1 165 VIDSEL0
R4_2 69 VIDSEL1
R4_3 127 MAGSEL0
R4_4 85 MAGSEL1
R4_5 82 CLKSEL0
R4_6 89 CLKSEL1
R4_7 126 CLKSEL2

REGISTERS AT I/O ADDRESSES 220H TO 237H
CLKSEL2=0 SELECTS 25FPS
CLKSEL2=1 SELECTS 30FPS

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LAST_MODIFIED=Mon Apr 24 12:33:04 2000

OEC MEDICAL SYSTEMS, INC.

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IMAGE CORRECTION MAP CONTROLLER PLD

U69 388P

ICM

ICM_CE* 68 ISA_BALE 69 ISA_SMEMR* 6 ISA_SMEMW* 73 ISA_ICM* 72 ISA_OFS* 129 VLI_IOCHRQ* 62 TDO1 55 TMS 59 TCLK 57 TRST* 40

ICM_CE* ISA_BALE ISA_RD* ISA_WR* ISA_ICM* ISA_OFS* VLI_IOCHRQ* TDI TMS TCLK TRST*

(I/O = 3.3V)

ICM_IOCHRDY → 147 ICM_RDY → TO SYNCGEN PLD

TDO → 95 TDO2 → TO VLI PLD

CONF_DONE 118 CFD4

STATUS* 83 STAT_ICM*

SDOUT 152 TO VLI PLD

V3.3 R141 1K

VCC R193 1K

XE18 1 38 XE19 3

N_SP MSEL1 MSEL0 DCLKA 120 DATA0A 113 CFD3 81 MRST* 87 ICM_HIZ* 35

DCLK DATA0 CONFIG* RST* CHIP_HIZ*

VCC R172 1K R189 1K

EPF8636AQC160-3

TP67 TP65 TP53 TP54 TP81

PIXCLK 116 HSYNC* 7 VSYNC* 115 CLKSEL2 142

PIXCLK HSYNC* VSYNC* CLKSEL2

RAM_CAS* 76 ICM_CAS*
RAM_RAS* 143 ICM_RAS*
RAM_WE* 56 ICM_WR*
RAM_CS* 58 ICM_CS*
RAM_CKE 130 ICM_CKE
RAM_DQMH 14 ICM_UDQM
RAM_DQML 13 ICM_LDQM

RAM_DO<15..0>

RAM_DO15 79 15
RAM_DO14 28 14
RAM_DO13 30 13
RAM_DO12 20 12
RAM_DO11 22 11
RAM_DO10 99 10
RAM_DO9 101 9
RAM_DO8 105 8
RAM_DO7 77 7
RAM_DO6 125 6
RAM_DO5 122 5
RAM_DO4 74 4
RAM_DO3 23 3
RAM_DO2 98 2
RAM_DO1 104 1
RAM_DO0 91 0

IMAGE CORRECTION MAP (ICM)

U68 SDRAM_1MX16 SPEED=12_NS

PIXCLK 35 → CLK
CKE 34
CS 18
RAS 17
CAS 16
WE 15
UDQM 36
LDQM 14

DQ15 48 RAM_DO<15> 15
DQ14 47 RAM_DO<14> 14
DQ13 46 RAM_DO<13> 13
DQ12 45 RAM_DO<12> 12
DQ11 44 RAM_DO<11> 11
DQ10 43 RAM_DO<10> 10
DQ09 42 RAM_DO<9> 9
DQ08 39 RAM_DO<8> 8
DQ07 38 RAM_DO<7> 7
DQ06 37 RAM_DO<6> 6
DQ05 33 RAM_DO<5> 5
DQ04 32 RAM_DO<4> 4
DQ03 31 RAM_DO<3> 3
DQ02 29 RAM_DO<2> 2
DQ01 28 RAM_DO<1> 1
DQ00 27 RAM_DO<0> 0

A11 19 RAM_ADR11
A10 20 RAM_ADR10
A09 32 RAM_ADR9
A08 31 RAM_ADR8
A07 30 RAM_ADR7
A06 29 RAM_ADR6
A05 28 RAM_ADR5
A04 27 RAM_ADR4
A03 24 RAM_ADR3
A02 23 RAM_ADR2
A01 22 RAM_ADR1
A00 21 RAM_ADR0

ISA INTERFACE (VCC = 3.3V)

U71 74LCX16245

OE2 25
DIR2 [BA] DIR2 [AB] ISA_SMEMR* 24 ICM_CE* 48 OE1 1
DIR1 [AB] DIR1 [BA]

ISA_D<15> 26 ISA_D<14> 27 ISA_D<13> 29 ISA_D<12> 30 ISA_D<11> 32 ISA_D<10> 33 ISA_D<9> 35 ISA_D<8> 36 ISA_D<7> 37 ISA_D<6> 38 ISA_D<5> 40 ISA_D<4> 41 ISA_D<3> 43 ISA_D<2> 44 ISA_D<1> 46 ISA_D<0> 47

A7 A6 A5 A4 A3 A2 A1 A0 — B7 B6 B5 B4 B3 B2 B1 B0

23 ICM_D<15> 22 ICM_D<14> 20 ICM_D<13> 19 ICM_D<12> 17 ICM_D<11> 16 ICM_D<10> 14 ICM_D<9> 13 ICM_D<8> 12 ICM_D<7> 11 ICM_D<6> 9 ICM_D<5> 8 ICM_D<4> 6 ICM_D<3> 5 ICM_D<2> 3 ICM_D<1> 2 ICM_D<0>

ISA_D<15..0>

ISA_DB15 ISA_DB14 ISA_DB13 ISA_DB12 ISA_DB11 ISA_DB10 ISA_DB9 ISA_DB8 ISA_DB7 ISA_DB6 ISA_DB5 ISA_DB4 ISA_DB3 ISA_DB2 ISA_DB1 ISA_DB0

BUFFER

BANK_SEL<5> 66 BANK_SEL<4> 128 BANK_SEL<3> 134 BANK_SEL<2> 11 BANK_SEL<1> 71 BANK_SEL<0> 31 ISA_A<14> 123 ISA_A<13> 124 ISA_A<12> 135 ISA_A<11> 94 ISA_A<10> 8 ISA_A<9> 9 ISA_A<8> 78 ISA_A<7> 132 ISA_A<6> 29 ISA_A<5> 133 ISA_A<4> 67 ISA_A<3> 65 ISA_A<2> 33 ISA_A<1> 27

ADD19 ADD18 ADD17 ADD16 ADD15 ADD14 ADD13 ADD12 ADD11 ADD10 ADD9 ADD8 ADD7 ADD6 ADD5 ADD4 ADD3 ADD2 ADD1 ADD0

ISA_A<19..0>

LUT_ADD15 LUT_ADD14 LUT_ADD13 LUT_ADD12 LUT_ADD11 LUT_ADD10 LUT_ADD9 LUT_ADD8 LUT_ADD7 LUT_ADD6 LUT_ADD5 LUT_ADD4 LUT_ADD3 LUT_ADD2 LUT_ADD1 LUT_ADD0

103 ICM<15> 43 ICM<14> 44 ICM<13> 112 ICM<12> 46 ICM<11> 10 ICM<10> 110 ICM<9> 92 ICM<8> 111 ICM<7> 108 ICM<6> 89 ICM<5> 114 ICM<4> 32 ICM<3> 109 ICM<2> 88 ICM<1> 157 ICM<0>

TO LUT ADDRESS LINES

ICM<15..0>

OFFSET-CORRECTED VIDEO DATA FROM CRCT PLD

OFFSUB<11..3>

ISA INTERFACE

U36 74HCT244

ISA_GAIN* 1 19

BANK_SEL<1> 8 BANK_SEL<0> 6 ISA_A<14> 4 ISA_A<13> 2 ISA_A<12> 11 ISA_A<11> 13 ISA_A<10> 15 ISA_A<9> 17

A3 A2 A1 A0 — Y3 Y2 Y1 Y0

OFFSUB<11> 11 OFFSUB<10> 10 OFFSUB<9> 9 OFFSUB<8> 8 OFFSUB<7> 7 OFFSUB<6> 6 OFFSUB<5> 5 OFFSUB<4> 4

U29 74HCT244

ISA_GAIN* 1 19

ISA_A<8> 8 ISA_A<7> 6 ISA_A<6> 4 ISA_A<5> 2 ISA_A<4> 11 ISA_A<3> 13 ISA_A<2> 15 ISA_A<1> 17

OFFSUB<3> 3 ICMDLY3<6> 6 ICMDLY3<5> 5 ICMDLY3<4> 4 ICMDLY3<3> 3 ICMDLY3<2> 2 ICMDLY3<1> 1 ICMDLY3<0> 0

ICMDLY3<6..0>

GAIN LOOK-UP TABLE (LUT) (ILLUMINATED CORRECTION)

U28 TCS51664 SPEED=15_NS

XE12 40 XE13 39

UB LB CS WR RD

GAIN_CE* 6 GAIN_WR* 17 GAIN_OE* 41

64K X16 SRAM

OFFSUB<11> 18 OFFSUB<10> 19 OFFSUB<9> 20 OFFSUB<8> 21 OFFSUB<7> 24 OFFSUB<6> 25 OFFSUB<5> 26 OFFSUB<4> 27 OFFSUB<3> 42 ICMDLY3<6> 6 ICMDLY3<5> 5 ICMDLY3<4> 4 ICMDLY3<3> 3 ICMDLY3<2> 2 ICMDLY3<1> 1 ICMDLY3<0> 0

A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0

D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0

GAIN<15> 38 GAIN<14> 37 GAIN<13> 36 GAIN<12> 35 GAIN<11> 32 GAIN<10> 31 GAIN<9> 30 GAIN<8> 29 GAIN<7> 16 GAIN<6> 15 GAIN<5> 14 GAIN<4> 13 GAIN<3> 10 GAIN<2> 9 GAIN<1> 8 GAIN<0> 7

ISA INTERFACE

U37 74HCT245

G3 19 ISA_GAIN* 3 EN1 [BA] 3 EN2 [AB] 1 ISA_SMEMR*

B A

GAIN<15> 11 GAIN<14> 12 GAIN<13> 13 GAIN<12> 14 GAIN<11> 15 GAIN<10> 16 GAIN<9> 17 GAIN<8> 18

ISA_D<15> 15 ISA_D<14> 14 ISA_D<13> 13 ISA_D<12> 12 ISA_D<11> 11 ISA_D<10> 10 ISA_D<9> 9 ISA_D<8> 8

U27 74HCT245

G3 19 ISA_GAIN* 3 EN1 [BA] 3 EN2 [AB] 1 ISA_SMEMR*

GAIN<7> 11 GAIN<6> 12 GAIN<5> 13 GAIN<4> 14 GAIN<3> 15 GAIN<2> 16 GAIN<1> 17 GAIN<0> 18

ISA_D<7> 9 ISA_D<6> 8 ISA_D<5> 7 ISA_D<4> 6 ISA_D<3> 5 ISA_D<2> 4 ISA_D<1> 3 ISA_D<0> 2

GAIN<15..0>

ONLY 12 LSB'S USED

OFFSET LOOK-UP TABLE (LUT) (NON-ILLUMINATED CORRECTION)

ISA INTERFACE

VCC R161 1K

U48 PD431000

OFS_WR* 29 OFS_CE* 22 30 OFS_OE* 24

WE CS1 CS2 OE

ICM<15> 15 FROM U4 SHEET 3

ICM<15> 2 ICM<14> 31 ICM<13> 3 ICM<12> 28 ICM<11> 4 ICM<10> 25 ICM<9> 23 ICM<8> 26 ICM<7> 27

A16 A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0

I/O 7 I/O 6 I/O 5 I/O 4 I/O 3 I/O 2 I/O 1 I/O 0

OFFSET<15> 21 OFFSET<14> 20 OFFSET<13> 19 OFFSET<12> 18 OFFSET<11> 17 OFFSET<10> 16 OFFSET<9> 15 OFFSET<8> 14

128Kx8 SRAM

CAM_GAIN<7> 5 CAM_GAIN<6> 6 CAM_GAIN<5> 7 CAM_GAIN<4> 8 CAM_GAIN<3> 9 CAM_GAIN<2> 10 CAM_GAIN<1> 11 CAM_GAIN<0> 12

ISA INTERFACE

U63 74HCT245

G3 19 ISA_OFS* 3 EN1 [BA] 3 EN2 [AB] 1 ISA_SMEMR*

B A

OFFSET<15> 11 OFFSET<14> 12 OFFSET<13> 13 OFFSET<12> 14 OFFSET<11> 15 OFFSET<10> 16 OFFSET<9> 17 OFFSET<8> 18

ISA_D<15> 15 ISA_D<14> 14 ISA_D<13> 13 ISA_D<12> 12 ISA_D<11> 11 ISA_D<10> 10 ISA_D<9> 9 ISA_D<8> 8

ISA INTERFACE

U38 74HCT244

ISA_OFS* 1 19

BANK_SEL<1> 8 BANK_SEL<0> 6 ISA_A<14> 4 ISA_A<13> 2 ISA_A<12> 11 ISA_A<11> 13 ISA_A<10> 15 ISA_A<9> 17

A3 A2 A1 A0 — Y3 Y2 Y1 Y0

ICM<14> 12 ICM<13> 14 ICM<12> 16 ICM<11> 18 ICM<10> 9 ICM<9> 7 ICM<8> 5 ICM<7> 3

U49 74HCT244

ISA_OFS* 1 19

ISA_A<8> 8 ISA_A<7> 6 ISA_A<6> 4 ISA_A<5> 2 ISA_A<4> 11 ISA_A<3> 13 ISA_A<2> 15 ISA_A<1> 17

CAM_GAIN<7> 12 CAM_GAIN<6> 14 CAM_GAIN<5> 16 CAM_GAIN<4> 18 CAM_GAIN<3> 9 CAM_GAIN<2> 7 CAM_GAIN<1> 5 CAM_GAIN<0> 3

ISA_A<19..0>

U47 PD431000

OFS_WR* 29 OFS_CE* 22 30 OFS_OE* 24

WE CS1 CS2 OE

ICM<15> 2 ICM<14> 31 ICM<13> 3 ICM<12> 28 ICM<11> 4 ICM<10> 25 ICM<9> 23 ICM<8> 26 ICM<7> 27

A16 A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0

I/O 7 I/O 6 I/O 5 I/O 4 I/O 3 I/O 2 I/O 1 I/O 0

OFFSET<7> 21 OFFSET<6> 20 OFFSET<5> 19 OFFSET<4> 18 OFFSET<3> 17 OFFSET<2> 15 OFFSET<1> 14 OFFSET<0> 13

128Kx8 SRAM

CAM_GAIN<7> 5 CAM_GAIN<6> 6 CAM_GAIN<5> 7 CAM_GAIN<4> 8 CAM_GAIN<3> 9 CAM_GAIN<2> 10 CAM_GAIN<1> 11 CAM_GAIN<0> 12

FROM DECODER PLD

CAM_GAIN<7..0>

ICM<15..0>

ISA INTERFACE

U62 74HCT245

G3 19 ISA_OFS* 3 EN1 [BA] 3 EN2 [AB] 1 ISA_SMEMR*

B A

OFFSET<7> 11 OFFSET<6> 12 OFFSET<5> 13 OFFSET<4> 14 OFFSET<3> 15 OFFSET<2> 16 OFFSET<1> 17 OFFSET<0> 18

ISA_D<7> 9 ISA_D<6> 8 ISA_D<5> 7 ISA_D<4> 6 ISA_D<3> 5 ISA_D<2> 4 ISA_D<1> 3 ISA_D<0> 2

ISA_D<15..0>

ONLY 12 LSB'S USED

OFFSET<15..0>

TO CRCT FPLD

DRAWING

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OEC MEDICAL SYSTEMS, INC.

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VLI FUNCTIONS

GAMMA LOOK-UP TABLE (LUT)

U31 SRAM_32KX8 SPEED=15_NS
U40 SRAM_32KX8 SPEED=15_NS
U20 74HCT244
U19 74HCT244

ISA_A<19..0>

NOTE: A0 IS NOT USED BECAUSE OF 16-BIT ADDRESSING ON SOME RAMS.

IN VIDEO MODE, PIXDAT<11..0> IS DRIVEN BY THE CRCT FPGA AND IS A TRI-STATE 12-BIT BUS.

FROM CRCT PLD PIXDAT<11..0>

ISA INTERFACE

U30 74HCT245
U39 74HCT245

ISA_D<15..0>

NOTE: PIXDATA USABLE BITS ARE 11-0. ACTUAL DATA PATH WIDTH IS 12 BITS.

FROM GAMMA' LUT GAMP_D<7..0>

TO CRCT PLD GAMMA<15..0>

ISA BUS ISA_A<19..0>

ISA BUS ISA_D<15..0>

VLI

U64 354P

EPF8820AQC160-4

FROM VMSK_LUT VMSK_D<7..0>

LAST FPGA IN CONFIGURATION SERIAL PATH

GAMMA PRIME (GAMP) LUT

U12 SRAM_32KX8 SPEED=15_NS
U20 74HCT244
U11 74HCT244

NOTE: ONLY 10 MSB'S OF PIXEL DATA ARE REQUIRED FOR GAMMA'. THE 2 LSB'S HAVE BEEN INCLUDED TO FACILITATE HOOKUP.

PIXDAT<11..0>

GAMP_D<7..0>

ISA INTERFACE

U21 74HCT245

ISA_D<15..0>

VLI MASK (VMSK) LUT

U52 74HCT244
U51 74HCT244
U50 SRAM_32KX8 SPEED=15_NS

VMSK_A<15..0>

ISA INTERFACE

U53 74HCT245

VMSK_D<7..0>

ISA_D<15..0>

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OEC MEDICAL SYSTEMS, INC.

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REF DES	DEVICE	DGND	VCC	UNUSED
U18	EPF8636ALC84	5,26,47,68	17,38,59,80	36,50,51,72 76,77
U46	EPF8452AQC160	13,14,28,46,60, 75,93,107,108, 126,140,155	21,41,53,67,80, 100,121,133,147, 160	2,3,38,39,69-72 74,82,83,91,92, 94,98,118,119, 124,148
U64	EPF8820AQC160	12,13,34,35,51, 63,75,80,83,93, 103,115,126,131, 143,155	3,23,24,46,47,57, 69,79,92,104,114, 127,137,149,159, 160	4,6,8,10,11,20, 48,52-56,59,60, 64,67,68,96, 120,121,133,136 138,141,144-148 150-152,156-158
U65	EPF8363AQC208	19,20,46,47,60, 67,95,109,111, 124,151,154,171, 200	+5VMB: 5,6,32,33,55, 78,91,102,110, 137,138,159,182, 193,206	1-3,16-18,25-27, 34-36,48,50-53,57, 104-107,121-123, 130-132,139-141, 154-157,162, 202-204,208
U3	EPC1	5	7,8	6
U4,11,19,20,29,36, 38,49,51,52,72-75	74HCT244	10	20	
U21,27,30,37, 39,53,62,63,70,76	74HCT245	10	20	
U12	74LS123	8	16	6
U10	CY7B991	12,13,21,22, 28,32	2,8,9,16, 18,25	
U13,26	74F02	7	14	
U44,45	74F574	10	20	2,19 OF U44
U12,31,40,50	PDM4256LA	14	28	
U28	TC551664	12,34	11,33	
U47,48	PD431000	16	32	
U77	74HC14	14	7	
Y1	38.934MHZ	4	8	
Y2	33.990MHZ	4	8	

ANALOG

REF DES	DEVICE	DGND	+5V	AGND	-5V	VCC	UNUSED
U24	74F02		14	7			
U61	DACMAX505	7	22	3,6			
U42	ADS800	1.14	20,24	25,28		15,17	
U1,17,35	MAX9698		11		6		
U15,16	GS4881		8	4			
U23,34	DG411		13		4		
U5,7-9,41,56	MAX452		6		3		
U14,33	MAX454		12	3	4		
U25,57,60	LF412C		8		4		
U22	HFA1103		7		4		
U32	CLC520		14	11	8		
U54,55	EL4450		12	2	3		
U58	AD680		2	4			
U43,59	OP177		7		4		
U6	GS4981		8	4			1,3,5

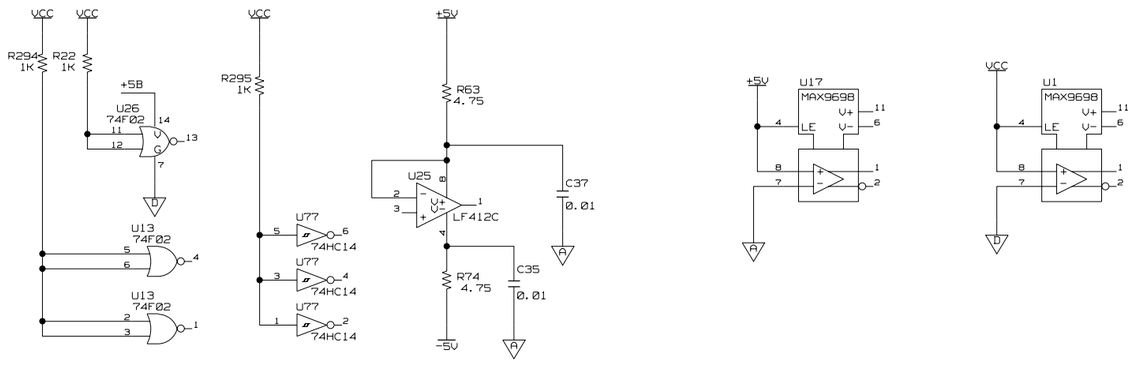
REFERENCE DESIGNATIONS

HIGHEST	UNUSED
U79	
R296	
C314	
L8	
CR7	
Q4	
DS3	
E12	
FL4	
P12	4
TP91	
XE21	
XU67	XU1,2,4-65
Y2	
T1	

REF DES	DEVICE	DGND	+5V	3.3V AGND	3.3V	UNUSED 3.3V	UNUSED UNUSED
U69	EPF8636AQC160	15,16,36, 37,48,61, 73,84,85, 86,97,117, 126,131,154	4,5,26, 85,106	+3.3V: 25, 41,60,70, 80,107,121, 140,149, 160			2,25,39,53, 54,82,107,119, 135,139,141, 144-146,149
U71	74LCX16245	4,10,15, 21,28, 34,39, 45		7,18,31, 42			
U68	SDRAM_1MX16	4,10,26, 41,47, 50		1,7,13, 25,38, 44			

00-879003-02 PCB, VIDEO CONTROL, ART/FAB, 9800
ASM_U3-25 OPT
00-881046-07 ASM, FW, U3, VID CTRL, 9800
00-879002-01 SCH, PCB, VIDEO CONTROL, 9800
00-879004-50 SPEC, PERF, VIDEO CONTROL PCB, 9800
00-901420-01 BRKT, PCI, RECT CUTOUT
00-901419-01 BRKT, ISA, DSUB CUTOUT
12-225104-04 SCR,SEMS SPR,PAN,TRX,4-40,1/4,SZC
SIZE=4
13-311104-00 NUT,HEX-LK-EXT-T,4-40,SST,NA,A-.250
SIZE=2
12-225104-05 SCR,SEMS SPR,PAN,TRX,4-40,5/16,SZC
SIZE=2
88-298900-00 CMPD,HS,BTL,20Z,250
ASM_U3-22 OPT
00-881745-01 FW ASM, U3, VID CTRL FS 9800
NOTE: 881745 FIRMWARE IS USED ON REV A5 OR EARLIER BOARDS ONLY.

UNUSED DEVICES



DRAWING
LAST_MODIFIED=Tue Apr 25 14:02:38 2000

OEC MEDICAL SYSTEMS, INC.

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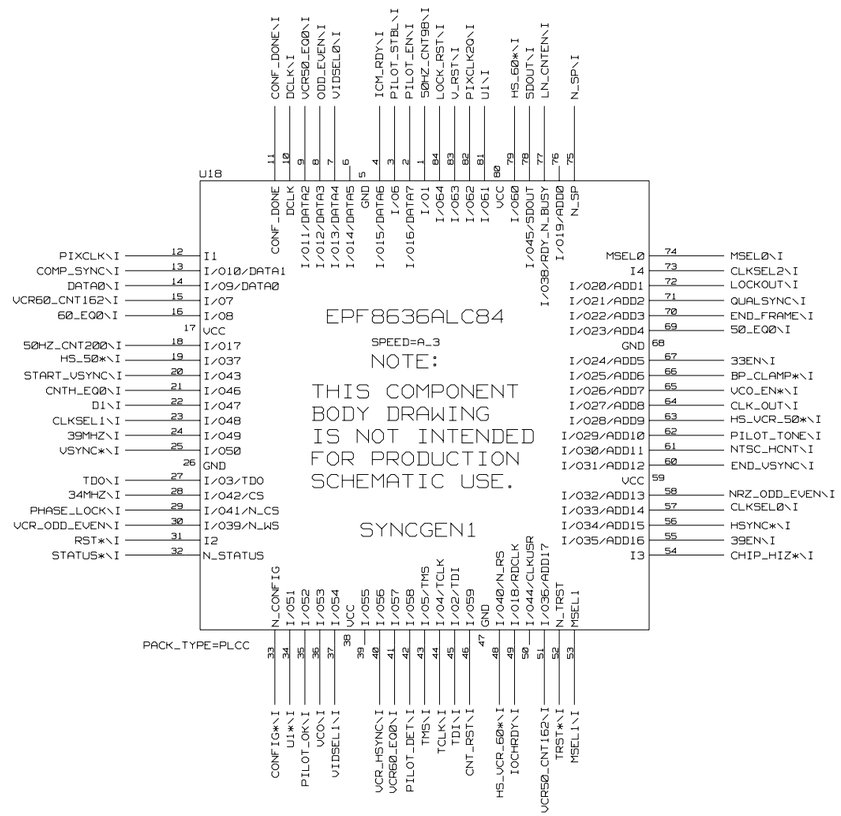

DRAWING
LAST_MODIFIED=Mon Apr 24 12:33:10 2000

OEC MEDICAL SYSTEMS, INC.

SIZE	DWG NO.	REV
D	00-879002	B6
SCALE:		SHEET 8 OF 16

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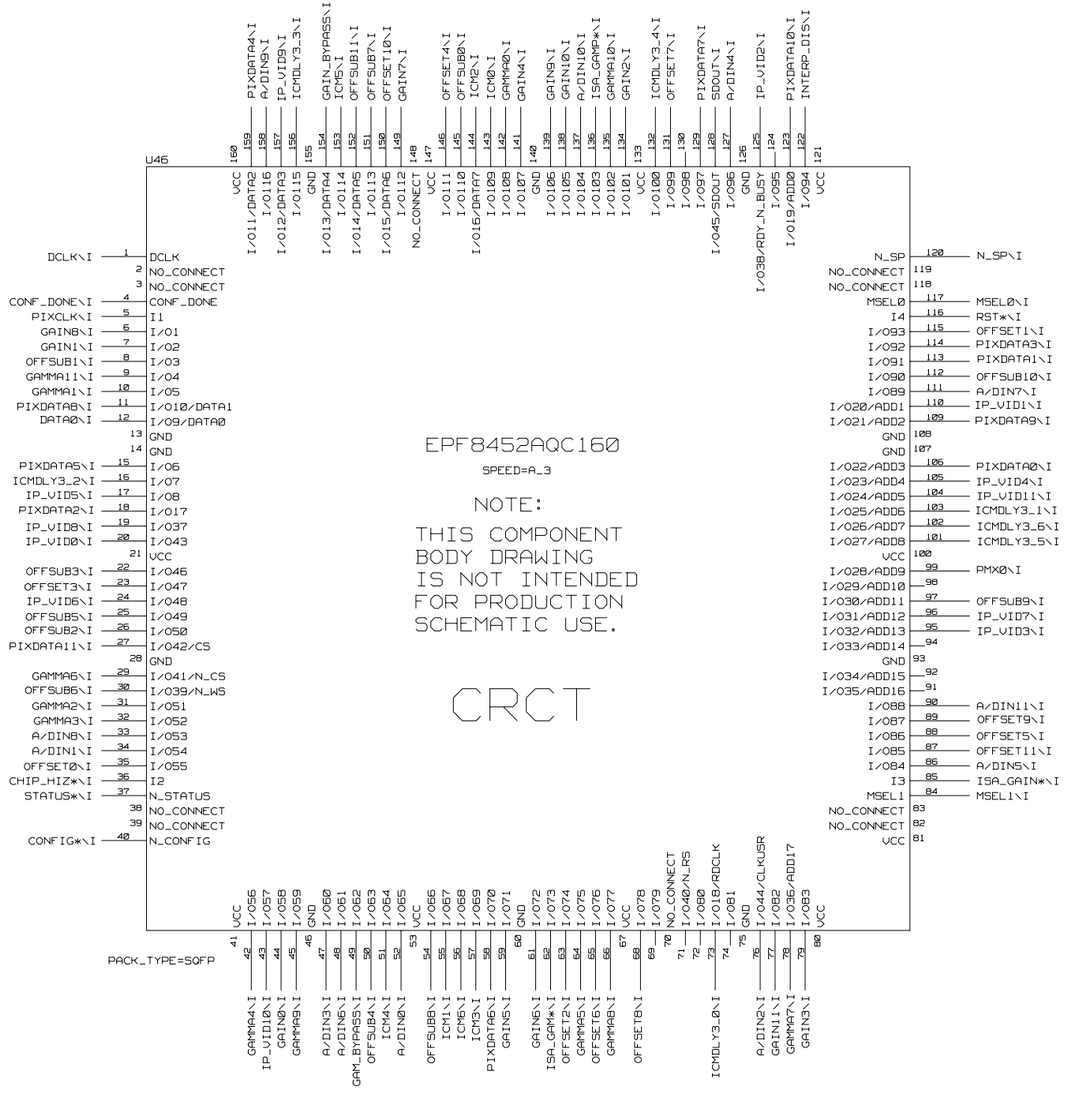

DRAWING
LAST_MODIFIED=Mon Apr 24 12:33:11 2000

OEC MEDICAL SYSTEMS, INC.

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D	00-879002	B6
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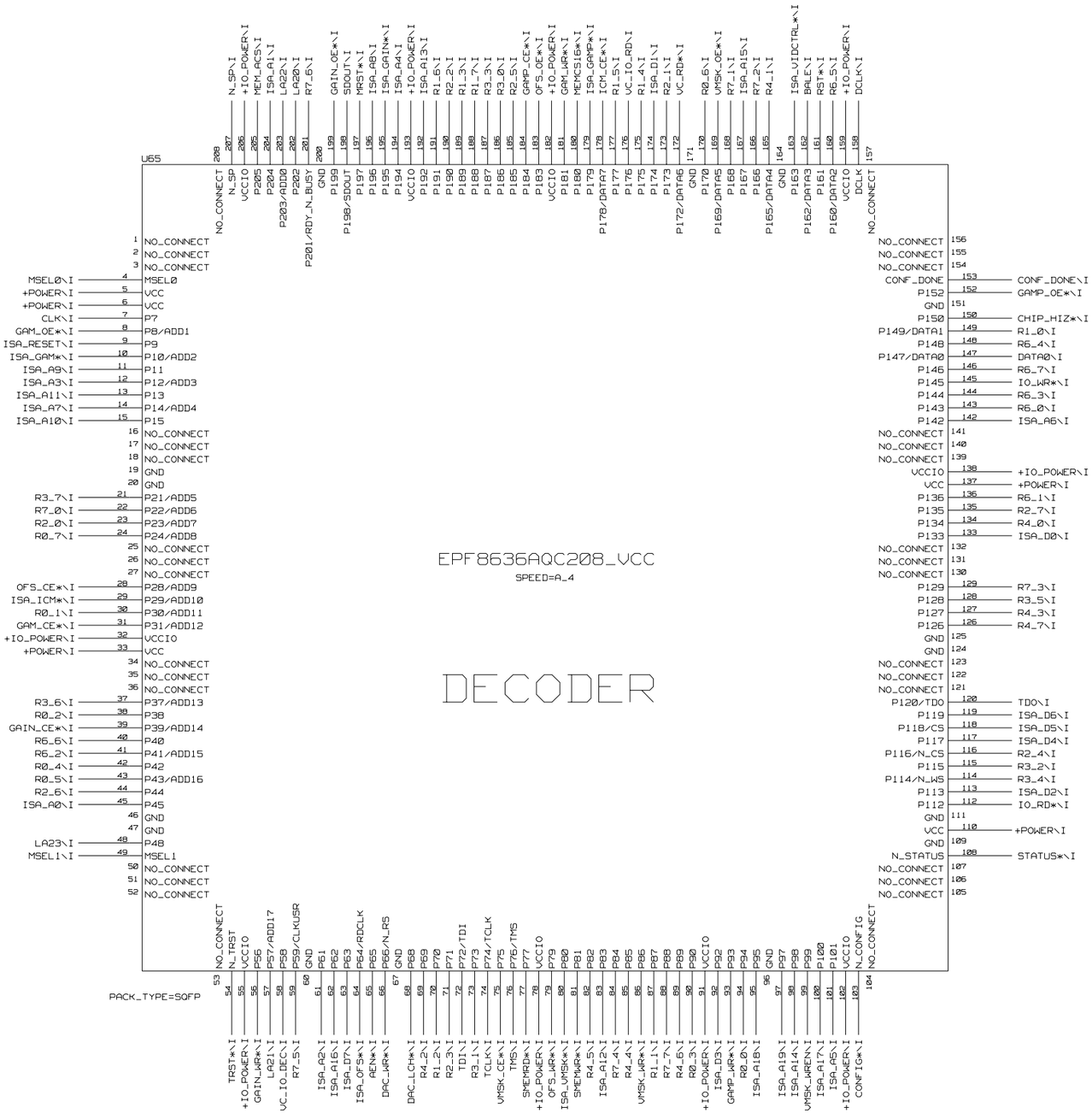

DRAWING
LAST_MODIFIED=Mon Apr 24 12:33:12 2000

OEC MEDICAL SYSTEMS, INC.

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SCALE:		SHEET 10 OF 16

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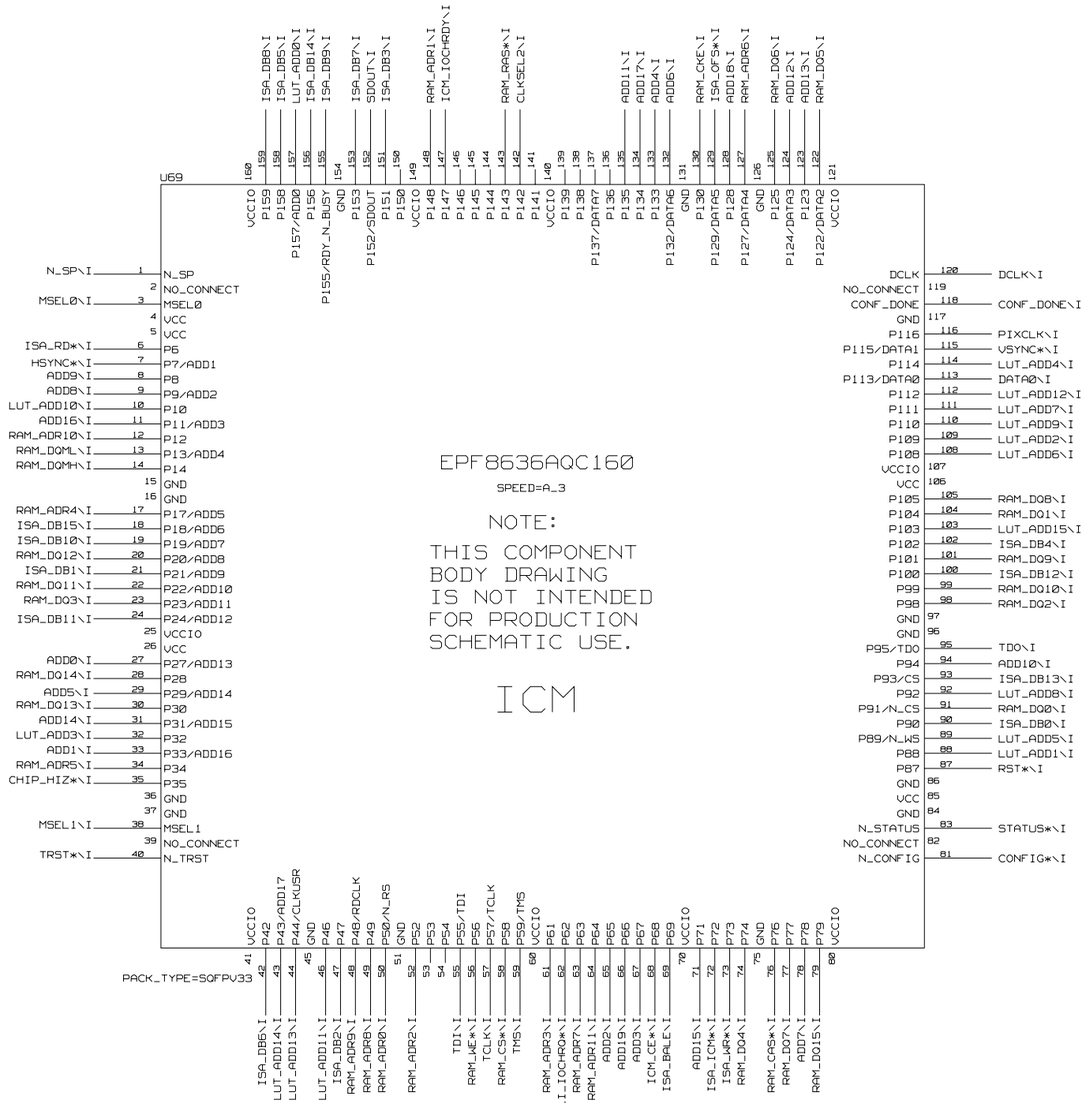

DRAWING
LAST_MODIFIED=Mon Apr 24 12:33:11 2000

OEC MEDICAL SYSTEMS, INC.

SIZE	DWG NO.	REV
D	00-879002	B6
SCALE:		SHEET 11 OF 16

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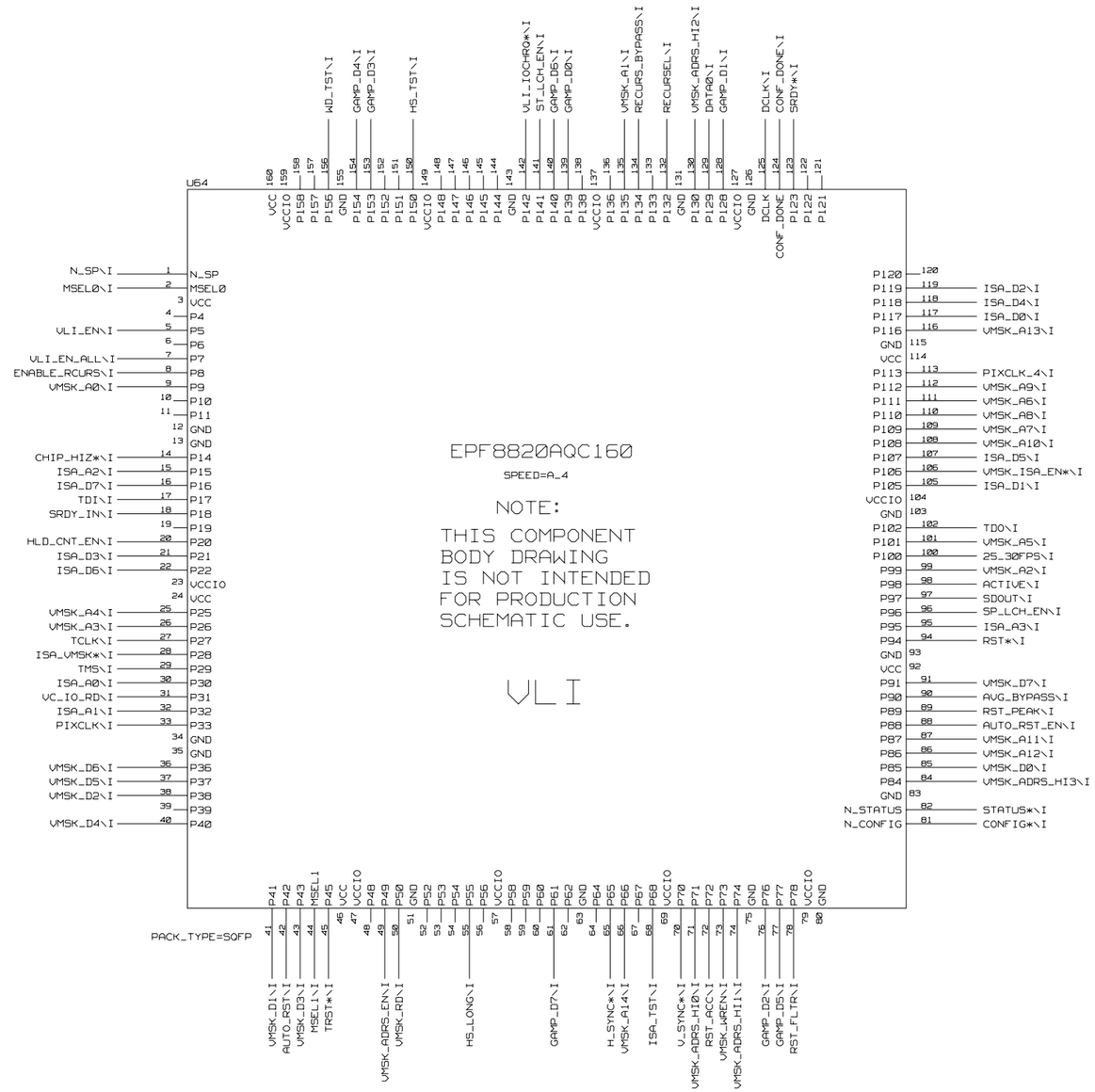

DRAWING

LAST_MODIFIED=Mon Apr 24 12:33:13 2000

OEC MEDICAL SYSTEMS, INC.

SIZE	DWG NO.	REV
D	00-879002	B6
SCALE:		SHEET 12 OF 16

05-017-9/93

*** Signal Cross-Reference ***
--- for the entire design --

+5B	3C5 1B1 1C1 7A7
+5VDC	3D8
+5VMB	4B6 4B7 4D3 4D4 3B8 4A6 4B6 4C6 4D6
33EN	1D3 1D6
34MHZ	1D5
39EN	1C3 1C6
39MHZ	1C5
ACTIVE	6C4
AD_IN <11..0>	2A1 2B1 2D3 3A3 3A4 3B3
AD_LCHEN *	2B2
AEN	4D8 4D6
AUTO_RST	6C4
AUTO_RST_EN	4B2 6C5
AVG_BYPASS	4A3 6C5
AVIG	2D3 2A8
BALE	4B8 4D6
BANK_SEL <5..0>	4B2 3C7 5B4 5B7 5D4
BBVCC	1D5 3B8
BP_CLAMP *	1D3 2B5
BP_EN *	4A2 1D8
BP_VSYNC *	4D6 1D8
CAM_GAIN <7..0>	4A2 5A3 5A4 5B3
CFD1	1D3 3D3
CFD2	3D2 4D4
CFD3	4D3 5D7
CFD4	5D6 6D5
CFG_DONE *	3C7 6D3 4C4
CLKSEL0	4A2 1B5
CLKSEL1	4A2 1B5
CLKSEL2	4A2 1B3 1B5 5C7 6C5
CLK_OUT	1B5 1D3
COMP_SYNC	1B5 1C5
CONFIG *	1D5 3C7
CONF_DONE	3C8 6D4
CRCT_HIZ *	3D3
CS_TEST	1B5 2C2
D1	1C4 1B3
DAC_LCH *	4B3 2C8
DAC_WR *	4B3 2C8
DATA0	3B8
DATA0A	3C6 1D5 3D3 4D4 5D7 6D5
DCLK	3C8 1D5
DCLKA	3C6 3D3 5D7
DCLKB	3C6 4D4 6D5
DEC_HIZ *	4D4
DEC_STAT *	4D3
DS3_DRV *	3C6
GAIN <15..0>	5C2 5D2 3B3 3B4 3C3
GAIN_BYPASS	4A2 3D3
GAIN_CE *	4C3 5D3
GAIN_OE *	4C3 5D3
GAIN_WR *	4C3 5D3
GAMMA <15..0>	6B6 6C6 6D6 3B3 3B4
GAMP_CE *	4C3 6D2
GAMP_D <7..0>	6D1 6D2 6B5 6C2
GAMP_OE *	4C3 6D2
GAMP_SEL <2..0>	4D2 6D2
GAMP_WR *	4C3 6D2
GAM_BYPASS	4A3 3D3
GAM_CE *	4C3 6C7 6D7
GAM_OE *	4C3 6C7 6D7
GAM_SEL <2..0>	4D3 6C7 6D7
GAM_WR *	4C3 6C7 6D7
HRAMP	1A8 2D7
HSYNC *	1D3 2C3 2D8 2A2 5C7 6C5
ICM <15..0>	3C6 5B4 3C3 3C4 5A3 5A4 5A6 5B3 5B4 5B6
ICMDLY3 <6..0>	3A2 5C3 3A2 3B2 5C3
ICM_ADRS <11..0>	5B6

ICM_CAS *	5C6
ICM_CE *	4C3 5C8 5D7
ICM_CKE	5C6
ICM_CS *	5C6
ICM_D <15..0>	5B7 5C7
ICM_HIZ *	5C7
ICM_LDQM	5C6
ICM_RAS *	5C6
ICM_RDY	1D5 5D5
ICM_UDQM	5C6
ICM_WR *	5C6
INTERP_DIS	4B3 3D3
IOCHRDY	1D3 4D8
IOR *	4B8 4D6
IOW *	4B8 4D6
ISARESET	4C8 4D6
ISA_+12V	3C6 3D6 4B8
ISA_-12V	3D6 4B8
ISA_A <19..0>	4B5 4B6 4C6 2C8 4A4 4B4 5A4 5A5 5A7 5A8 5B4 5B7 5C4 5D4 6A4 6B3 6B5 6C3 6C8 6D3 6D4 6D8
ISA_AEN	4D5 4D4
ISA_BALE	4D5 4D4 5D7
ISA_D <15..0>	4A5 4A6 4B6 5A1 5B1 5B8 5C1 5C8 5D1 6B1 6C5 6D1 6D5 2B8 2C8 4A4 5A1 5B8 6A5 6B1 6B5 6D1
ISA_GAIN *	4C3 3D3 5C1 5C4 5D1 5D4
ISA_GAM *	4C3 3D3 6C5 6C8 6D5 6D8
ISA_GAMP *	4C3 3D3 6D1 6D3
ISA_GND	4B7 4B8 4C8
ISA_ICM *	4C3 5D7
ISA_IORD *	4D6 4C4
ISA_IOWR *	4D6 4C4
ISA_LA <23..20>	4D5 4B4
ISA_OFS *	4B3 3C7 5B1 5B4 5C1 5D7
ISA_RESET	4D5 4D4
ISA_SMEMR *	4D6 4C4 5B1 5C1 5C8 5D1 5D7 6B1 6C5 6D1 6D5
ISA_SMEMW *	4C6 4C4 5D7
ISA_VIDCTRL *	4B7 4C2 4A6
ISA_VMSK *	4C3 6D5
LA <23..20>	4D7 4D6
MAGSEL0	4A2 2A8
MAGSEL1	4A2 2A8
MEMCS16 *	4C7 4D3
MRST *	4D3 1D5 3D3 5C7 6C5
MUXVID	1B6 1C6 1D7
MVBUF	1D6
NRVID	1B7
NRZ_ODD_EVEN	1C5 1C6
ODD_EVEN	1C4 2C3 2B2
OFFSET <15..0>	5A2 5B2 3C3 3C4
OFFSUB <11..0>	3C2 5C3 5D3 3C2 5C3 5D3
OFS_CE *	4B3 5B3 5C3
OFS_OE *	4B3 5B3 5C3
OFS_WR *	4B3 5B3 5C3
PHASE_LOCK	1B1 1C5 4C4
PILOT_DET	1D6 1D5 4C4
PILOT_HI	1D8
PILOT_LO	1D8
PILOT_STBL	1D5
PILOT_TONE	1D6 1C5
PIXCLK	1A3 2C3 1D5 2A2 2B3 3D3 4D4 5C5 5C7 6C5
PIXCLK2Q	1A3 1D5
PIXDAT <11..0>	3C1 6C3 6C7 6D3 6D7 3C2 3D2 6B7 6B8 6C2 6C3 6C7 6D2 6D7
PIX_DIV4	1B3 6C5
PU1000	2D6
PU1000G	2C6
RAM_DQ <15..0>	5B5 5C5
RECURSEL	4B3 6C5
RECURS_BYPASS	4B2 6C5

REV <3..0>	4C4
RST *	4D4
RST_ACC	4B3 6C5
RST_FLTR	4B3 6C5
RST_PEAK	4B3 6C5
SA <19..0>	4C8 4B6 4B7 4C6
SD <15..0>	4A6 4B6 4C7 4D8 4A7
SLAV_SYNC *	2D1 4D7
SMEMR *	4B8 4D6
SMEMW *	4B8 4C6
SPARE1	4A3
SPARE2	4D3
SPARE3	4D3
SRDY	4C3 6D5
SRDY *	4B8 6D3
STATUS *	1D3 3B7
STAT_CRCT *	3D2
STAT_ICM *	5D6
STAT_VLI *	6D4
SYNC_HIZ *	1D5
TCLK	4D5 1D5 4D4 5D7 6D5
TDI	4D5 1D5
TDO	4D5 6D3
TDO1	4D3 5D7
TDO2	5D6 6D5
TDO_0	1D3 4D4
TMS	4D5 1D5 4D4 5D7 6D5
TRST *	4D5 1D5 4D4 5D7 6D5
U1 *	1C3 1B3
U4G	1B7 1C7 2D6 2D8
U4VM	2D6 1B7 1C7 2D8
U4VP	2D6 1B7 1C7 2D8
U23M	2D4 1A8
U23P	2D4 1A8
VCO	1B1 1C5
VCO_EN *	1C3 1B2
VCRVID	1B7 1C7
VCR_HSYNC	1C5
VCR_ODD_EVEN	1C5 1C6
VC_D <11..0>	2D1 3B2 2D2 3B2
VC_FIELD	2B1 2C3 2D2
VC_HSYNC *	2A1 2C2 2D3
VC_IO_RD	4C3 6D5
VC_PIXCLK	1A3 2C2
VC_RD *	4B7 4C3 4A6
VC_VSYNC *	2A1 2C3 2D2
VID	1A5 2A8
VIDEO_HI	1B8
VIDEO_LO	1B8
VIDSEL0	4A2 1A8 1B5 2B6
VIDSEL1	4A2 1A8 1C5
VLI_EN	6C4
VLI_EN_ALL	4B3 6C5
VLI_HIZ *	6C5
VLI_IOCHRQ *	5D7 6D3
VMSK_A <15..0>	6B3 6A3 6A4 6B2 6B4
VMSK_ADRS_EN	6C4
VMSK_BANK0	4B3 6C5
VMSK_BANK1	4B3 6C5
VMSK_BANK2	4A3 6C5
VMSK_BANK3	4A3 6C5
VMSK_CE *	4C3 6B2
VMSK_D <7..0>	6B1 6B2 6B5
VMSK_ISA_EN *	6C4
VMSK_OE *	4C3 6B2
VMSK_WR *	4C3 6B2
VMSK_WREN	6C3 4C4
VSYNC *	1D3 2C3 2D7 4C4 2A2 5C7 6C5

OEC MEDICAL SYSTEMS, INC.

SIZE	DWG NO.	REV
D	00-879002	B6

SCALE: | SHEET 13 OF 16

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*** Unit Cross-Reference ***
--- for the entire design --

C1	CERSMT_1206	1D7
C2	CERSMT_1206	3A7
C3	CERSMT_1206	3B8
C4	CERSMT_1206	1B7
C5	CERSMT_1206	1C8
C6	CERSMT_1206	1C6
C7	CERSMT_1206	1D6
C9	TASMT_7343	3D7
C10	CERSMT_1206	1B7
C11	CERSMT_1206	1C6
C12	CERSMT_1206	1C6
C13	CERSMT_1206	1C5
C14	CERSMT_1206	1C8
C15	CERSMT_1206	1C8
C16	CERSMT_1206	1D8
C17	CERSMT_1206	1A3
C18	CERSMT_1206	1B6
C19	CERSMT_1206	1B6
C20	CERSMT_1206	1C7
C21	CERSMT_1206	1C7
C22	CERSMT_1206	1B7
C23	CERSMT_1206	1C7
C24	CERSMT_1206	1D7
C25	CERSMT_1206	1D7
C26	CERSMT_1206	1C7
C27	CERSMT_1206	1B5
C28	MICAR_30P_41159575	1B2
C29	MICAR_20P_41159573	1B1
C30	TASMT_7343	3D7
C31	CERSMT_1206	1A6
C32	CERSMT_1206	1B7
C33	CERSMT_1206	2D6
C34	CERSMT_1206	2D6
C35	CERSMT_1206	7A6
C36	CERSMT_1206	1B5
C37	CERSMT_1206	7A6
C38	CERSMT_1206	1B1
C39	CERSMT_1206	1B1
C40	CERSMT_1206	1A6
C41	CERSMT_1206	2A6
C42	CERSMT_1206	2A6
C43	TASMT_7343	3D7
C44	CERSMT_1206	2A8
C45	CERSMT_1206	2A8
C46	CERSMT_1206	2A7
C47	CERSMT_1206	2A7
C48	CERSMT_1206	2B6
C49	CERSMT_1206	2B6
C50	CERSMT_1206	2A4
C51	CERSMT_1206	1C1
C52	CERSMT_1206	2C4
C53	CERSMT_1206	2A8
C54	CERSMT_1206	2A8
C55	CERSMT_1206	2B5
C56	CERSMT_1206	2B3
C57	CERSMT_1206	2A3
C58	CERSMT_1206	2B5
C59	CERSMT_1206	2C4
C60	TASMT_6032	2C7
C61	TASMT_6032	2D6
C62	CERSMT_1206	2D4
C63	CERSMT_1206	2A4
C64	POLYPR_0X1U_41507724	2D6
C65	POLYPR_0X01U_41507725	2D8
C66	CERSMT_1206	2B4
C67	CERSMT_1206	2B3
C68	CERSMT_1206	2D4
C69	CERSMT_1206	2B7
C70	CERSMT_1206	2C7
C71	TASMT_6032	2C6
C72	TASMT_6032	2C5
C73	CERSMT_1206	2A4
C74	CERSMT_1206	2A4
C75	CERSMT_1206	2B4
C76	CERSMT_1206	2C4
C77	CERSMT_1206	2C8
C78	CERSMT_1206	2B7
C79	CERSMT_1206	2B7
C80	CERSMT_1206	2D8
C81	CERSMT_1206	2B7
C82	CERSMT_1206	3D5
C83	CERSMT_1206	3D4
C84	TASMT_7343	3D7
C85	TASMT_6032	3D6
C86	TASMT_6032	3D5
C87	TASMT_7343	4B7
C88	CERSMT_1206	3A7
C89	CERSMT_1206	3A7
C90	CERSMT_1206	1D6
C91	CERSMT_1206	3A8
C92	CERSMT_1206	3B7
C93	CERSMT_1206	3A8
C94	CERSMT_1206	3A7
C95	CERSMT_1206	3A7
C96	CERSMT_1206	3A7
C97	CERSMT_1206	3B7
C98	CERSMT_1206	3B6
C99	CERSMT_1206	3A7
C100	CERSMT_1206	3A7
C101	CERSMT_1206	3A8
C102	CERSMT_1206	3B8
C103	CERSMT_1206	3A6
C104	CERSMT_1206	3A7
C105	CERSMT_1206	3A7
C106	CERSMT_1206	3A6
C107	CERSMT_1206	3A6
C108	CERSMT_1206	3A8
C109	CERSMT_1206	3A7
C110	CERSMT_1206	3A7
C111	CERSMT_1206	3A6
C112	CERSMT_1206	3A7
C113	CERSMT_1206	3A6
C114	CERSMT_1206	3A8
C115	CERSMT_1206	3A7
C116	CERSMT_1206	3A8
C117	CERSMT_1206	3A6
C118	CERSMT_1206	3B8
C119	CERSMT_1206	3A5
C120	CERSMT_1206	4D4
C121	CERSMT_1206	3A7
C122	CERSMT_1206	3A7
C123	CERSMT_1206	3A8
C124	CERSMT_1206	3A7
C125	CERSMT_1206	3A7
C126	CERSMT_1206	1B2
C127	CERSMT_1206	3A8
C128	CERSMT_1206	3A7
C129	CERSMT_1206	3B8
C130	CERSMT_1206	3A6
C131	CERSMT_1206	3B7
C132	CERSMT_1206	3A7
C133	CERSMT_1206	3A7
C134	CERSMT_1206	3A6
C135	CERSMT_1206	3A6
C136	CERSMT_1206	3A7
C137	CERSMT_1206	3C5
C138	CERSMT_1206	1D7
C139	CERSMT_1206	3A8
C140	CERSMT_1206	3A6
C141	CERSMT_1206	3A8
C142	CERSMT_1206	3A6
C143	CERSMT_1206	3A6
C144	CERSMT_1206	3A7
C145	CERSMT_1206	3A8
C146	CERSMT_1206	3A8
C147	CERSMT_1206	3A7
C148	CERSMT_1206	3A7
C149	CERSMT_1206	3A7
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C152	CERSMT_1206	3A8
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C162	CERSMT_1206	3A8
C163	CERSMT_1206	3B6
C164	CERSMT_1206	3B8
C165	CERSMT_1206	3A7
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C170	CERSMT_1206	3A7
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C185	CERSMT_1206	3A7
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C199	CERSMT_1206	3B6
C200	CERSMT_1206	3B8
C201	CERSMT_1206	3A8
C202	CERSMT_1206	3A5
C203	CERSMT_1206	3A6
C204	CERSMT_1206	3A6
C205	CERSMT_1206	3A6
C206	CERSMT_1206	3B8
C207	CERSMT_1206	3A6
C208	CERSMT_1206	3B6
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C213	CERSMT_1206	3A8
C214	CERSMT_1206	3B7
C215	CERSMT_1206	3A6
C216	CERSMT_1206	3B6
C217	CERSMT_1206	2B8
C218	CERSMT_1206	2B8
C219	CERSMT_1206	2B8
C220	CERSMT_1206	2B8
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C232	CERSMT_1206	3B6
C233	CERSMT_1206	3B6
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C245	CERSMT_1206	3A7
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C250	CERSMT_1206	3A3
C251	CERSMT_1206	3A5
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C261	CERSMT_1206	3A6
C262	CERSMT_1206	3A6
C263	CERSMT_1206	3A4
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C265	CERSMT_1206	3A8
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C267	CERSMT_1206	3A6
C268	CERSMT_1206	3B7
C269	CERSMT_1206	4B6
C270	CERSMT_1206	3A7
C271	CERSMT_1206	3A3
C272	CERSMT_1206	3A4
C273	CERSMT_1206	3A6
C274	CERSMT_1206	3A4
C275	CERSMT_1206	3A4
C276	CERSMT_1206	3A6
C277	CERSMT_1206	3B7
C278	CERSMT_1206	3A3
C279	CERSMT_1206	3A4
C280	CERSMT_1206	3A4
C281	CERSMT_1206	3A4
C282	CERSMT_1206	4A6
C283	CERSMT_1206	4D6
C284	CERSMT_1206	4C6
C285	CERSMT_1206	4C6
C286	CERSMT_1206	4D6
C287	CERSMT_1206	3B7
C288	CERSMT_1206	3A5
C289	CERSMT_1206	3A4
C290	CERSMT_1206	3A5

OEC MEDICAL SYSTEMS, INC.

SIZE	DWG NO.	REV
D	00-879002	B6
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C291	CERSMT_1206	3A3
C292	CERSMT_1206	3A5
C293	CERSMT_1206	3A3
C294	CERSMT_1206	3A5
C295	CERSMT_1206	3A3
C296	CERSMT_1206	3A5
C297	CERSMT_1206	3A8
C298	CERSMT_1206	3B7
C299	CERSMT_1206	1A3
C300	CERSMT_1206	1A3
C301	CERSMT_1206	4B8
C302	CERSMT_1206	3A5
C303	CERSMT_1206	1D6
C304	CERSMT_1206	3C5
C305	TASMT_6032	3C6
C308	CERSMT_1206	3C5
C309	CERSMT_1206	3A6
C310	CERSMT_1206	2C3
C311	CERSMT_1206	2C3
CR1	DIO_SMT_VAR_2101	1B2
CR2	DIO_SMT_VAR_2101	1B1
CR3	DIO_SMT_VAR_2101	1B1
CR4	DIO_SMT_1501A	1B2
CR5	DIO_SMT_1501A	1B2
CR6	DIO_SMT_1501A	1D7
CR7	DIO_SMT_1501A	1D7
DS1	LED_RA_67599204	1C1
DS2	LED_RA_67599204	1C1
DS3	LED_RA_67599204	3C5
E1	JMPST_1X2_90012601	1D7
E2	JMPST_1X3_90012601	1A5
E3	JMPST_1X3_90012601	1A5
E4	JMPST_1X3_90012601	1A5
E5	JMPST_1X3_90012601	1A4
E6	JMPST_1X3_90012601	1A4
E7	JMPST_1X3_90012601	1A4
E8	JMPST_1X2_90012601	2A5
E9	JMPST_1X2_90012601	2B5
E10	JMPST_1X2_90012601	4D4
E11	EMI_ENCLOS_90116701	3C5
E12	JMPST_1X2_90012601	1B5
FL1	EMI_FLTR_43600000	3D7
FL2	EMI_FLTR_43600000	3D7
FL3	EMI_FLTR_43600000	3D6
FL4	EMI_FLTR_43600000	3D5
L1	INDSMTMLD_1210	2B6
L2	INDSMTMLD_1210	1B1
L3	INDSMTMLD_1210	2B6
L4	INDSMTMLD_1210	2B6
L5	INDSMTMLD_1210	2B6
L6	INDSMTMLD_1210	2B6
L7	INDSMTMLD_1210	2B6
P1	CONN_EDG_AB31	4B8 4B8 4B8 4B8 4C8 4C8 4C8 4C8 4C8 4D8 4D8 4D8
P2	CONN_EDG_CD18	4B7 4C7 4C7 4C7 4C7 4C7 4D7 4D7 4D7 4D7
P3	D50RA_40P_51180007	2C1 2C1 2D1 2D1
P5	CONN_SMBHS_58019880	1C8
P6	HDMLXMFLKRA_2X4_51411327	1A8 1B8 1D8 1D8
P7	MINJRRA_2X4_51411109	3D8
P8	HDMLXMFLKRA_2X2_51411325	2D1
P9	CONN_SMBHS_58019880	1C8
P10	HDBKRA_2X5_90012604	3B8 3B8 3C8 3C8
P11	HDBKRA_2X5_90012604	4D5
P12	HDBKST_2X20_90012602	2C2 2C2 2C2 2D2 2D2
Q1	MMBT3904	1D8
Q2	MMBT3904	1D7
Q3	MMBT3904	1B2
Q4	MMBT3906	1B2
R1	RESSMT_1206	1D7
R2	RESSMT_1206	1D7
R3	RESSMT_1206	1A3
R4	RESSMT_1206	1D6
R5	RESSMT_1206	3C7
R6	RESSMT_1206	1D8
R7	RESSMT_1206	1D7
R8	RESSMT_1206	1B8
R9	RESSMT_1206	1B7
R10	RESSMT_1206	1B8
R11	RESSMT_1206	1B8
R12	RESSMT_1206	1C6
R13	RESSMT_1206	1C8
R14	RESSMT_1206	1C8
R15	RESSMT_1206	1C8
R16	RESSMT_1206	1C8
R17	RESSMT_1206	1C8
R18	RESSMT_1206	1D7
R19	RESSMT_1206	1D6
R20	RESSMT_1206	1D6
R21	RESSMT_1206	1A3
R22	RESSMT_1206	7A7
R23	RESSMT_1206	1B7
R24	RESSMT_1206	1B8
R25	RESSMT_1206	1C6
R26	RESSMT_1206	1C8
R27	RESSMT_1206	1C8
R28	RESSMT_1206	1C8
R29	RESSMT_1206	1D8
R30	RESSMT_1206	1D8
R31	RESSMT_1206	1C6
R32	RESSMT_1206	1B2
R33	RESSMT_1206	1B2
R34	RESSMT_1206	1D6
R35	RESSMT_1206	1A3
R36	RESSMT_1206	3B8
R37	RESSMT_1206	1D8
R38	RESSMT_1206	1A7
R39	RESSMT_1206	1B6
R40	RESSMT_1206	1B8
R41	RESSMT_1206	1C7
R42	RESSMT_1206	1A8
R43	RESSMT_1206	1C7
R44	RESSMT_1206	1D7
R45	RESSMT_1206	1B8
R46	RESSMT_1206	1C7
R47	RESSMT_1206	1B6
R48	RESSMT_1206	1B6
R49	RESSMT_1206	1B2
R50	RESSMT_1206	2C8
R51	RESSMT_1206	1B5
R52	RESSMT_1206	1A6
R53	RESSMT_1206	1D5
R54	RESSMT_1206	1B2
R55	RESSMT_1206	1D8
R56	RESSMT_1206	1A6
R57	RESSMT_1206	1B6
R58	RESSMT_1206	1C8
R59	RESSMT_1206	2D6
R60	RESSMT_1206	1A8
R61	RESSMT_1206	2D6
R62	RESSMT_1206	1B2
R63	RESSMT_1206	7A6
R64	RESSMT_1206	1B2
R65	RESSMT_1206	1B6
R66	RESSMT_1206	1B1
R67	RESSMT_1206	1B2
R68	RESSMT_1206	1A6
R69	RESSMT_1206	1A5
R70	RESSMT_1206	1A6
R71	RESSMT_1206	1A6
R72	RESSMT_1206	1A5
R73	RESSMT_1206	1A5
R74	RESSMT_1206	7A6
R75	RESSMT_1206	1C2
R76	RESSMT_1206	1B2
R77	RESSMT_1206	1B2
R78	RESSMT_1206	2A8
R79	RESSMT_1206	2B8
R80	RESSMT_1206	2B8
R81	RESSMT_1206	2A8
R82	RESSMT_1206	2A7
R83	RESSMT_1206	2B7
R84	RESSMT_1206	2B7
R85	RESSMT_1206	2B6
R86	RESSMT_1206	2A5
R87	RESSMT_1206	1B2
R88	RESSMT_1206	1C2
R89	RESSMT_1206	2C4
R90	RESSMT_1206	1C2
R91	RESSMT_1206	2D7
R92	RESSMT_1206	2D8
R93	RESSMT_1206	2A8
R94	RESSMT_1206	2A8
R95	RESSMT_1206	2A7
R96	RESSMT_1206	2A6
R97	RESSMT_1206	2A6
R98	RESSMT_1206	2B5
R99	RESSMT_1206	2B4
R100	RESSMT_1206	2B5
R101	RESSMT_1206	2C4
R102	RESSMT_1206	2B3
R103	RESSMT_1206	2B2
R104	RESSMT_1206	2A5
R105	RESSMT_1206	2A4
R106	RESSMT_1206	2B4
R107	RESSMT_1206	1D8
R108	RESSMT_1206	2A4
R109	RESSMT_1206	2B3
R110	RESSMT_1206	2B3
R111	RESSMT_1206	2D4
R112	RESSMT_1206	2D4
R113	RESSMT_1206	2D4
R114	RESSMT_1206	2D4
R115	RESSMT_1206	1A8
R116	RESSMT_1206	2D4
R117	RESSMT_1206	2D4
R118	RESSMT_1206	2D4
R119	RESSMT_1206	2C4
R120	RESSMT_1206	2C7
R121	RESSMT_1206	2C8
R122	RESSMT_1206	2B7
R123	RESSMT_1206	2B7
R124	RESSMT_1206	2C7
R125	RESSMT_1206	2D4
R126	RESSMT_1206	2A4
R127	RESSMT_1206	2A4
R128	RESSMT_1206	2B4
R129	RESSMT_1206	2A4
R130	RESSMT_1206	2A4
R131	RESSMT_1206	2A5
R132	RESSMT_1206	1D8
R133	RESSMT_1206	2C4
R134	RESSMT_1206	2B6
R135	RESSMT_1206	2C6
R136	RESSMT_1206	2B7
R137	RESSMT_1206	2D8
R138	RESSMT_1206	2C7
R139	RESWW_2_25W	3D6
R140	RESWW_2_25W	3D5
R141	RESSMT_1206	5D8
R142	RESSMT_1206	4B7
R143	RESSMT_1206	3C6
R144	RESSMT_1206	3B7
R145	RESSMT_1206	3C6
R146	RESSMT_1206	3B7
R147	RESSMT_1206	3B7
R148	RESSMT_1206	1D5
R149	RESSMT_1206	6D4
R150	RESSMT_1206	1D3
R151	RESSMT_1206	3C7
R152	RESSMT_1206	1C1
R153	RESSMT_1206	1C1
R154	RESSMT_1206	1D7
R155	RESSMT_1206	1D6
R156	RESSMT_1206	1D7
R157	RESSMT_1206	1B5
R158	RESSMT_1206	1D5
R159	RESSMT_1206	1D5
R160	RESSMT_1206	3C7
R161	RESSMT_1206	5C3
R162	RESSMT_1206	3D2
R163	RESSMT_1206	4D2
R164	RESSMT_1206	4C4
R165	RESSMT_1206	4C5
R166	RESSMT_1206	4C4
R167	RESSMT_1206	2B2
R168	RESSMT_1206	4D3
R169	RESSMT_1206	4D4
R170	RESSMT_1206	4D4
R171	RESSMT_1206	4C4
R172	RESSMT_1206	5D6
R173	RESSMT_1206	6D4
R174	RESSMT_1206	3D2
R175	RESSMT_1206	4C5
R176	RESSMT_1206	4C5
R177	RESSMT_1206	1D3
R178	RESSMT_1206	3D4
R179	RESSMT_1206	4C5
R180	RESSMT_1206	4C4
R181	RESSMT_1206	6C5
R182	RESSMT_1206	4B4
R183	RESSMT_1206	4D6
R184	RESSMT_1206	4C6
R185	RESSMT_1206	4C6
R186	RESSMT_1206	4D7
R187	RESSMT_1206	4D7
R189	RESSMT_1206	5D5
R190	RESSMT_1206	2A4
R193	RESSMT_1206	5D7
R194	RESSMT_1206	2A4
R274	RESSMT_1206	1D7
R275	RESSMT_1206	1D7
R276	RESSMT_1206	1D7
R277	RESSMT_1206	1D6
R278	RESSMT_1206	1C5
R280	RESSMT_1206	1D5
R281	RESSMT_1206	1A5
R282	RESSMT_1206	1A5
R283	RESSMT_1206	1A5
R284	RESSMT_1206	1A5
R285	RESSMT_1206	1A4
R286	RESSMT_1206	1A4
R287	RESSMT_1206	1B4
R288	RESSMT_1206	1A4
R289	RESSMT_1206	1A4
R290	RESSMT_1206	1A4
R291	RESSMT_1206	1A4
R292	RESSMT_1206	1A4
R293	RESSMT_1206	1A4
R294	RESSMT_1206	7A7
R295	RESSMT_1206	7A7
R296	RESSMT_1206	1B6
T1	XFMR_SMT_44800000	1D8
TP1	TEST_POINT_COLOR	1B8
TP2	TEST_POINT_COLOR	1D7
TP3	TEST_POINT_COLOR	1D6
TP4	TEST_POINT_COLOR	1D3
TP5	TEST_POINT_COLOR	3D6
TP6	TEST_POINT_COLOR	1D6
TP7	TEST_POINT_COLOR	1D3
TP8	TEST_POINT_COLOR	1D3
TP9	TEST_POINT_COLOR	3D7

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TP10	TEST_POINT_COLOR	1C3
TP11	TEST_POINT_COLOR	1D3
TP12	TEST_POINT_COLOR	1B3
TP13	TEST_POINT_COLOR	3D6
TP14	TEST_POINT_COLOR	3D7
TP15	TEST_POINT_COLOR	1B8
TP16	TEST_POINT_COLOR	1C5
TP17	TEST_POINT_COLOR	3D5
TP18	TEST_POINT_COLOR	1D5
TP19	TEST_POINT_COLOR	1D5
TP20	TEST_POINT_COLOR	1C3
TP21	TEST_POINT_COLOR	3D7
TP22	TEST_POINT_COLOR	4A2
TP23	TEST_POINT_COLOR	1C3
TP24	TEST_POINT_COLOR	3D7
TP25	TEST_POINT_COLOR	1B3
TP26	TEST_POINT_COLOR	1B1
TP27	TEST_POINT_COLOR	1D5
TP28	TEST_POINT_COLOR	4A2
TP29	TEST_POINT_COLOR	4D2
TP30	TEST_POINT_COLOR	3D7
TP31	TEST_POINT_COLOR	1B6
TP32	TEST_POINT_COLOR	2D7
TP33	TEST_POINT_COLOR	1B2
TP34	TEST_POINT_COLOR	1D3
TP35	TEST_POINT_COLOR	1C1
TP36	TEST_POINT_COLOR	4A2
TP37	TEST_POINT_COLOR	3D7
TP38	TEST_POINT_COLOR	1C3
TP39	TEST_POINT_COLOR	3A8
TP40	TEST_POINT_COLOR	4A2
TP41	TEST_POINT_COLOR	4B2
TP42	TEST_POINT_COLOR	4D2
TP43	TEST_POINT_COLOR	2B7
TP44	TEST_POINT_COLOR	1D3
TP45	TEST_POINT_COLOR	4D5
TP46	TEST_POINT_COLOR	4D5
TP47	TEST_POINT_COLOR	2D3
TP48	TEST_POINT_COLOR	1A5
TP49	TEST_POINT_COLOR	2C4
TP50	TEST_POINT_COLOR	2B5
TP51	TEST_POINT_COLOR	2B3
TP52	TEST_POINT_COLOR	2B3
TP53	TEST_POINT_COLOR	5D5
TP54	TEST_POINT_COLOR	5C6
TP55	TEST_POINT_COLOR	1B3
TP56	TEST_POINT_COLOR	6C3
TP57	TEST_POINT_COLOR	6C3
TP58	TEST_POINT_COLOR	4D3
TP59	TEST_POINT_COLOR	4A2
TP60	TEST_POINT_COLOR	2C4
TP61	TEST_POINT_COLOR	2D8
TP62	TEST_POINT_COLOR	2C6
TP63	TEST_POINT_COLOR	2C8
TP64	TEST_POINT_COLOR	3D5
TP65	TEST_POINT_COLOR	5D5
TP66	TEST_POINT_COLOR	4B7
TP67	TEST_POINT_COLOR	5D6
TP68	TEST_POINT_COLOR	6C4
TP69	TEST_POINT_COLOR	3D5
TP70	TEST_POINT_COLOR	2D6
TP71	TEST_POINT_COLOR	3D4
TP72	TEST_POINT_COLOR	4B6
TP73	TEST_POINT_COLOR	4D5
TP74	TEST_POINT_COLOR	4D5
TP75	TEST_POINT_COLOR	6C3
TP76	TEST_POINT_COLOR	4D6
TP77	TEST_POINT_COLOR	4D5
TP78	TEST_POINT_COLOR	4A2
TP79	TEST_POINT_COLOR	4C4
TP80	TEST_POINT_COLOR	4A2
TP81	TEST_POINT_COLOR	5C5
TP82	TEST_POINT_COLOR	4D5

TP83	TEST_POINT_COLOR	4A2
TP84	TEST_POINT_COLOR	3D7
TP85	TEST_POINT_COLOR	4B7
TP86	TEST_POINT_COLOR	3D7
TP87	TEST_POINT_COLOR	1B3
TP88	TEST_POINT_COLOR	3C5
TP89	TEST_POINT_COLOR	4B6
TP90	TEST_POINT_COLOR	1B4
U1	MAX9698_DG	1D7 7A4
U2	74LS123	1D5 1D6
U3	EPC1	3B7
U4	74HCT244	3C6
U5	MAX452	1B8
U6	GS4981	1C6
U7	MAX452	1C8
U8	MAX452	1D8
U9	MAX452	1D6
U10	CY7B991	1B4
U11	74HCT244	6D3
U12	SRAM_32KX8	6D2
U13	74F02	1D8 7A7
U14	MAX454	1B7
U15	GS4881	1C7
U16	GS4881	1D7
U17	MAX9698_AG	1B6 7A5
U19	74HCT244	6C8
U20	74HCT244	6D3 6D8
U21	74HCT245	6D1
U22	HFA1103	1A6
U23	DG411	1B7 1C7 2D6 2D8
U24	74F02_VCC	1B3 2A7 2B6
U25	LF412C	1B2 7A6
U26	74F02_VCC	1B1 1C1 7A7
U27	74HCT245	5C1
U28	TC551664	5D3
U29	74HCT244	5C4
U30	74HCT245	6D5
U31	SRAM_32KX8	6D7
U32	CLC520	2A8
U33	MAX454	2A7
U34	DG411	2B4 2B5
U35	MAX9698_AG	1C2
U36	74HCT244	5D4
U37	74HCT245	5D1
U38	74HCT244	5B4
U39	74HCT245	6C5
U40	SRAM_32KX8	6C7
U41	MAX452	2B4
U42	ADS800	2B3
U43	OP177	2C4
U44	74F574	2B1
U45	74F574	2A1
U47	SRAM_128KX8	5B3
U48	SRAM_128KX8	5C3
U49	74HCT244	5B4
U50	SRAM_32KX8	6B2
U51	74HCT244	6B3
U52	74HCT244	6C3
U53	74HCT245	6B1
U54	EL4450	2D7
U55	EL4450	2D5
U56	MAX452	2A4
U57	LF412C	1A8 2D4
U58	AD680	2C5
U59	OP177	2C4
U60	LF412C	2C8 2D6
U61	DAC_MAX505	2C8
U62	74HCT245	5B1
U63	74HCT245	5C1
U66	7805	3D6
U67	7905	3D5
U68	SDRAM_1MX16	5C5
U70	74HCT245_VCC	4B6

U71	74LCX16245	5C8
U72	74HCT244_VCC	4D6
U73	74HCT244_VCC	4C6
U74	74HCT244_VCC	4C6
U75	74HCT244_VCC	4D6
U76	74HCT245_VCC	4A6
U77	74HC14	1C5 6D3 7A7
U78	78L05	3C6
XE2	JMP_BERG	1A5
XE3	JMP_BERG	1A5
XE5	JMP_BERG	1A4
XE6	JMP_BERG	1A4
XE7	JMP_BERG	1A4
XE9	JMP_BERG	2B5
XE10	SHORT_PC_X1	1D5
XE11	SHORT_PC_X1	1D5
XE12	SHORT_PC_X1	5D3
XE13	SHORT_PC_X1	5D3
XE14	SHORT_PC_X1	3D3
XE15	SHORT_PC_X1	3D3
XE16	SHORT_PC_X1	4D4
XE17	SHORT_PC_X1	4D4
XE18	SHORT_PC_X1	5D7
XE19	SHORT_PC_X1	5D7
XE20	SHORT_PC_X1	6D5
XE21	SHORT_PC_X1	6D5
XU66	HTSNK_T0220HU_66899846	3D5
XU67	HTSNK_T0220HU_66899846	3D5
Y1	OSC_8P_EN_10TTL	1C6
Y2	OSC_8P_EN_10TTL	1D6

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ENGIN. REV. 4.1 REVISIONS — EDR 01346

REV	DESCRIPTION	DATE	APPROVED
A	REL TO MFG PER ECO BA20	3-24-98	C. BALL
A1	REVISED PER ECO BW38	4-05-99	MAHON
A2	REVISED PER ECO BY09	5-14-99	C. BALL
A3	REVISED PER ECO CD96	10-1-99	C. BALL
A4	REVISED PER ECO CF94		

P8 connector: DCLK, GND, CONF_DONE, VCC, NCONFIG, BBVCC, NSTATUS, BBGND, DATA0, GND

P3 connector: +5VDC_SEN, +5VDC, +3.3V, +3.3V_SEN, GND, +5VDC, +3.3V, GND

U13 74LCX16245 — CONF_DONE DS1 3.3V DRIVE

FPGA_DCLKA OUT — 3D5 8D8 11D7 12D8 14D7

FPGA_DCLKB OUT — 5D6 6D6 7D7 9D8

PCI_TRST* OUT — 3D5 5D6 6D6 7D7 8D8 9D8 10D5 11D7 12D8 14D7

PCI_TCK OUT — 3D5 5D6 6D6 7D7 8D8 9D8 10D5 11D7 12D8 14D7

PCI_TMS OUT — 3D5 5D6 6D6 7D7 8D8 9D8 10D5 11D7 12D8 14D7

FPGA_DATA0A OUT — 3D5 8D8 11D7 12D8 14D7

FPGA_DATA0B OUT — 5D6 6D6 7D7 9D8 10D5

JTAG LOOP ORDER

13D8	PCI_TDI	TDI_IMG	11D7
11D5	IMG_TDO	TDI_PEAK	12D8
12D5	PEAK_TDO	TDI_ISC	3D5
3D3	ISC_TDO	TDI_FIFO_C	14D7
14D5	FIFO_C_TDO	TDI_MASK	8D8
8D5	MASK_TDO	TDI_TEXT	10D5
10D3	TEXT_TDO	TDI_EDGE	6D6
6D4	EDGE_TDO	TDI_MANRS	5D6
5D4	MANRS_TDO	TDI_FLTR	7D7
7D5	FLTR_TDO	TDI_BIT	9D8
9D5	BIT_TDO	PCI_TDO	13D8

ALTERA CONFIGURATION ORDER

14C1	NCONFIG1	NCONFIG_TEXT
10D3	TEXT_CONF_DONE	NCONFIG_EDGE
6D4	EDGE_CONF_DONE	NCONFIG_MANRS
5D4	MANRS_CONF_DONE	NCONFIG_FLTR
7D5	FLTR_CONF_DONE	NCONFIG_BIT
9D6	BIT_CONF_DONE	NCONFIG_IMG
11D6	IMG_CONF_DONE	NCONFIG_PEAK
12D6	PEAK_CONF_DONE	NCONFIG_ISC
3D4	ISC_CONF_DONE	NCONFIG_FIFO_C
14D6	FIFO_C_CONF_DONE	NCONFIG_MASK
8D6	MASK_CONF_DONE	CONF_DONE

U18-103	10D5
U29-120	6D6
U53-120	5D6
U62-103	7D7
U59-120	9D8
U24-103	11D7
U48-103	12D8
U22-120	3D5
U36-103	14D7
U27-103	8D8
P8-3	1D7
	3C4

13-311104-00	NUT, HEX-LK-EXT-T, 4-40, SST, NA, A-.250
12-225104-06	SCR, SEMS SPR, PAN, TRX, 4-40, 3/8, SZC
ASM_U65	
00-880639-02	ASM, FW, IP PLX, 9800
ASM_U49	
00-880664-03	ASM, FW, CNFG, IP, 9800
ASM_U10	
00-880666-05	ASM, FW, U10, IP, 9800
ASM_U19	
00-880669-05	ASM, FW, U19, IP, 9800
00-901419-01	BRKT, ISA, DSUB CUTOUT
00-901420-01	BRKT, PCI, RECT CUTOUT
00-879017-01	PCB, IMAGE PROCESSOR, ART/FAB, 9800
00-879016-03	SCH, PCB, IMAGE PROCESSOR, 9800
00-879018-60	SPEC, PERF, IMAGE PROC PCB, 9800-60
00-879018-61	SPEC, PERF, IMAGE PROC PCB, 9800-61

-03 SHOWN
-02 INACTIVE
-01 INACTIVE

ALTERA FPGA LOADER
POWER CONNECTOR

DRAWING LAST_MODIFIED=Wed Apr 5 13:10:57 2000
ACTIVE_BOMS=-23

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00-879018	9800
NEXT ASSEMBLY	USED ON
APPLICATION	

CONTRACT NO.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE:
FRACTIONS: +/-
DECIMALS: .XX+/-
.XXX+/-
ANGLES: +/-

MATERIAL
FINISH

DO NOT SCALE DRAWING

	APPROVED	DATE
DRAWN	J.ALLRED/G.POPE	12/10/96
CHECKED	GORDON POPE	12-16-96
ENGINEERING	J.ALLRED	12-16-96
APPROVED		

PARTS LIST

ITEM	QTY.	PART OR IDENT NO.	DESCRIPTION

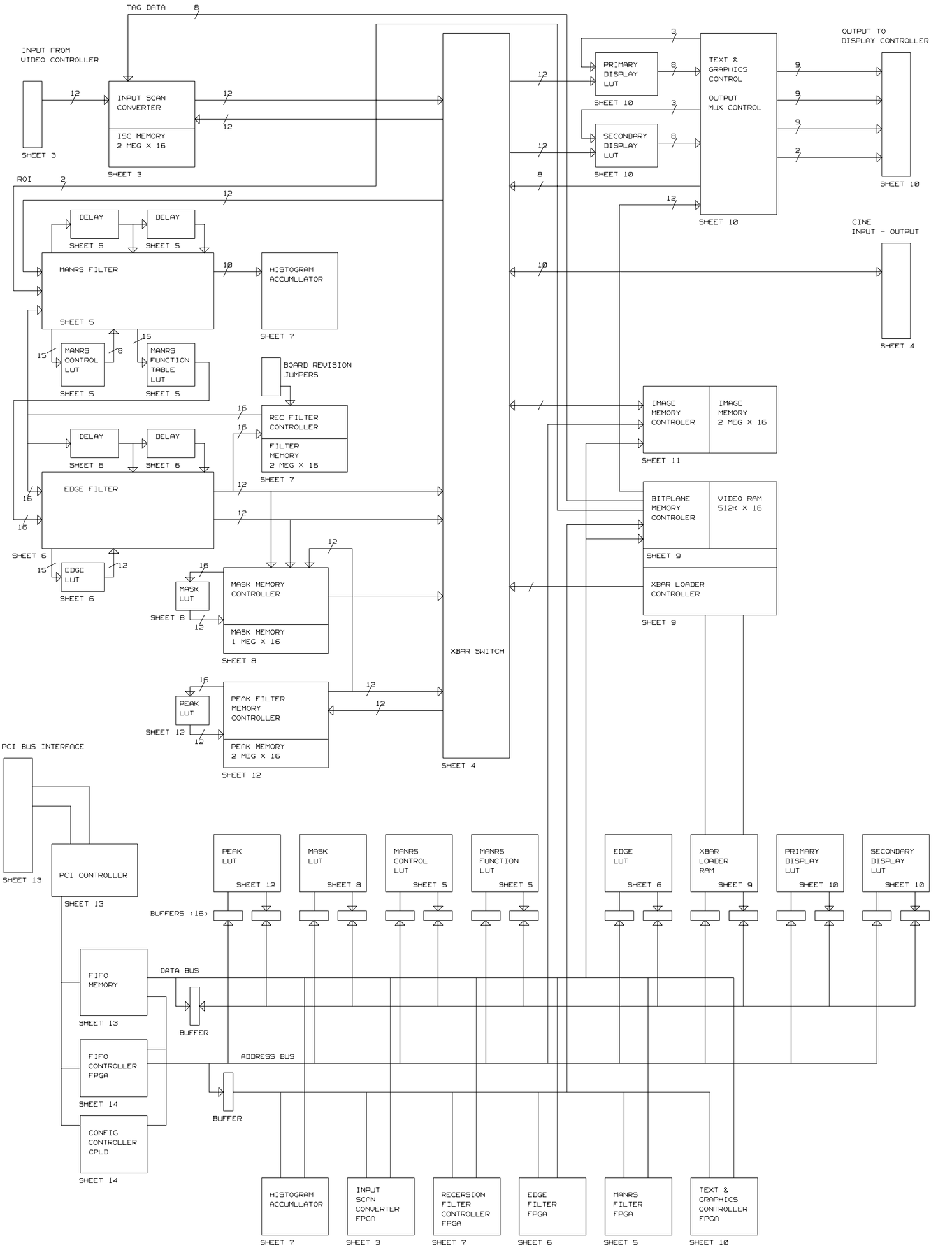
OEC MEDICAL SYSTEMS, INC.

DWG TITLE: SCH, IMAGE PROCESSOR, 9800

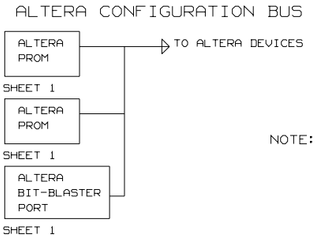
SIZE D | DWG NO. 00-879016 | REV A4

SCALE: NONE | SHEET 1 OF 34

05-016-9/93



ALTERA CONFIGURATION BUS



NOTE: BUS DEVICES SHOWN ON THIS BLOCK DIAGRAM MAY BE FOUND IN TWO PLACES. THIS SHOWS PCI INTERFACE PATHS AS WELL AS IMAGE FLOW DATA PATHS.

OEC MEDICAL SYSTEMS, INC.

SIZE D | DWG NO. 00-879016 | REV A4 | SCALE | SHEET 2

BLOCK DIAGRAM WITH VIDEO IMAGE PATHS AND PCI INTERFACE DATA PATHS

DWG NO. 00-879016 | SHT 2 | REV A4

IBRARIAN LAST MODIFIED Mon Apr 5 12:39:28 2000

THESE PIN NUMBERS ARE REVERSED FROM VIDEO CONTROL.

U22 INPUT_SCAN_CONV

U1 74LCX16374

U25 49FCT3806

U20 SDRAM_1MX16 SPEED=12_NS

U21 SDRAM_1MX16 SPEED=12_NS

PART OF INPUT_SCAN_CONV

INPUT SCAN CONVERTER

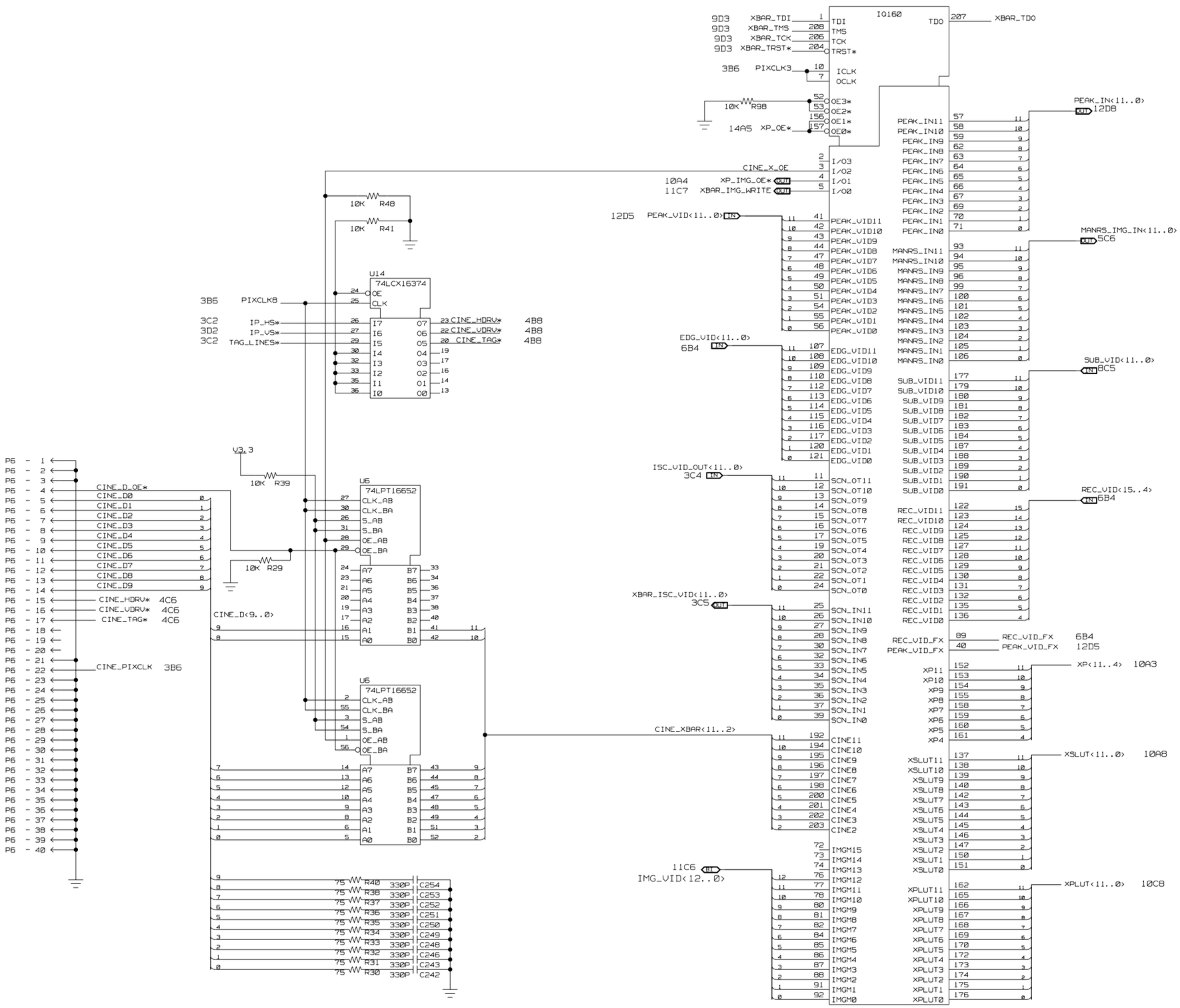
DRAWING LAST_MODIFIED=Wed Apr 5 13:11:02 2000

OEC MEDICAL SYSTEMS, INC.

SIZE	DWG NO.	REV
D	00-879016	A4

SCALE: | SHEET 3

05-017-9/93



CROSSPOINT SWITCH
CINE INTERFACE

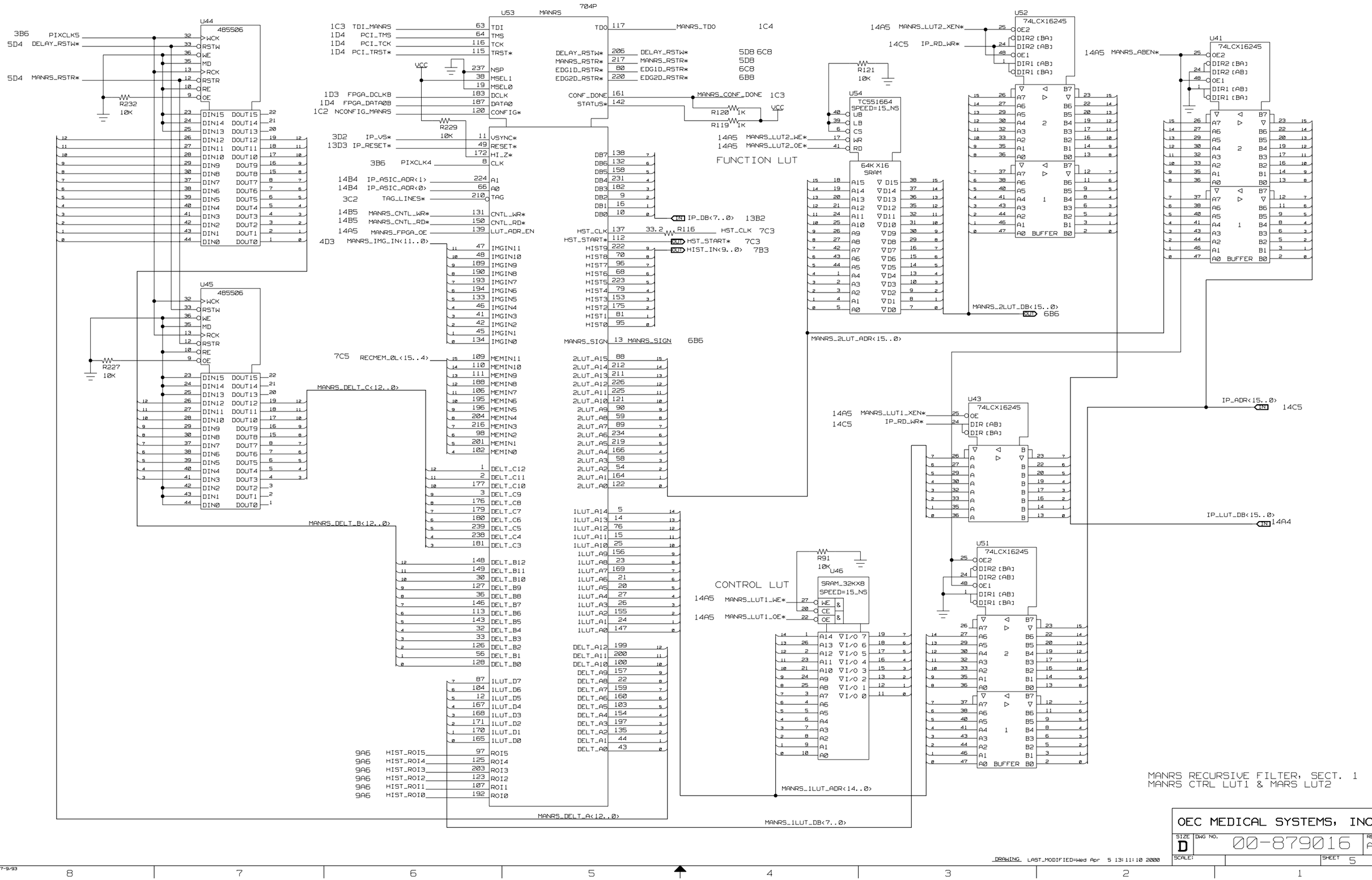
OEC MEDICAL SYSTEMS, INC.

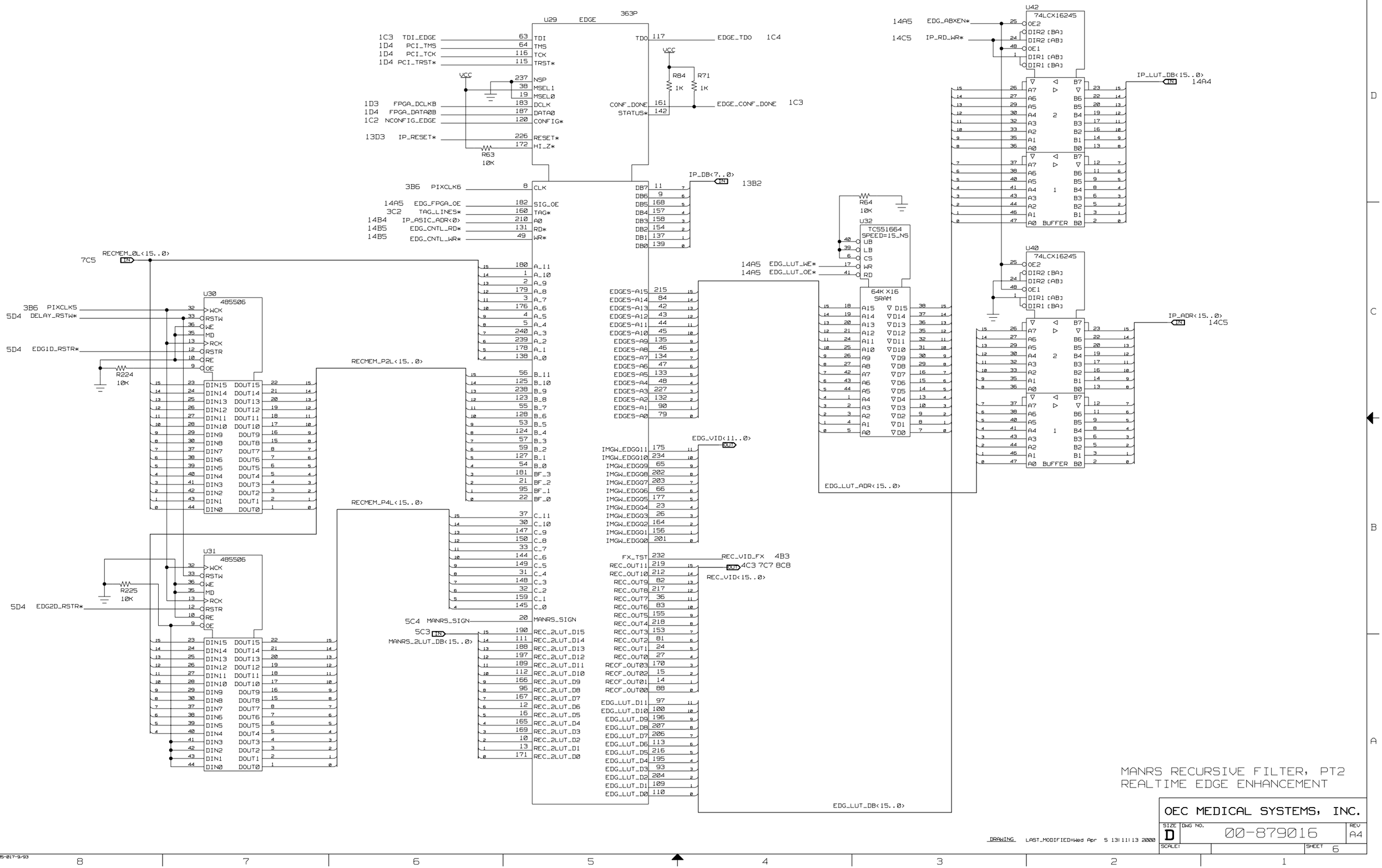
SIZE	DWG NO.	REV
D	00-879016	A4

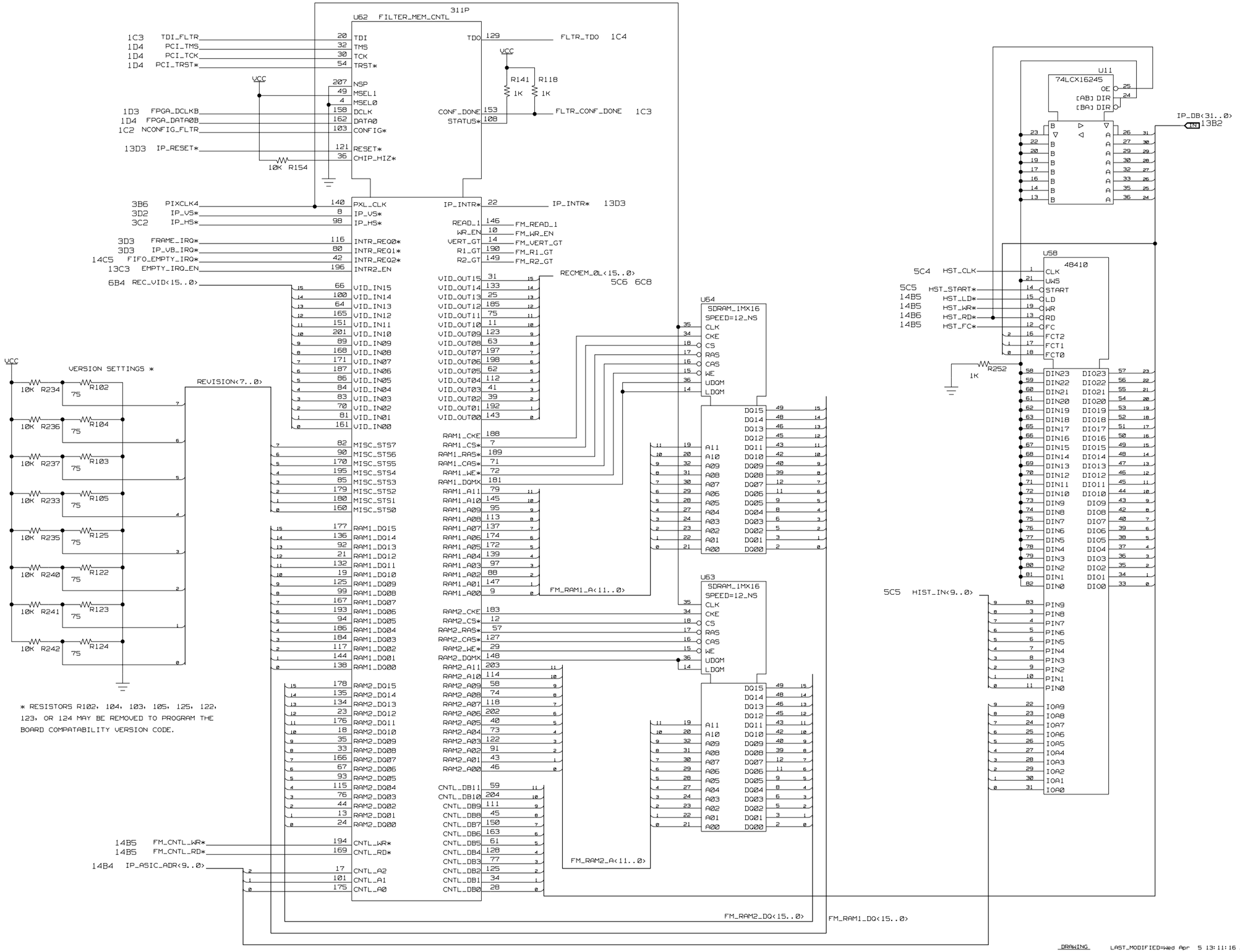
SCALE: | SHEET 4

DRAWING LAST_MODIFIED=Wed Apr 5 13:11:06 2000

05-017-9/93


704P
U53 MANRS
U44 485506
U45 485506
U52 74LCX16245
U41 74LCX16245
U54 TC551664 SPEED=15_NS
64K X16 SRAM
U43 74LCX16245
U51 74LCX16245
U46 SRAM_32KX8 SPEED=15_NS
FUNCTION LUT
CONTROL LUT
MANRS_2LUT_ADR<15..0>
MANRS_2LUT_DB<15..0>
MANRS_1LUT_ADR<14..0>
MANRS_1LUT_DB<7..0>
IP_ADR<15..0>
IP_LUT_DB<15..0>
MANRS_DELT_A<12..0>
MANRS_DELT_B<12..0>
MANRS_DELT_C<12..0>
MANRS RECURSIVE FILTER, SECT. 1
MANRS CTRL LUT1 & MARS LUT2


U29 EDGE 363P
1C3 TDI_EDGE 63 TDI
1D4 PCI_TMS 64 TMS
1D4 PCI_TCK 116 TCK
1D4 PCI_TRST* 115 TRST*
237 NSP
38 MSEL1
19 MSEL0
1D3 FPGA_DCLKB 183 DCLK
1D4 FPGA_DATA0B 187 DATA0
1C2 NCONFIG_EDGE 120 CONFIG*
13D3 IP_RESET* 226 RESET*
172 HI_Z*
R63 10K
VCC
R84 1K
R71 1K
TDO 117 EDGE_TDO 1C4
CONF_DONE 161
STATUS* 142 EDGE_CONF_DONE 1C3
3B6 PIXCLK6 8 CLK
14A5 EDG_FPGA_OE 182 SIG_OE
3C2 TAG_LINES* 160 TAG*
14B4 IP_ASIC_ADR<0> 210 A0
14B5 EDG_CNTL_RD* 131 RD*
14B5 EDG_CNTL_WR* 49 WR*
IP_DB<7..0> 13B2
DB7 11
DB6 9
DB5 168
DB4 157
DB3 158
DB2 154
DB1 137
DB0 139
7C5 RECMEM_0L<15..0>
A_11 180
A_10 1
A_9 2
A_8 179
A_7 3
A_6 176
A_5 4
A_4 5
A_3 240
A_2 239
A_1 178
A_0 138
U30 485506
3B6 PIXCLK5 WCK
5D4 DELAY_RSTW* RSTW
WE
MD
RCK
5D4 EDG1D_RSTR* RSTR
RE
OE
R224 10K
DIN15 DOUT15
DIN14 DOUT14
DIN13 DOUT13
DIN12 DOUT12
DIN11 DOUT11
DIN10 DOUT10
DIN9 DOUT9
DIN8 DOUT8
DIN7 DOUT7
DIN6 DOUT6
DIN5 DOUT5
DIN4 DOUT4
DIN3 DOUT3
DIN2 DOUT2
DIN1 DOUT1
DIN0 DOUT0
RECMEM_P2L<15..0>
B_11 56
B_10 125
B_9 238
B_8 123
B_7 55
B_6 128
B_5 53
B_4 124
B_3 57
B_2 59
B_1 127
B_0 54
BF_3 181
BF_2 21
BF_1 95
BF_0 22
RECMEM_P4L<15..0>
C_11 37
C_10 30
C_9 147
C_8 150
C_7 33
C_6 144
C_5 149
C_4 31
C_3 148
C_2 32
C_1 159
C_0 145
U31 485506
R225 10K
5D4 EDG2D_RSTR*
5C4 MANRS_SIGN 20 MANRS_SIGN
5C3 MANRS_2LUT_DB<15..0>
REC_2LUT_D15 190
REC_2LUT_D14 111
REC_2LUT_D13 188
REC_2LUT_D12 197
REC_2LUT_D11 189
REC_2LUT_D10 112
REC_2LUT_D9 166
REC_2LUT_D8 96
REC_2LUT_D7 167
REC_2LUT_D6 12
REC_2LUT_D5 16
REC_2LUT_D4 165
REC_2LUT_D3 169
REC_2LUT_D2 10
REC_2LUT_D1 13
REC_2LUT_D0 171
EDGES-A15 215
EDGES-A14 84
EDGES-A13 42
EDGES-A12 43
EDGES-A11 44
EDGES-A10 45
EDGES-A9 135
EDGES-A8 46
EDGES-A7 134
EDGES-A6 47
EDGES-A5 133
EDGES-A4 48
EDGES-A3 227
EDGES-A2 132
EDGES-A1 90
EDGES-A0 79
EDG_VID<11..0>
IMGW_EDGQ11 175
IMGW_EDGQ10 234
IMGW_EDGQ9 65
IMGW_EDGQ8 202
IMGW_EDGQ7 203
IMGW_EDGQ6 66
IMGW_EDGQ5 177
IMGW_EDGQ4 23
IMGW_EDGQ3 26
IMGW_EDGQ2 164
IMGW_EDGQ1 156
IMGW_EDGQ0 201
FX_TST 232
REC_OUT11 219
REC_OUT10 212
REC_OUT9 82
REC_OUT8 217
REC_OUT7 36
REC_OUT6 83
REC_OUT5 155
REC_OUT4 218
REC_OUT3 153
REC_OUT2 81
REC_OUT1 24
REC_OUT0 27
RECF_OUT03 170
RECF_OUT02 15
RECF_OUT01 14
RECF_OUT00 88
REC_VID_FX 4B3
4C3 7C7 8C8
REC_VID<15..0>
EDG_LUT_D11 97
EDG_LUT_D10 100
EDG_LUT_D9 196
EDG_LUT_D8 207
EDG_LUT_D7 206
EDG_LUT_D6 113
EDG_LUT_D5 216
EDG_LUT_D4 195
EDG_LUT_D3 93
EDG_LUT_D2 204
EDG_LUT_D1 109
EDG_LUT_D0 110
EDG_LUT_DB<15..0>
R64 10K
U32 TC551664 SPEED=15_NS
UB
LB
CS
14A5 EDG_LUT_WE* WR
14A5 EDG_LUT_OE* RD
64K X16 SRAM
A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0
EDG_LUT_ADR<15..0>
U42 74LCX16245
14A5 EDG_ABXEN* OE2
14C5 IP_RD_WR* DIR2 [BA]
DIR2 [AB]
OE1
DIR1 [AB]
DIR1 [BA]
A7 A6 A5 A4 A3 A2 A1 A0
B7 B6 B5 B4 B3 B2 B1 B0
2
1
BUFFER
IP_LUT_DB<15..0> 14A4
U40 74LCX16245
IP_ADR<15..0> 14C5
MANRS RECURSIVE FILTER, PT2
REALTIME EDGE ENHANCEMENT
OEC MEDICAL SYSTEMS, INC.
SIZE D
DWG NO. 00-879016
REV A4
SCALE:
SHEET 6
DRAWING LAST_MODIFIED=Wed Apr 5 13:11:13 2000
05-017-9/93



RECURSIVE FILTER MEMORY HISTOGRAM

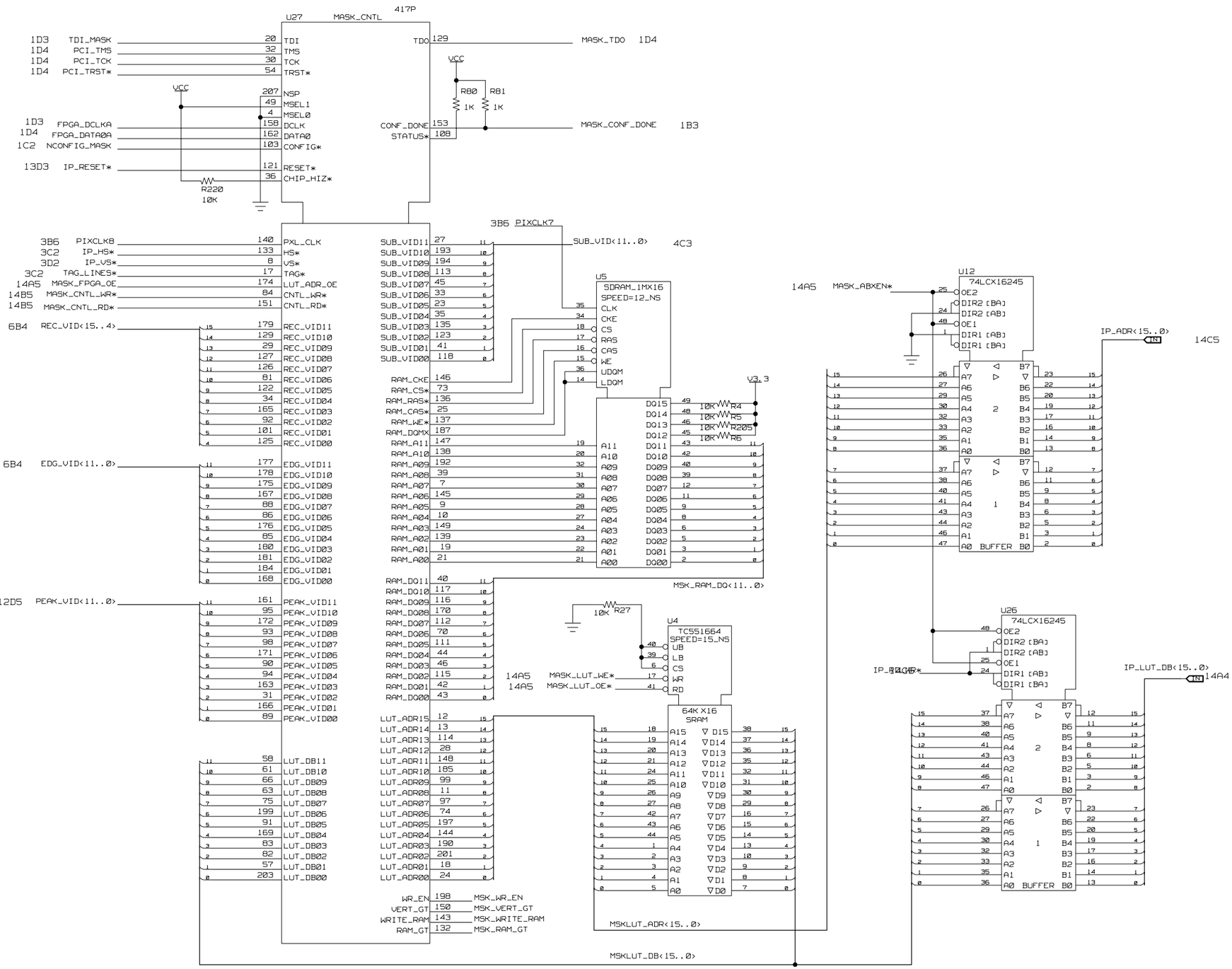
OEC MEDICAL SYSTEMS, INC.

SIZE	DWG NO.	REV
D	00-879016	A4

SCALE: | SHEET 7

DRAWING LAST_MODIFIED=Wed Apr 5 13:11:16 2000

05-017-9/93


U27 MASK_CNTL 417P
1D3 TDI_MASK 20 TDI
1D4 PCI_TMS 32 TMS
1D4 PCI_TCK 30 TCK
1D4 PCI_TRST* 54 TRST*
TDO 129 MASK_TDO 1D4
VCC
R80 1K
R81 1K
207 NSP
49 MSEL1
4 MSEL0
1D3 FPGA_DCLKA 158 DCLK
1D4 FPGA_DATA0A 162 DATA0
1C2 NCONFIG_MASK 103 CONFIG*
CONF_DONE 153
STATUS* 108
MASK_CONF_DONE 1B3
13D3 IP_RESET* 121 RESET*
36 CHIP_HIZ*
R220 10K
3B6 PIXCLK7
3B6 PIXCLK8 140 PXL_CLK
3C2 IP_HS* 133 HS*
3D2 IP_VS* 8 VS*
3C2 TAG_LINES* 17 TAG*
14A5 MASK_FPGA_OE 174 LUT_ADR_OE
14B5 MASK_CNTL_WR* 84 CNTL_WR*
14B5 MASK_CNTL_RD* 151 CNTL_RD*
SUB_VID11 SUB_VID10 SUB_VID09 SUB_VID08 SUB_VID07 SUB_VID06 SUB_VID05 SUB_VID04 SUB_VID03 SUB_VID02 SUB_VID01 SUB_VID00
SUB_VID<11..0> 4C3
6B4 REC_VID<15..4>
REC_VID11 REC_VID10 REC_VID09 REC_VID08 REC_VID07 REC_VID06 REC_VID05 REC_VID04 REC_VID03 REC_VID02 REC_VID01 REC_VID00
U5 SDRAM_1MX16 SPEED=12_NS
CLK CKE CS RAS CAS WE UDQM LDQM
RAM_CKE RAM_CS* RAM_RAS* RAM_CAS* RAM_WE* RAM_DQMX
V3.3
DQ15 DQ14 DQ13 DQ12 10K R4 10K R5 10K R205 10K R6
6B4 EDG_VID<11..0>
EDG_VID11 EDG_VID10 EDG_VID09 EDG_VID08 EDG_VID07 EDG_VID06 EDG_VID05 EDG_VID04 EDG_VID03 EDG_VID02 EDG_VID01 EDG_VID00
RAM_A11 RAM_A10 RAM_A09 RAM_A08 RAM_A07 RAM_A06 RAM_A05 RAM_A04 RAM_A03 RAM_A02 RAM_A01 RAM_A00
A11 A10 A09 A08 A07 A06 A05 A04 A03 A02 A01 A00
DQ11 DQ10 DQ09 DQ08 DQ07 DQ06 DQ05 DQ04 DQ03 DQ02 DQ01 DQ00
RAM_DQ11 RAM_DQ10 RAM_DQ09 RAM_DQ08 RAM_DQ07 RAM_DQ06 RAM_DQ05 RAM_DQ04 RAM_DQ03 RAM_DQ02 RAM_DQ01 RAM_DQ00
MSK_RAM_DQ<11..0>
12D5 PEAK_VID<11..0>
PEAK_VID11 PEAK_VID10 PEAK_VID09 PEAK_VID08 PEAK_VID07 PEAK_VID06 PEAK_VID05 PEAK_VID04 PEAK_VID03 PEAK_VID02 PEAK_VID01 PEAK_VID00
10K R27
U4 TC551664 SPEED=15_NS
UB LB CS WR RD
14A5 MASK_LUT_WE*
14A5 MASK_LUT_OE*
64K X16 SRAM
A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0
LUT_ADR15 LUT_ADR14 LUT_ADR13 LUT_ADR12 LUT_ADR11 LUT_ADR10 LUT_ADR09 LUT_ADR08 LUT_ADR07 LUT_ADR06 LUT_ADR05 LUT_ADR04 LUT_ADR03 LUT_ADR02 LUT_ADR01 LUT_ADR00
MSKLUT_ADR<15..0>
LUT_DB11 LUT_DB10 LUT_DB09 LUT_DB08 LUT_DB07 LUT_DB06 LUT_DB05 LUT_DB04 LUT_DB03 LUT_DB02 LUT_DB01 LUT_DB00
MSKLUT_DB<15..0>
WR_EN 198 MSK_WR_EN
VERT_GT 150 MSK_VERT_GT
WRITE_RAM 143 MSK_WRITE_RAM
RAM_GT 132 MSK_RAM_GT
14A5 MASK_ABXEN*
U12 74LCX16245
OE2 DIR2 [BA] DIR2 [AB] OE1 DIR1 [AB] DIR1 [BA]
A7 A6 A5 A4 A3 A2 A1 A0
B7 B6 B5 B4 B3 B2 B1 B0
BUFFER
IP_ADR<15..0>
14C5
U26 74LCX16245
IP_LUT_DB<15..0>
14A4

MASK MEMORY

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OEC MEDICAL SYSTEMS, INC.

SIZE	DWG NO.	REV
D	00-879016	A4
SCALE:		SHEET 8

05-017-9/93

U59 BITMEM_CNTL

1C3 TDI_BIT 63 TDI
1D4 PCI_TMS 64 TMS
1D4 PCI_TCK 116 TCK
1D4 PCI_TRST* 175 TRST*
239 SPLIT_EN
237 NSP
38 MSEL1
19 MSEL0
1D3 FPGA_DCLKB 183 DCLK
1D4 FPGA_DATA0B 187 DATA0
1C2 NCONFIG_BIT 120 CONFIG*
13D3 IP_RESET* 49 RESET*
131 CHIP_HIZ*

TDO 117 BIT_TDO 1C4
CONF_DONE 161 BIT_CONF_DONE 1C3
STATUS* 142

VCC R228 10K R62 75
VCC R135 1K R100 1K
VCC R243 10K

3B6 PIXCLK4 8 PXL_CLK
3D2 IP_VS* 35 IP_VS*
3C2 IP_HS* 217 IP_HS*
14B5 BIT_REG_CS* 69 REG_CS*
14B5 BIT_MEM_CS* 210 MEM_CS*
14C5 IP_RD_WR* 1 IP_RD_WR*
13B2 FIFO_FFB* 81 FIFO_FF*
13B2 FIFO_AFB* 104 FIFO_AF*
13B2 FIFO_EFB* 103 FIFO_EF*
13B2 FIFO_AEB* 196 FIFO_AE*

FIFO_EN 177 BIT_FIFO_ENB 14C3

HI_RES7 200 TAG_DATA<7..0> 3C5
HI_RES6 218
HI_RES5 224
HI_RES4 219
HI_RES3 83
HI_RES2 132
HI_RES1 154
HI_RES0 22

13B2 IN IP_DB_BE<1..0>* 238 BE1* 197 BE0*

14C5 IN IP_ADR<18..16> IP_ASIC_ADR<15..0> 14B4 IN
199 IP_ADR18
106 IP_ADR17
194 IP_ADR16
193 IP_ADR15
164 IP_ADR14
223 IP_ADR13
87 IP_ADR12
76 IP_ADR11
111 IP_ADR10
206 IP_ADR09
112 IP_ADR08
107 IP_ADR07
98 IP_ADR06
77 IP_ADR05
216 IP_ADR04
88 IP_ADR03
229 IP_ADR02
172 IP_ADR01
97 IP_ADR00

IP_DB<31..0> 13B2 IN
156 IP_DB15
159 IP_DB14
155 IP_DB13
153 IP_DB12
21 IP_DB11
41 IP_DB10
135 IP_DB09
134 IP_DB08
48 IP_DB07
109 IP_DB06
72 IP_DB05
227 IP_DB04
80 IP_DB03
79 IP_DB02
220 IP_DB01
213 IP_DB00

PRI_HIRES1 99 PRI_TXT&G1 10C4
PRI_HIRES0 43 PRI_TXT&G0 10C4
PRI_LORES2 182 PRI_MASK 10C4
PRI_LORES1 211 PRI_WE 10B4
PRI_LORES0 138 PRI_SPF 10B4

SEC_HIRES1 189 SEC_TXT&G1 10B4
SEC_HIRES0 215 SEC_TXT&G0 10B4
SEC_LORES2 89 SEC_MASK 10B4
SEC_LORES1 56 SEC_WE 10B4
SEC_LORES0 46 SEC_SPF 10B4

VCC R152 10K R153 10K

COMP_GT 37 BM_COMP_GT
RAMX_DSF 2
RAM1_RAS* 176
RAM1_CAS* 180
RAMX_WEU* 188
RAMX_WEL* 179
RAMX_TRG* 181
RAMX_DSF 86
SC_CLK 143
RAM1_SE* 47
RAM2_RAS* 240
RAM2_CAS* 82
RAM2_SE* 93

U61 VRAM 256KX16
U60 VRAM 256KX16
RAS CAS WEU WEL TRG DSF SC SE QSF
A8 A7 A6 A5 A4 A3 A2 A1 A0
SQ15 SQ14 SQ13 SQ12 SQ11 SQ10 SQ09 SQ08 SQ07 SQ06 SQ05 SQ04 SQ03 SQ02 SQ01 SQ00
DQ15 DQ14 DQ13 DQ12 DQ11 DQ10 DQ09 DQ08 DQ07 DQ06 DQ05 DQ04 DQ03 DQ02 DQ01 DQ00
NC

BIT_RAMX_A<11..0>
RAMX_A08 207
RAMX_A07 222
RAMX_A06 137
RAMX_A05 231
RAMX_A04 150
RAMX_A03 68
RAMX_A02 203
RAMX_A01 149
RAMX_A00 147

RAMX_DQ15 24
RAMX_DQ14 27
RAMX_DQ13 25
RAMX_DQ12 23
RAMX_DQ11 158
RAMX_DQ10 44
RAMX_DQ09 42
RAMX_DQ08 133
RAMX_DQ07 45
RAMX_DQ06 139
RAMX_DQ05 225
RAMX_DQ04 166
RAMX_DQ03 74
RAMX_DQ02 66
RAMX_DQ01 234
RAMX_DQ00 226

LO_RES7 31 HIST_ROI1 5A6
LO_RES5 122 HIST_ROI3 5A6
LO_RES4 58 HIST_ROI2 5A6
LO_RES3 124 HIST_ROI0 5A6
LO_RES1 65 HIST_ROI5 5A6
LO_RES0 121 HIST_ROI4 5A6

BIT_RAMX_DQ<15..0>
BIT_RAMX_SQ<15..0>

SQ15 145 SQ14 102 SQ13 34 SQ12 146 SQ11 32 SQ10 148 SQ09 157 SQ08 20 SQ07 36 SQ06 113 SQ05 30 SQ04 144 SQ03 212 SQ02 33 SQ01 26 SQ00 160

358P

U59 PART OF BITMEM_CNTL

R117 10K

XTRST* 175 XBAR_TRST* 4D4
XTCK 202 XBAR_TCK 4D4
XTMS 55 R229 33.2 XBAR_TMS 4D4
XTDI 52 XBAR_TDI 4D4

3D3 IP_VB_IRQ* 54 VB*
14A7 XBAR_CNTL_WR* 128 XREG_WR*
14A7 XBAR_CNTL_RD* 105 XREG_RD*
14A7 XBAR_FPGA_OE 100 XFPGA_OE

XRAM_ADR14 15
XRAM_ADR13 14
XRAM_ADR12 13
XRAM_ADR11 12
XRAM_ADR10 11
XRAM_ADR09 10
XRAM_ADR08 9
XRAM_ADR07 16
XRAM_ADR06 165
XRAM_ADR05 195
XRAM_ADR04 167
XRAM_ADR03 168
XRAM_ADR02 169
XRAM_ADR01 170
XRAM_ADR00 171

XBAR_ADR<14..0>

84 XRAM_DB07
53 XRAM_DB06
123 XRAM_DB05
127 XRAM_DB04
126 XRAM_DB03
57 XRAM_DB02
59 XRAM_DB01
125 XRAM_DB00

XBAR_DB<7..0>

U67 SRAM_32KX8 SPEED=15_NS
WE CE OE

14A7 XBAR_RAM_WE*
14A7 XBAR_RAM_OE*
R140 10K

A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
I/O 7 I/O 6 I/O 5 I/O 4 I/O 3 I/O 2 I/O 1 I/O 0

U50 74LCX16245
14A7 XBAR_ABXEN*
14C5 IP_RD_WR*
OE DIR [AB] DIR [BA]
A B

IP_LUT_DB<7..0> IN 14A4

U38 74LCX16245
OE2 DIR2 [BA] DIR2 [AB] OE1 DIR1 [AB] DIR1 [BA]
A7 A6 A5 A4 A3 A2 A1 A0 2
B7 B6 B5 B4 B3 B2 B1 B0
A7 A6 A5 A4 A3 A2 A1 A0 1
B7 B6 B5 B4 B3 B2 B1 B0
BUFFER

IP_ADR<18..0> IN 14C5

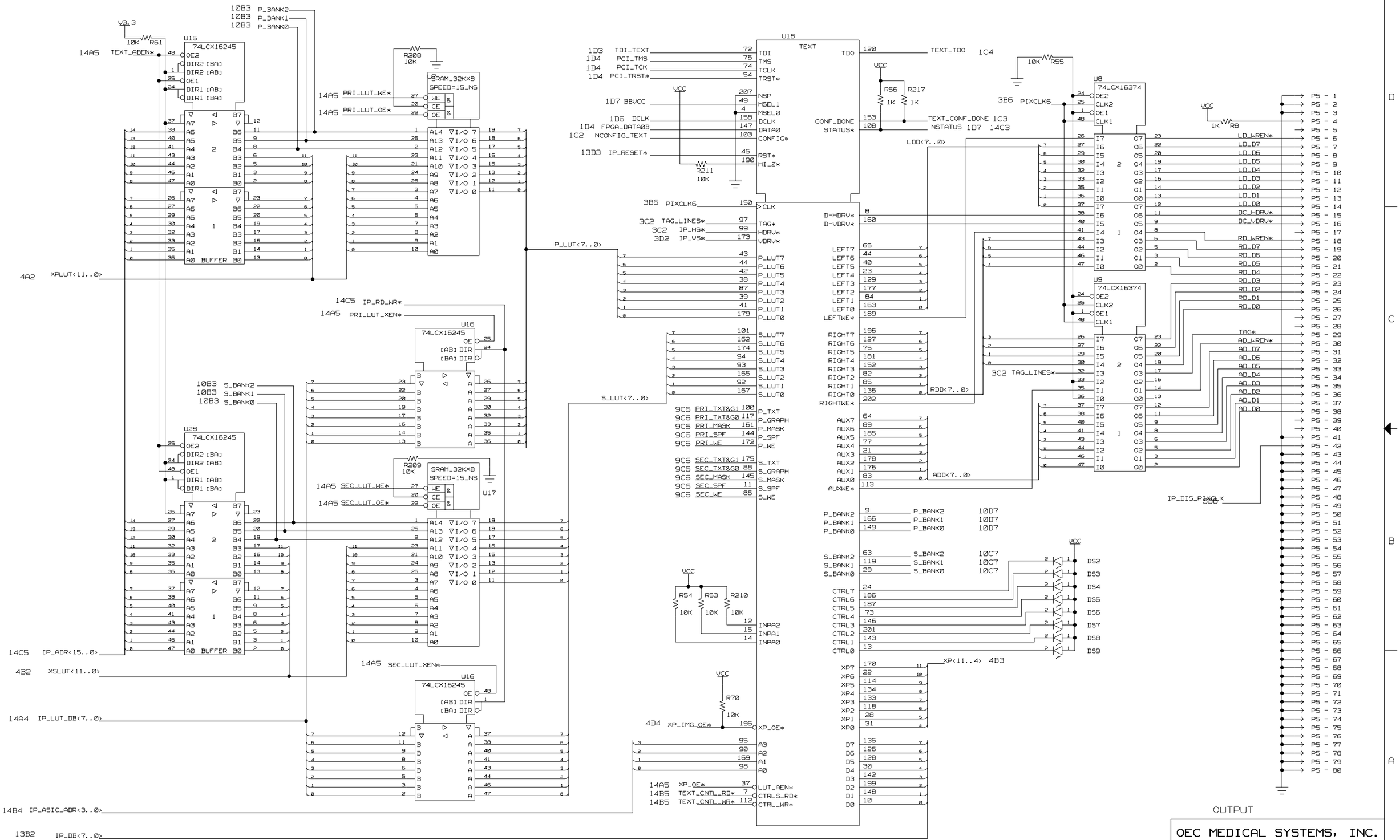
BITPLANE MEMORY / XBAR JTAG RAM

OEC MEDICAL SYSTEMS, INC.

SIZE D | DWG NO. 00-879016 | REV A4 | SCALE: | SHEET 9

DRAWING LAST_MODIFIED=Wed Apr 5 13:11:20 2000

05-017-9/93



OUTPUT

OEC MEDICAL SYSTEMS, INC.

SIZE	DWG NO.	REV
D	00-879016	A4
SCALE:		SHEET 10

DRAWING LAST_MODIFIED=Wed Apr 5 13:11:25 2000

05-017-9/93

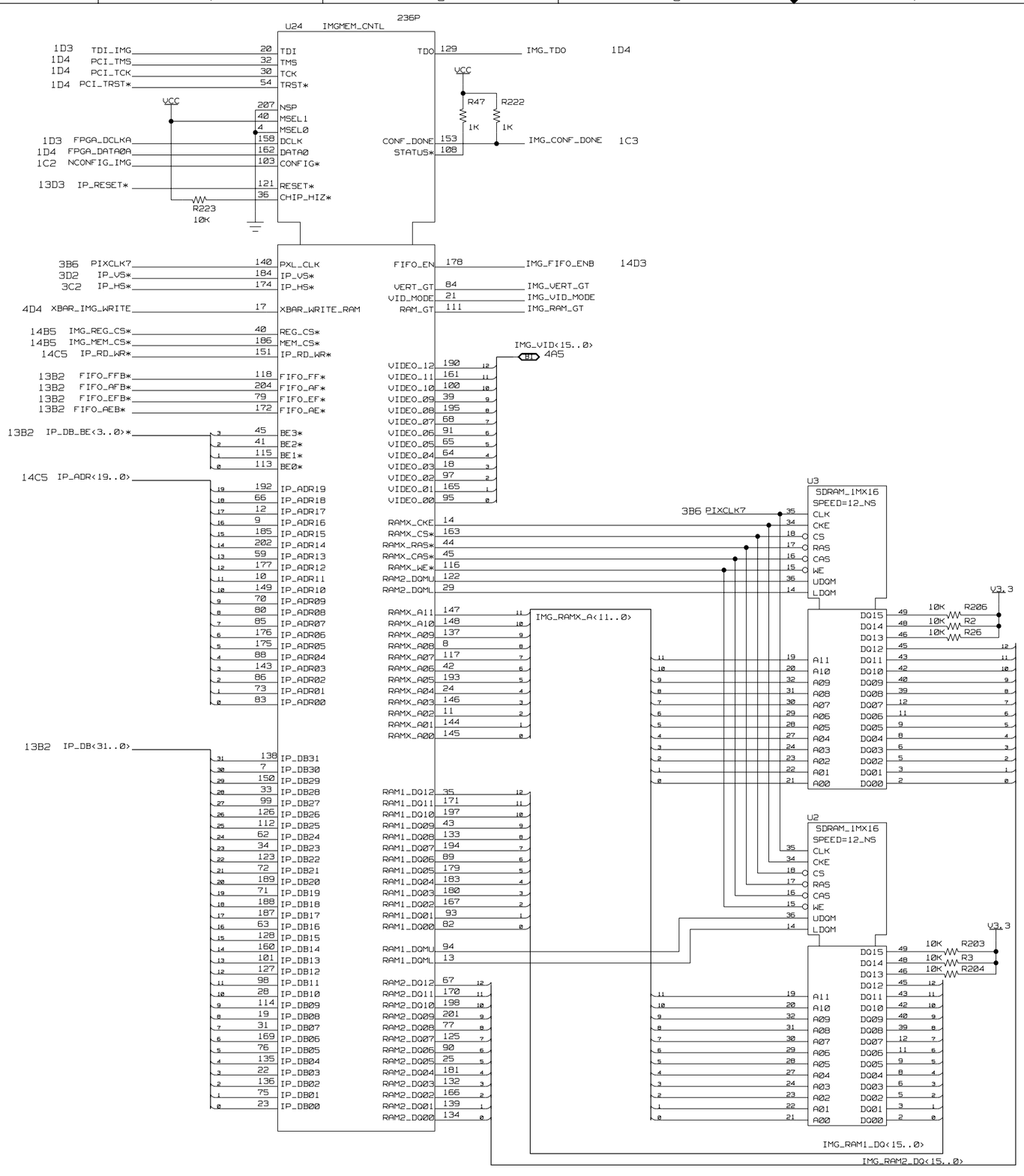


IMAGE MEMORY

OEC MEDICAL SYSTEMS, INC.

SIZE	DWG NO.	REV
D	00-879016	A4
SCALE:		SHEET 11

DRAWING LAST_MODIFIED=Wed Apr 5 13:11:28 2000

05-017-9/93

341P

U48 PEAK

1D3 TDI_PEAK — 20 TDI
1D4 PCI_TMS — 32 TMS
1D4 PCI_TCK — 30 TCK
1D4 PCI_TRST* — 54 TRST*
TDO 129 — PEAK_TDO 1D4

VCC
R105 1K
R88 1K

207 NSP
49 MSEL1
4 MSEL0
1D3 FPGA_DCLKA — 158 DCLK
1D4 FPGA_DATA0A — 162 DATA0
1C2 NCONFIG_PEAK — 103 CONFIG*
CONF_DONE 153
STATUS* 108
PEAK_CONF_DONE 1C3

13D3 IP_RESET* — 121 RESET*
36 CHIP_HIZ*

VCC
R127 10K

3B6 PIXCLK2 — 140 PXL_CLK
3D2 IP_V5* — 41 IP_V5*
3C2 IP_HS* — 93 IP_HS*
3C2 TAG_LINES* — 145 TAG*
4D3 PEAK_IN<11..0> — VID_IN11..VID_IN00
TEST_VID 144 — PEAK_VID_FX 4B3
VID_OUT11..VID_OUT00 — PEAK_VID<11..0> 4D5 8B8

LUT_DB15..LUT_DB00
LUT_ADR15..LUT_ADR00 — PK_LUT_ADR<15..0>

RAM1_DQ15..RAM1_DQ00
RAM1_CKE 170
RAM1_CS* 45
RAM1_RAS* 12
RAM1_CAS* 123
RAM1_WE* 171
RAM1_DQMX 193
RAM1_A11..RAM1_A00 — PK_RAM1_A<11..0>

RAM2_DQ15..RAM2_DQ00
RAM2_CKE 148
RAM2_CS* 165
RAM2_RAS* 112
RAM2_CAS* 63
RAM2_WE* 111
RAM2_DQMX 95
RAM2_A11..RAM2_A00 — PK_RAM2_A<11..0>

14B5 PEAK_CNTL_WR* — 163 CNTL_WR*
14B5 PEAK_FPGA_OE — 150 LUT_ADR_OE
PK_R1_GT — 10 R1_GT
PK_R2_GT — 9 R2_GT
TEST PADS PK_WR_EN — 14 WR_EN
PK_READ_1 — 138 READ_1
PK_VERT_GT — 46 VERT_GT
PCI_DB7..PCI_DB0 — PK_DB<7..0>

PK_R2DQ<15..0>
PK_R1DQ<15..0>

U33 SDRAM_1MX16 SPEED=12_NS
CLK, CKE, CS, RAS, CAS, WE, UDQM, LDQM
A11..A00, DQ15..DQ00

U47 SDRAM_1MX16 SPEED=12_NS
CLK, CKE, CS, RAS, CAS, WE, UDQM, LDQM
A11..A00, DQ15..DQ00

R126 10K

U55 TC551664 SPEED=15_NS
UB, LB, CS, WR, RD
64K X16 SRAM
A15..A0, D15..D0

14B5 PEAK_LUT_WE*
14B5 PEAK_LUT_OE*

PKLUTDB<15..0>

U34 74LCX16245
14B5 PEAK_ABXEN* — OE2, OE1
DIR2 [BA], DIR2 [AB], DIR1 [AB], DIR1 [BA]
A7..A0, B7..B0, BUFFER
IP_ADR<15..0> IN 14C5

U35 74LCX16245
14A7 PEAK_DBXEN* — OE2, OE1
14C5 IP_RD_WR* — DIR2 [BA], DIR2 [AB], DIR1 [AB], DIR1 [BA]
A7..A0, B7..B0, BUFFER

VCC
R83 10K

U43 74LCX16245
OE, [AB] DIR, [BA] DIR
B..A
PEAK_CNTL_RD* IN 14B5
IP_LUT_DB<15..0> IN 14A4

PEAK / FILTER

OEC MEDICAL SYSTEMS, INC.

SIZE D | DWG NO. 00-879016 | REV A4 | SCALE: | SHEET 12

DRAWING LAST_MODIFIED=Wed Apr 5 13:11:31 2000

05-017-9/93

P1 - B7 ← INTB#
P1 - B8 ← INTD#
P1 -B10 ← RESERVED
P1 -B14 ← RESERVED
P1 -B18 ← REQ#
P1 -B60 ← ACK64#
P1 - A7 ← INTC#
P1 - A9 ← RESERVED
P1 -A11 ← RESERVED
P1 -A14 ← RESERVED
P1 -A17 ← GNT#
P1 -A19 ← RESERVED
P1 -A40 ← SDONE
P1 -A41 ← SBO#
P1 -A60 ← REQ64#
P1 - A1 ← IN_PCI_TRST* 1D5
P1 - B2 ← IN_PCI_TCK 1D5
P1 - A3 ← IN_PCI_TMS 1D5
P1 - A4 ← PCI_TDI 1D4
P1 - B4 ← PCI_TDO 1C3
P1 - B9 ← PRSNT1n
P1 -B11 ← PRSNT2n
25W MAX

VCC
C173 0.01 C187 0.01 C767 0.01 C87 0.01 C716 0.01 C675 0.01 C678 0.01 C14 0.01

TP11 RED

P1 - B5 ← PCI_+5V
P1 - B6 ← PCI_+5V
P1 -B61 ← PCI_+5V
P1 -B62 ← PCI_+5V
P1 - A5 ← PCI_+5V
P1 - A8 ← PCI_+5V
P1 -A61 ← PCI_+5V
P1 -A62 ← PCI_+5V
C174 68 6.3V
C775 0.1 C718 0.01 C771 0.1
C679 0.1 C715 0.1 C770 0.1 C774 0.1 C766 0.01 C677 0.1 C765 0.1
PCI_+5V → OUT 1D6 13C6

P1 -B19 ← PCI_+5V_IO
P1 -B59 ← PCI_+5V_IO
P1 -A10 ← PCI_+5V_IO
P1 -A16 ← PCI_+5V_IO
P1 -A59 ← PCI_+5V_IO

P1 -B25 ← PCI_+3.3V
P1 -B31 ← PCI_+3.3V
P1 -B36 ← PCI_+3.3V
P1 -B41 ← PCI_+3.3V
P1 -B43 ← PCI_+3.3V
P1 -B54 ← PCI_+3.3V
P1 -A21 ← PCI_+3.3V
P1 -A27 ← PCI_+3.3V
P1 -A33 ← PCI_+3.3V
P1 -A39 ← PCI_+3.3V
P1 -A45 ← PCI_+3.3V
P1 -A53 ← PCI_+3.3V

P1 - B1 ← PCI_-12V
P1 - A2 ← PCI_+12V
C186 0.1 C185 0.1 C769 0.1 C773 0.1

P1 - B3 ← PCI_GND
P1 -B12 ← PCI_GND
P1 -B13 ← PCI_GND
P1 -B15 ← PCI_GND
P1 -B17 ← PCI_GND
P1 -B22 ← PCI_GND
P1 -B28 ← PCI_GND
P1 -B34 ← PCI_GND
P1 -B38 ← PCI_GND
P1 -B46 ← PCI_GND
P1 -B49 ← PCI_GND
P1 -B57 ← PCI_GND
P1 -A12 ← PCI_GND
P1 -A13 ← PCI_GND
P1 -A18 ← PCI_GND
P1 -A24 ← PCI_GND
P1 -A30 ← PCI_GND
P1 -A35 ← PCI_GND
P1 -A37 ← PCI_GND
P1 -A42 ← PCI_GND
P1 -A48 ← PCI_GND
P1 -A56 ← PCI_GND

R136 10K
U65 NM93CS46
VCC 8, PE 6, PRE 7
SK 2 ← 144 EESK
CS 1 ← 142 EECS
DI 3 ← 145 EEDI
DO 4 → 143 EEDO
R245 10K
R244 10K

U66 PCI9050 469P
VCC 146
TEST 99
MODE 68

P1 -A15 ← RSTn 148 → RST
P1 -B16 ← CLK 149 → CLK
P1 -B39 ← LOCKn 18 → LOCK
P1 - A6 ← INTAn 44 → INTA
P1 -A43 ← PAR 21 → PAR
P1 -B40 ← PERRn 19 → PERR
P1 -B42 ← SERRn 20 → SERR
P1 -A26 ← IDSEL 159 → IDSEL
P1 -A34 ← FRAMEn 13 → FRAME
P1 -B35 ← IRDYn 14 → IRDY
P1 -A36 ← TRDYn 15 → TRDY
P1 -A38 ← STOPn 17 → STOP
P1 -B37 ← DEVSELn 16 → DEVSEL
P1 -B26 ← C_BEN3 158 → C/BE3
P1 -B33 ← C_BEN2 12 → C/BE2
P1 -B44 ← C_BEN1 22 → C/BE1
P1 -A52 ← C_BEN0 33 → C/BE0

P1 -B20 ← AD31 150 → AD31
P1 -A20 ← AD30 151 → AD30
P1 -B21 ← AD29 152 → AD29
P1 -A22 ← AD28 153 → AD28
P1 -B23 ← AD27 154 → AD27
P1 -A23 ← AD26 155 → AD26
P1 -B24 ← AD25 156 → AD25
P1 -A25 ← AD24 157 → AD24
P1 -B27 ← AD23 2 → AD23
P1 -A28 ← AD22 3 → AD22
P1 -B29 ← AD21 4 → AD21
P1 -A29 ← AD20 5 → AD20
P1 -B30 ← AD19 6 → AD19
P1 -A31 ← AD18 7 → AD18
P1 -B32 ← AD17 8 → AD17
P1 -A32 ← AD16 11 → AD16
P1 -A44 ← AD15 23 → AD15
P1 -B45 ← AD14 24 → AD14
P1 -A46 ← AD13 25 → AD13
P1 -B47 ← AD12 28 → AD12
P1 -A47 ← AD11 29 → AD11
P1 -B48 ← AD10 30 → AD10
P1 -A49 ← AD9 31 → AD9
P1 -B52 ← AD8 32 → AD8
P1 -B53 ← AD7 34 → AD7
P1 -A54 ← AD6 35 → AD6
P1 -B55 ← AD5 36 → AD5
P1 -A55 ← AD4 37 → AD4
P1 -B56 ← AD3 38 → AD3
P1 -A57 ← AD2 39 → AD2
P1 -B58 ← AD1 42 → AD1
P1 -A58 ← AD0 43 → AD0

LRESET 132 ← OUT IP_RESET* 3D5 5D6 6D6 7D7 8D8 9D8 10D5 11D7 12D8 14D3 14D7
BCLKO 63
LCLK 135 ← IN PIXCLK 3B6
LINTI2 136
LINTI1 137 ← IN IP_INTR* 7D5
LHOLD 134
LHOLDA 133

LW/RN 127 ← OUT PLX_LWR_RD* 14C3 14C7
WR 125 ← OUT PLX_WR*
RD 126 ← OUT PLX_RD*
BTERM 129 → IN PLX_BTERM* 14C1
LRDYI 128 → IN PLX_LRDY* 14C1
BLAST 124 ← OUT PLX_BLAST*
ADS 123 ← OUT PLX_ADS* 14C3 14C7
ALE 64
USER1
LLOCK 139
USER0
WAIT0 138 ← OUT PLX_LWAIT*
USER3
CS3 141 ← OUT EXT_FIFO_RESET* 14A7
USER2
CS2 140 ← OUT EMPTY_IRQ_EN 7C7
CS1 131 ← OUT PLX_LC51*
CS0 130 ← OUT PLX_LC50* 14C3 14C7

LA27 122
LA26 119
LA25 118
LA24 117 ← OUT PLX_LA<24..2> 14C7
LA23 116
LA22 115
LA21 114
LA20 113
LA19 112
LA18 111
LA17 110
LA16 109
LA15 108
LA14 107
LA13 106
LA12 105
LA11 102
LA10 101
LA9 100
LA8 98
LA7 97
LA6 96
LA5 95
LA4 94
LA3 93
LA2 92

LBE3 45
LBE2 46
LBE1 47
LBE0 48

LAD31 52
LAD30 53
LAD29 54
LAD28 55
LAD27 56
LAD26 57
LAD25 58
LAD24 59
LAD23 60
LAD22 61
LAD21 62
LAD20 69
LAD19 70
LAD18 71
LAD17 72
LAD16 73
LAD15 74
LAD14 75
LAD13 76
LAD12 77
LAD11 78
LAD10 79
LAD9 82
LAD8 83
LAD7 84
LAD6 85
LAD5 86
LAD4 87
LAD3 88
LAD2 89
LAD1 90
LAD0 91

PLX_LBE<3..0>
10K R251 R150 R149 R250 R148 R249 R147 R248 R145 R247 R144 R246 R151 R139 R146 R143 R110 R133 R108 R134 R111 R107 R109 R113 R112 R95 R94 R93 R132 R131 R130 R129
PLX_LAD<31..0>

VCC
R75 R128 R226 R238 R239 R230 R82 R221 10K
TP12 WHT
TP13 WHT

U57 FIFO 1024X36X2 BMBS SPEED=20_NS
14C1 FIFO_A2A → A2A
14C1 FIFO_A1A → A1A
14C1 FIFO_A0A → A0A
14A7 FIFO_RESET* → RS
A0B → WS1 → IN FIFO_WS1 14A7
WS0 → IN FIFO_WS0 14A7
CKA
REQA → IN FIFO_REQA 14C5
14C1 FIFO_RD_WRA* → R/WnA
14C1 FIFO_ENA → ENA
14C1 FIFO_OEA* → OEA
CKB
REQB → IN FIFO_REQB 14C5
R/WnB → IN FIFO_RD_WRB* 14D5
ENB → IN FIFO_ENB 14D1
OEB → IN FIFO_OEB* 14D5
PFA
PFB
RT2
RT1
14C3 FIFO_FFA* → OUT FFA1
14C3 FIFO_AFA* → OUT AF1
FF2 → FIFO_FFB* 9C8 11C7
AF2 → FIFO_AFB* 9C8 11C7 14C7
HF1
HF2
14C3 FIFO_EFA* → OUT EF2
14C3 FIFO_AEA* → OUT AE2
EF1 → FIFO_EFB* 9C8 11C7 14C7
AE1 → FIFO_AEB* 9C8 11C7 14C7
MBF2
MBF1
ACKA
ACKB

D35A D35B → OUT IP_DB_BE<3..0>* 9C8 11C7
D34A D34B
D33A D33B
D32A D32B
D31A D31B
D30A D30B
D29A D29B
D28A D28B
D27A D27B
D26A D26B
D25A D25B
D24A D24B
D23A D23B
D22A D22B
D21A D21B
D20A D20B
D19A D19B
D18A D18B
D17A D17B
D16A D16B
D15A D15B
D14A D14B
D13A D13B
D12A D12B
D11A D11B
D10A D10B
D9A D9B
D8A D8B
D7A D7B
D6A D6B
D5A D5B
D4A D4B
D3A D3B
D2A D2B
D1A D1B
D0A D0B → OUT IP_DB<31..0> 3A4 5C5 6D4 7D2 9B8 10A8 11B7 14A3

DRAWING
LAST_MODIFIED=Wed Apr 5 13:11:36 2000

PCI BUS INTERFACE

OEC MEDICAL SYSTEMS, INC.

SIZE	DWG NO.	REV
D	00-879016	A4
SCALE:		SHEET 13

05-017-9/93

U36 FIFO_CNTL

1D3 TDI_FIFO_C → 20 TDI
1D4 PCI_TMS → 32 TMS
1D4 PCI_TCK → 30 TCK
1D4 PCI_TRST* → 54 TRST*
TDO 129 → FIFO_C_TDO 1D4
VCC → 207 NSP
VCC → 49 MSEL1
4 MSEL0
1D3 FPGA_DCLKA → 158 DCLK
1D4 FPGA_DATA0A → 162 DATA0
1C2 NCONFIG_FIFO_C → 103 CONFIG*
CONF_DONE 153 → FIFO_C_CONF_DONE 1C3
STATUS* 108
13D3 IP_RESET* → 121 RESET*
36 CHIP_HIZ*

VCC → R78 1K, R115 1K
R231 10K
3V3 → R96 10K, R137 10K, R89 1K

3B6 PIXCLK2 → 140 PXL_CLK

FIFO_OE* 175 → FIFO_OEB* 13C2
FIFO_RD_WR* 174 → FIFO_RD_WRB* 13C2
FIFO_REQ 95 → FIFO_REQB 13C2
FIFO_EN 203
FIFO_GATE 149
A_SM_ENABLE 40
WR_EMPTY_INTR* 80 → FIFO_EMPTY_IRQ* 7C7
IP_RD_WR* 88 → OUT IP_RD_WR* 5C3 5D3 6D3 8B4 9C2 9C8 10C6 11C7 12C3

13B2 FIFO_AFB* → 39 FIFO_AF*
13B2 FIFO_EFB* → 151 FIFO_EF*
13B2 FIFO_AEB* → 117 FIFO_AE*

13C3 PLX_LCS0* → 150 LCS*
13D3 PLX_ADS* → 17 ADS*
13D3 PLX_LWR_RD* → 138 LWR_RD*

13C4 PLX_LA<24..2>

24	148	LA22
23	10	LA21
22	170	LA20
21	120	LA19
20	7	LA18
19	86	LA17
18	29	LA16
17	181	LA15
16	172	LA14
15	34	LA13
14	35	LA12
13	99	LA11
12	161	LA10
11	122	LA09
10	165	LA08
9	19	LA07
8	22	LA06
7	134	LA05
6	25	LA04
5	98	LA03
4	101	LA02
3	100	LA01
2	136	LA00

IP_ADR19 197 … IP_ADR00 14 → 19 … 0
OUT 5C1 6C2 8C3 9A2 9C8 10B8 11C7 12C2 IP_ADR<19..0>

IMG_MEM_CS* 81 → IMG_MEM_CS* 11C7
IMG_REG_CS* 139 → IMG_REG_CS* 11C7
BIT_MEM_CS* 179 → BIT_MEM_CS* 9C8
BIT_REG_CS* 180 → BIT_REG_CS* 9D8
NREG_WR0* 58 → ISC_CNTL_WR* 3B5
NREG_RD0* 83 → ISC_CNTL_RD* 3B5
NREG_WR1* 184 → FM_CNTL_WR* 7A7
NREG_RD1* 82 → FM_CNTL_RD* 7A7
NREG_WR2* 135 → EDG_CNTL_WR* 6C6
NREG_RD2* 177 → EDG_CNTL_RD* 6C6
NREG_WR3* 133 → MANR5_CNTL_WR* 5C6
NREG_RD3* 116 → MANR5_CNTL_RD* 5C6
NREG_WR4* 185 → TEXT_CNTL_WR* 10A4
NREG_RD4* 114 → TEXT_CNTL_RD* 10A4
NREG_WR5* 18 → HST_WR* 7C3
NREG_RD5* 74 → HST_RD* 7C3
NREG7_WR0* 45 → HST_LD* 7C3
NREG7_WR1* 118 → HST_FC* 7C3
LREG_WR0* 57 → PEAK_CNTL_WR* 12A8
LREG_RD0* 73 → PEAK_CNTL_RD* 12B2
LFPGA_OE0 111 → PEAK_FPGA_OE 12A8
LRAM_WE0* 93 → PEAK_LUT_WE* 12D4
LRAM_OE0* 176 → PEAK_LUT_OE* 12D4
LABXEN0* 43 → PEAK_ABXEN* 12D3
LREG_WR1* 145 → MASK_CNTL_WR* 8C8
LREG_RD1* 187 → MASK_CNTL_RD* 8C8
LFPGA_OE1 47 → MASK_FPGA_OE 8C8
LRAM_WE1* 188 → MASK_LUT_WE* 8B5
LRAM_OE1* 56 → MASK_LUT_OE* 8B5
LABXEN1* 112 → MASK_ABXEN* 8C4
LFPGA_OE3 41 → EDG_FPGA_OE 6D5
LRAM_WE3* 71 → EDG_LUT_WE* 6C4
LRAM_OE3* 97 → EDG_LUT_OE* 6C4
LABXEN3* 90 → EDG_ABXEN* 6D3
DLFPGA_OE0 146 → MANR5_FPGA_OE 5C6
DLABEN0* 169 → MANR5_ABEN* 5D2
DLRAM_WE0* 91 → MANR5_LUT1_WE* 5B4
DLRAM_OE0* 84 → MANR5_LUT1_OE* 5B4
DLRAM_XEN0* 171 → MANR5_LUT1_XEN* 5C3
DLRAM_WE1* 168 → MANR5_LUT2_WE* 5D4
DLRAM_OE1* 123 → MANR5_LUT2_OE* 5D4
DLRAM_XEN1* 205 → MANR5_LUT2_XEN* 5D3
DLFPGA_OE1* 8 → XP_OE* 4D4 10A4
DLABEN1* 93 → TEXT_ABEN* 10D8
DLRAM_WE2* 167 → PRI_LUT_WE* 10D6
DLRAM_OE2* 61 → PRI_LUT_OE* 10D6
DLRAM_XEN2* 204 → PRI_LUT_XEN* 10C6
DLRAM_WE3* 94 → SEC_LUT_WE* 10B6
DLRAM_OE3* 125 → SEC_LUT_OE* 10B6
DLRAM_XEN3* 44 → SEC_LUT_XEN* 10A6

9D5 XBAR_CNTL_WR* OUT → 113 LREG_WR2*
9D5 XBAR_CNTL_RD* OUT → 186 LREG_RD2*
9C3 XBAR_RAM_WE* OUT → 189 LRAM_WE2*
9C3 XBAR_RAM_OE* OUT → 202 LRAM_OE2*
9C2 XBAR_ABXEN* OUT → 115 LABXEN2*
9D5 XBAR_FPGA_OE OUT → 42 LFPGA_OE2
12C3 PEAK_DBXEN* OUT → 89 LDBXEN0*

13C2 FIFO_WS1 OUT → 68 FIFO_WS1
13C2 FIFO_WS0 OUT → 147 FIFO_WS0
13C3 FIFO_RESET* OUT → 9 FIFO_RESET*
13C3 EXT_FIFO_RESET* OUT → 85 EXT_FIFO_RESET*
14C1 FIFO_ENA → 163 FIA_EN

33 LUTGRP_READ

U23 74LCX16245
OE2 25
[BA] DIR2 25
[AB] DIR2 24
OE1 48
[AB] DIR1 1
[BA] DIR1
B7 23 … B0 15 ↔ A7 26 … A0 38
BUFFER

IP_ASIC_ADR<15..0>
OUT 3B5 5D6 6C6 7A7 9C8 10A8

R69 10K
R79 10K

U37 74LCX16245
25 OE2
DIR2 [BA]
24 DIR2 [AB]
48 OE1
1 DIR1 [AB]
DIR1 [BA]
A7 26 … A0 38 ↔ B7 23 … B0 15
BUFFER

10A8 9C1 8B3 6D2 5B1 12A2 IP_LUT_DB<15..0> OUT
IP_DB<15..0> IN 13B2

R90 10K

U49 CONFIG

13D3 IP_RESET* → 1 RESET*
3B6 PIXCLK2 → 43 PXL_CLK
44 CHIP_HIZ
R92 10K

11D5 IMG_FIFO_ENB → 8 IMG_FIFO_ENB
9D5 BIT_FIFO_ENB → 40 BIT_FIFO_ENB
21 FC_FIFO_ENB
41 FC_FIFO_ENB_GATE
19 SM_ENABLE

13C3 PLX_LCS0* → 12 LCS0*
13D3 PLX_ADS* → 39 ADS*
1D7 NCONFIG → 20 CONFIG*
13D3 PLX_LWR_RD* → 16 LWR_RD*

7 FIFO_FFA*
5 FIFO_AFA*
6 FIFO_EFA*
18 FIFO_AEA*
1D7 38 BBVCC
10D3 1D7 17 NSTATUS01

FIFO_ENB 36 → FIFO_ENB 13C2
CONFIG1* 14 → NCONFIG1 1C3
FIFO_OEA* 25 → FIFO_OEA* 13C3
FIFO_RD_WRA* 24 → FIFO_RD_WRA* 13C3
FIFO_ENA* 34 → FIFO_ENA 13C3 14A7
FIFO_A2A 29 → FIFO_A2A 13C3
FIFO_A1A 28 → FIFO_A1A 13C3
FIFO_A0A 26 → FIFO_A0A 13C3
BTERM* 31 → PLX_BTERM* 13D3
LRDY* 32 → PLX_LRDY* 13D3
EPC_OE 37 → EPC_OE 1D6

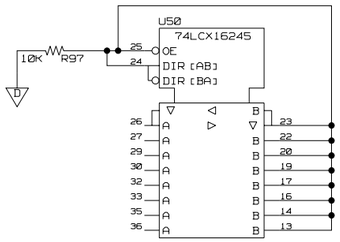
FIFO CONTROLLER

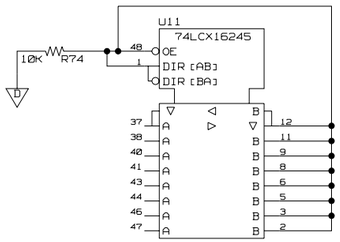
OEC MEDICAL SYSTEMS, INC.

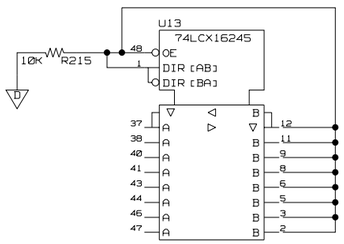
SIZE D | DWG NO. 00-879016 | REV A4 | SCALE: | SHEET 14

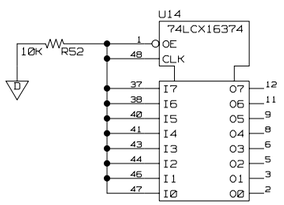
DRAWING LAST_MODIFIED=Wed Apr 5 13:11:38 2000

05-017-9/93









REFERENCE DESIGNATIONS

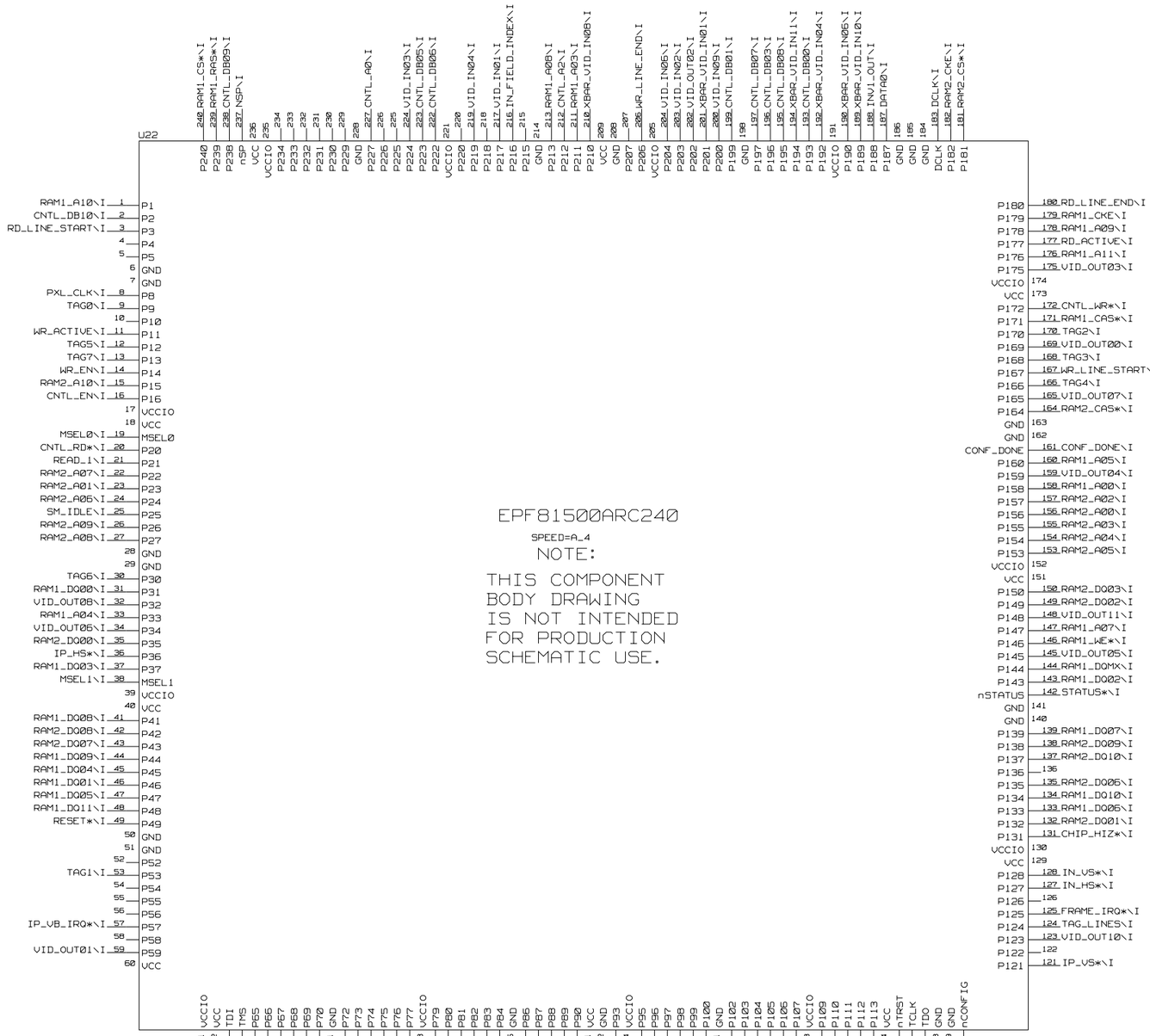
HIGHEST	UNUSED
C777	C189-199
DS9	
FL2	
P6	
R252	R157-199
TP14	
U67	

REF DESIGNATIONS	DEVICE	GND	3.3V	+5V UNUSED
U1,8,9,14	74LCX16374	4,10,15,21,28,34,39,45	7,18,31,42	
U2,3,5,20,21,33,47,63,64	SDRAM_1MX16	4,10,26,41,47,50	1,7,13,25,38,44	
U4,32,54,55	TC551664	12,34		11,33
U6	74LCX16652	4,11,18,25,32,39,46,53	7,22,35,50	
U7,17,46,67	SRAM_32KX8	14		28
U10,19	EPC1	5		7, 8
U11-13,15,16,23,26,28,34,35,37,38,40-42,51,52	74LCX16245	4,10,15,21,28,34,39,45	7,18,31,42	
U18	EPF8636AQC208	19,20,46,47,60,67,96,109,111,124,125,151,164,171,200		
U24,27,36,48,62	EPF8820AQC208	15,16,37,38,60,78,96,109,110,120,130,142,152,164,182,200		
U25	49FCT3806	5,8,16	1,20	
U22,29,53,59	EPF81500ARC240	6,7,28,29,50,51,71,85,92,101,118,119,140,141,162,163,184-186,198,208,214,228	17,39,61,78,94,108,130,152,174,191,205,221,235	18,40,60,62,91,114,129,151,173,209,236
U30,31,44,45	485506	11,34		14,31
U39	FPID_IQ160	6,9,18,23,31,38,46,60,68,75,83,90,97,111,118,126,134,141,149,163,171,178,185,193,199		8,29,45,61,79,98,119,133,148,164,186,205
U49	EPM7032	10,22,30,42		3,15,23,35
U56	VREG_3X3V	SHOWN	SHOWN	
U57	FIFO_512X36X2	10,23,33,40,48,59,66,74,81,92,99,107,118,132		5,15,30,43,57,70,86,97,110,125
U60,61	VRAM_256KX16	3,13,23,33,42,52,62		1,8,18,32,47,57
U66	PCI9050	9,26,40,51,65,80,104,120,147,160		1,10,27,41,50,66,81,103,121,146

OEC MEDICAL SYSTEMS, INC.

SIZE	DWG NO.	REV
D	00-879016	A4
SCALE:		SHEET 15

05-017-9/93



INPUT_SCAN_CONV FPGA

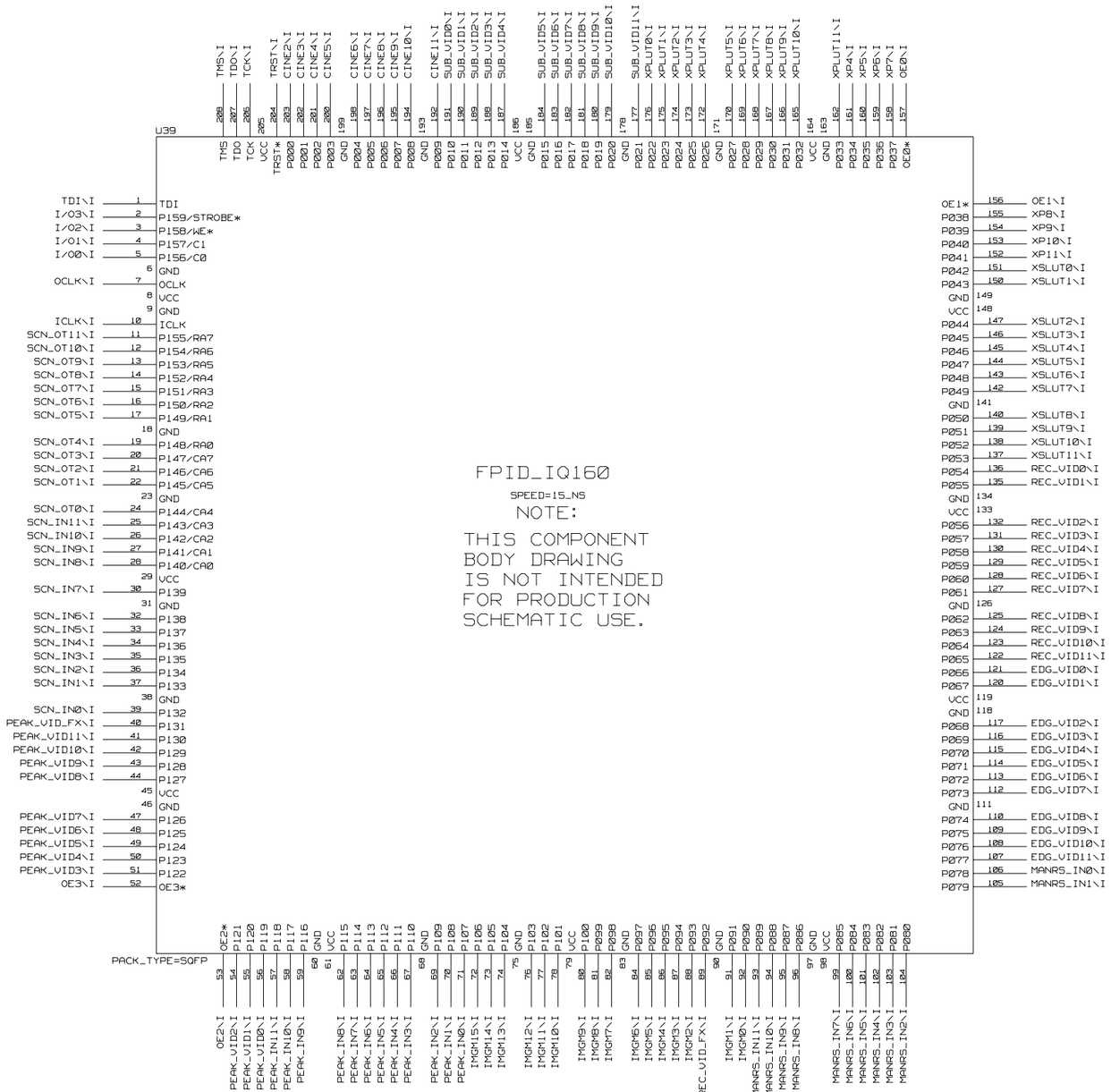
OEC MEDICAL SYSTEMS, INC.

SIZE	DWG NO.	REV
D	00-879016	A4

SCALE: NONE | SHEET 16

DRAWING LAST_MODIFIED=Wed Apr 5 13:11:39 2000

05-017-9/93



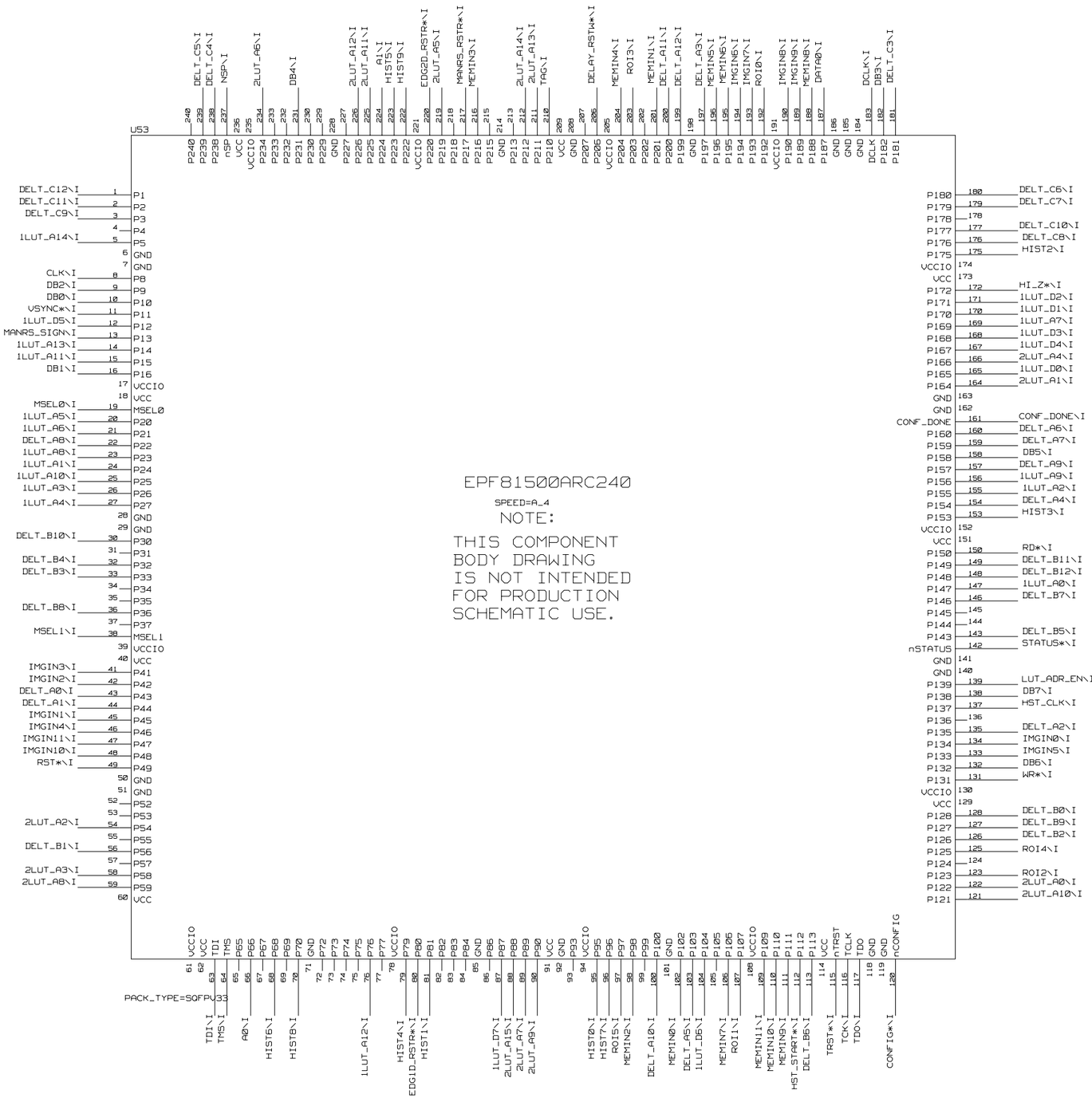
CROSS POINT SWITCH PINOUT

DRAWING LAST_MODIFIED=Wed Apr 5 13:11:41 2000

OEC MEDICAL SYSTEMS, INC.

SIZE	DWG NO.	REV
D	00-879016	A4
SCALE: NONE		SHEET 17

05-017-9/93



NOTE:

THIS COMPONENT BODY DRAWING IS NOT INTENDED FOR PRODUCTION SCHEMATIC USE.

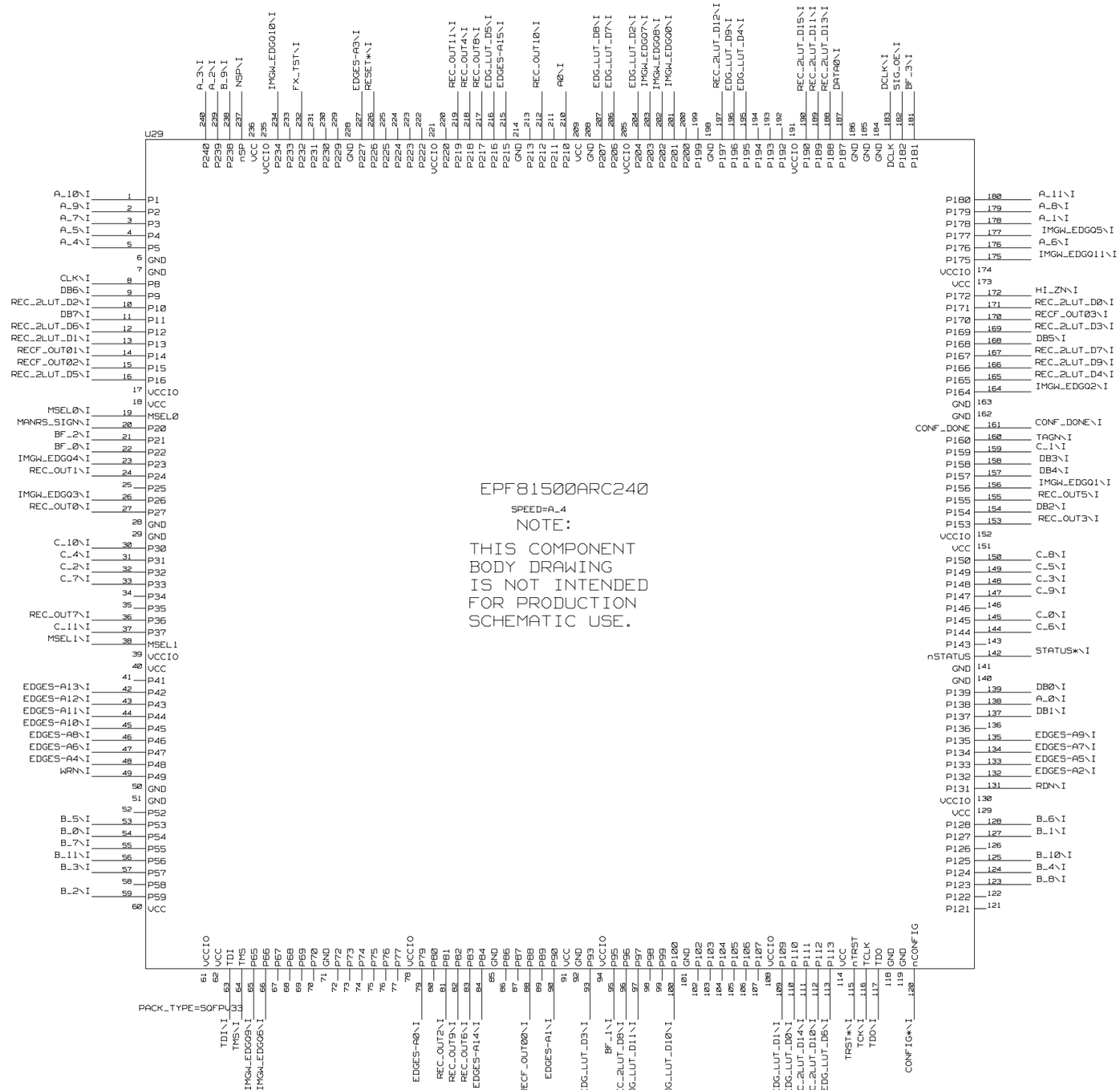
MANRS FPGA PINOUT

DRAWING LAST_MODIFIED=Wed Apr 5 13:11:42 2000

OEC MEDICAL SYSTEMS, INC.

SIZE	DWG NO.	REV
D	00-879016	A4
SCALE: NONE		SHEET 18

05-017-9/93



X5

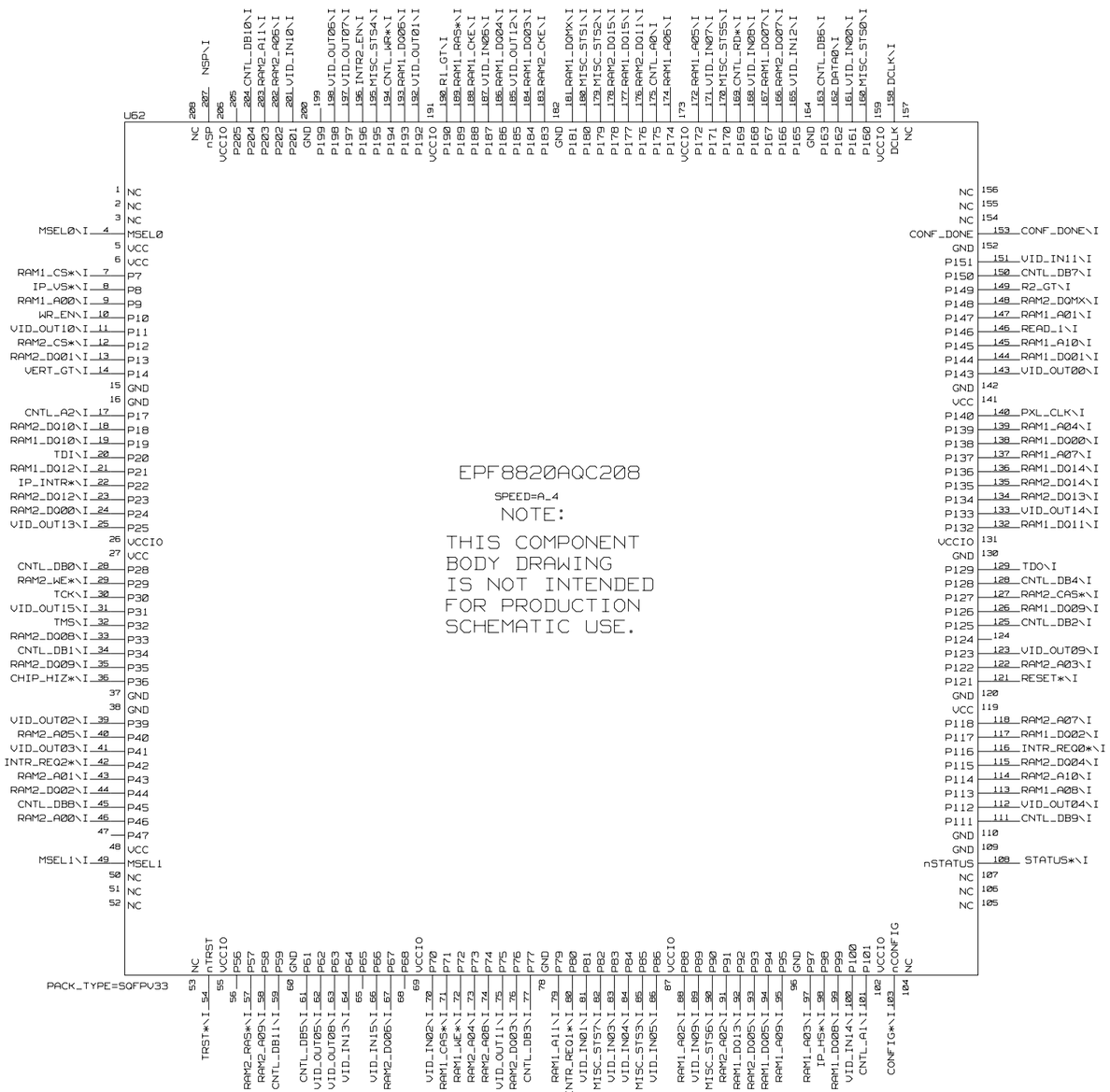
EDGE FPGA PINOUT

DRAWING LAST_MODIFIED=Wed Apr 5 13:11:42 2000

OEC MEDICAL SYSTEMS, INC.

SIZE	DWG NO.	REV
D	00-879016	A4
SCALE: NONE		SHEET 19

05-017-9/93



FILTER MEMORY FPGA

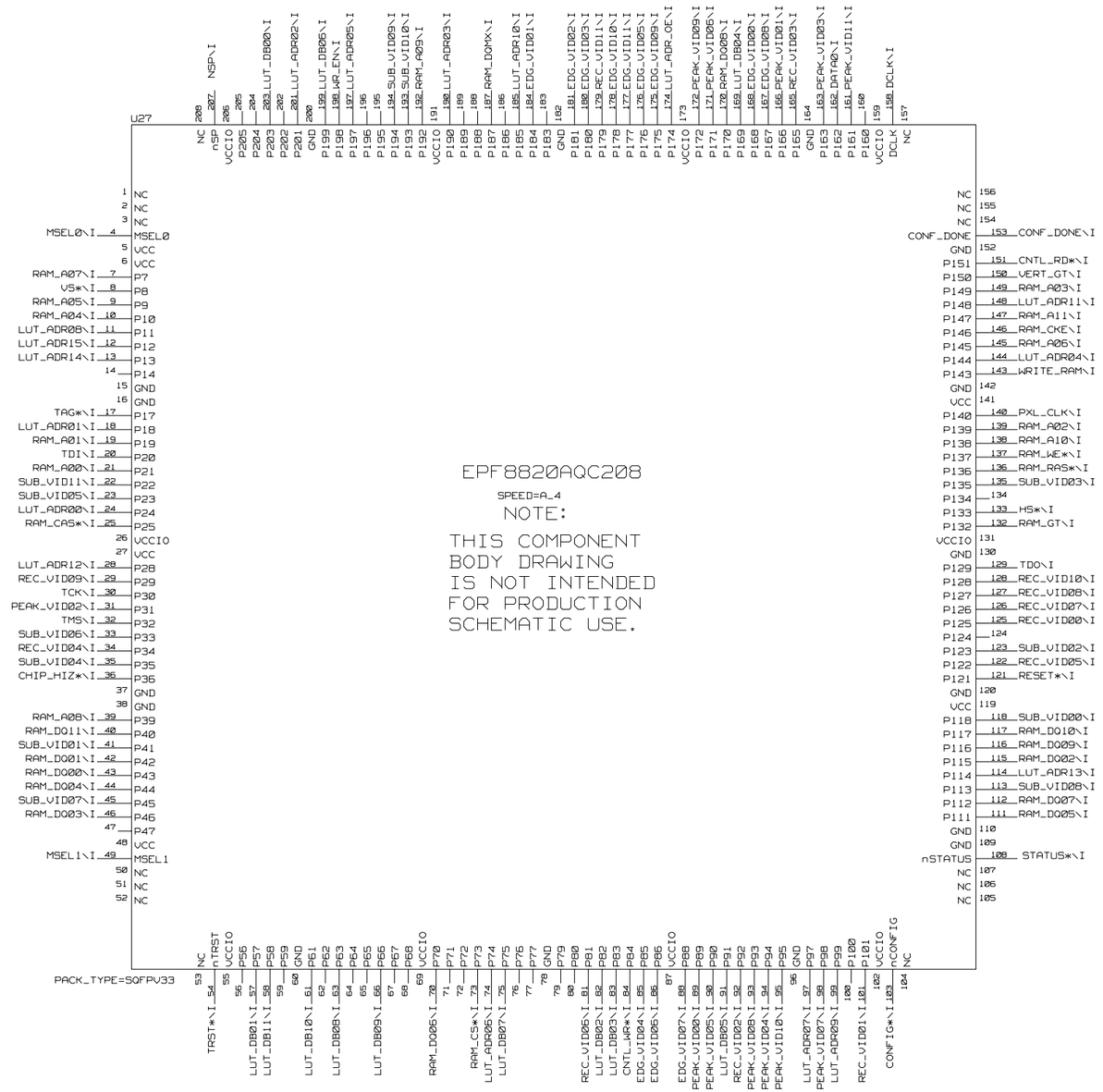
OEC MEDICAL SYSTEMS, INC.

SIZE	DWG NO.	REV
D	00-879016	A4

SCALE: NONE SHEET 20

DRAWING LAST_MODIFIED=Wed Apr 5 13:11:43 2000

05-017-9/93



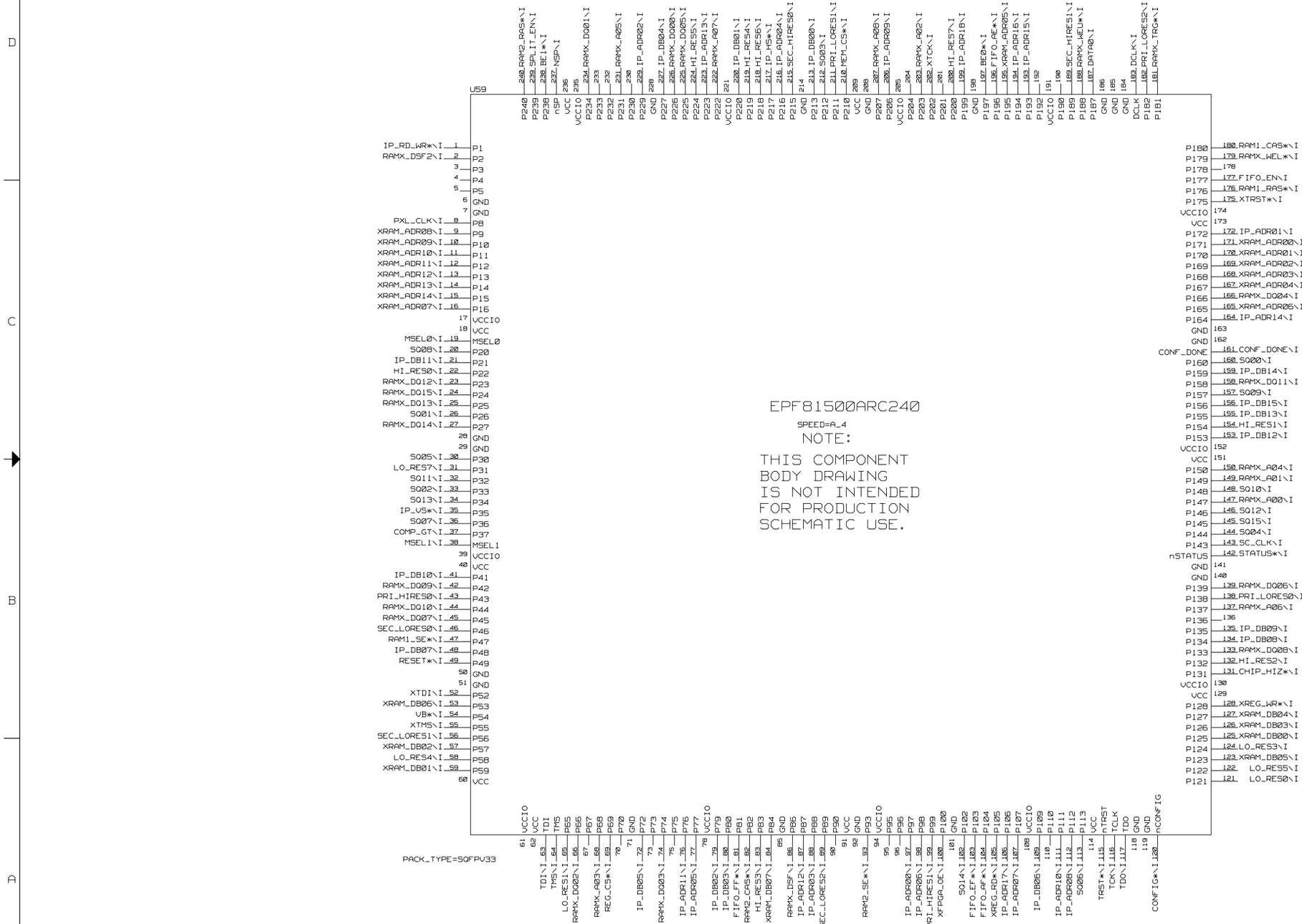
MASK_CNTL FPGA

OEC MEDICAL SYSTEMS, INC.

SIZE	DWG NO.	REV
D	00-879016	A4
SCALE: NONE		SHEET 21

DRAWING LAST_MODIFIED=Wed Apr 5 13:11:43 2000

05-017-9/93



BITMEM_CNTL FPGA

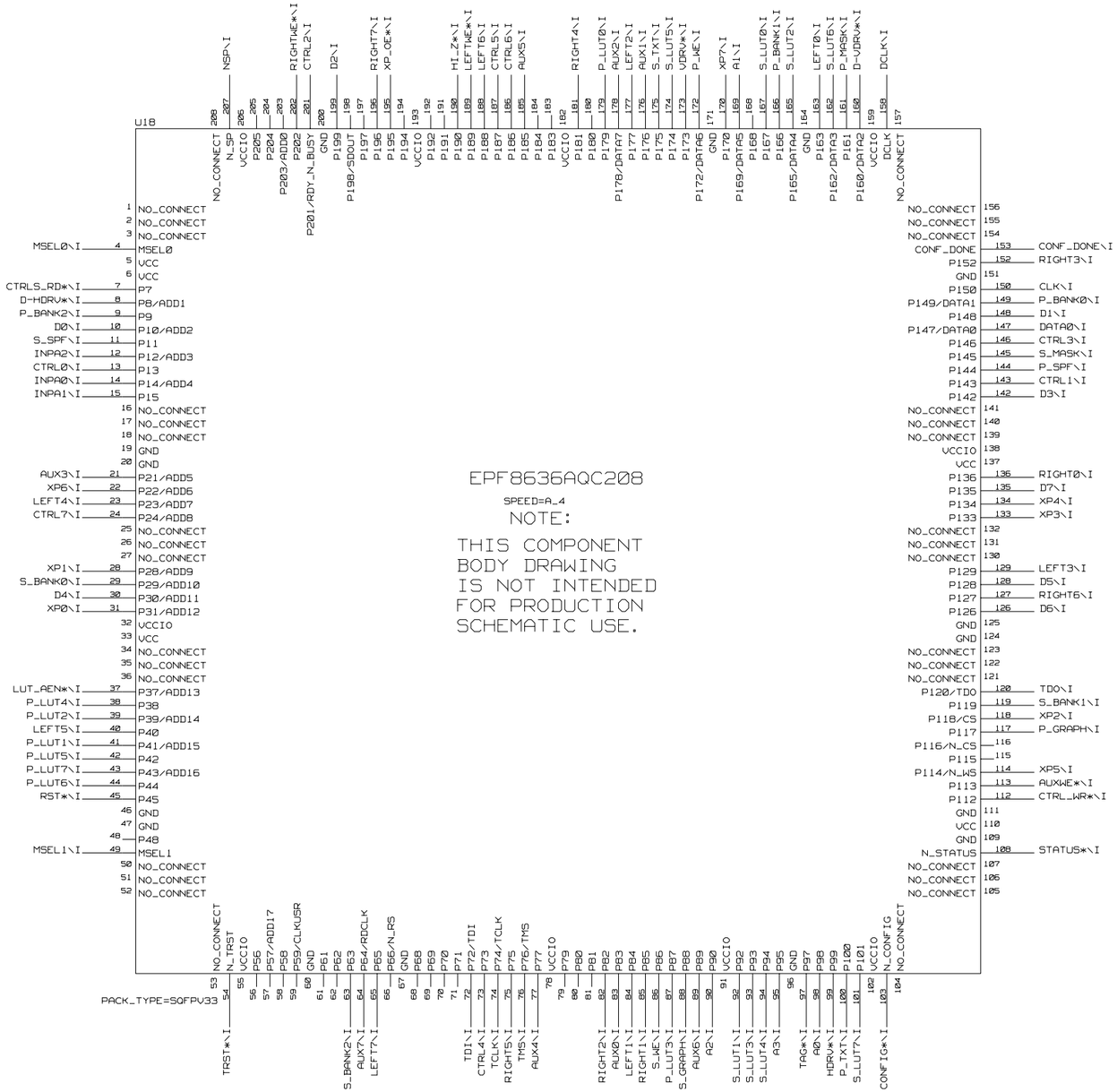
OEC MEDICAL SYSTEMS, INC.

SIZE	DWG NO.	REV
D	00-879016	A4

SCALE: NONE | SHEET 22

DRAWING LAST_MODIFIED=Wed Apr 5 13:11:44 2000

05-017-9/93

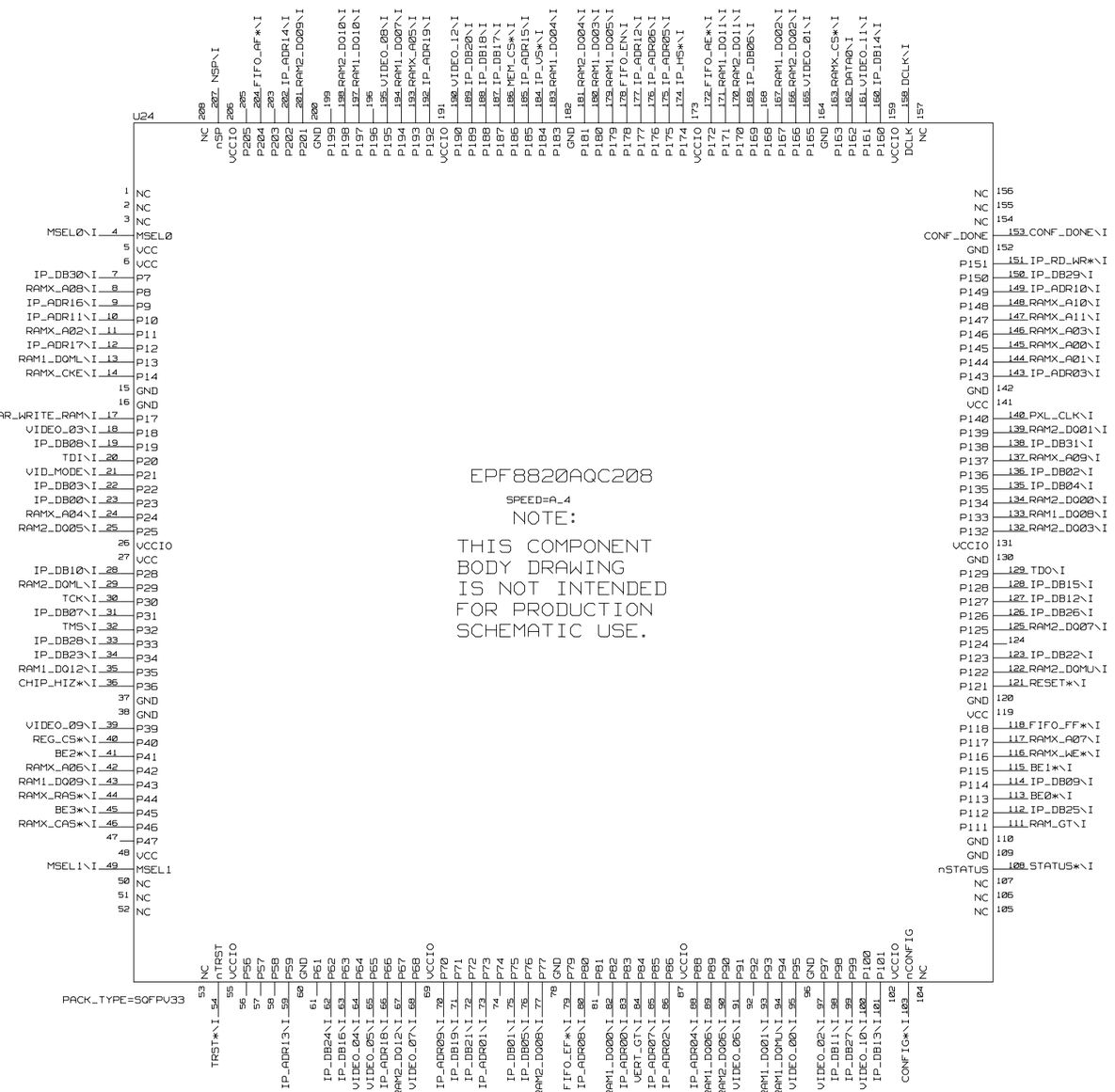


TEXT FPGA PINOUT

DRAWING LAST_MODIFIED=Wed Apr 5 13:11:45 2000

OEC MEDICAL SYSTEMS, INC.			
SIZE D	DWG NO. 00-879016		REV A4
SCALE: NONE		SHEET 23	

05-017-9/93



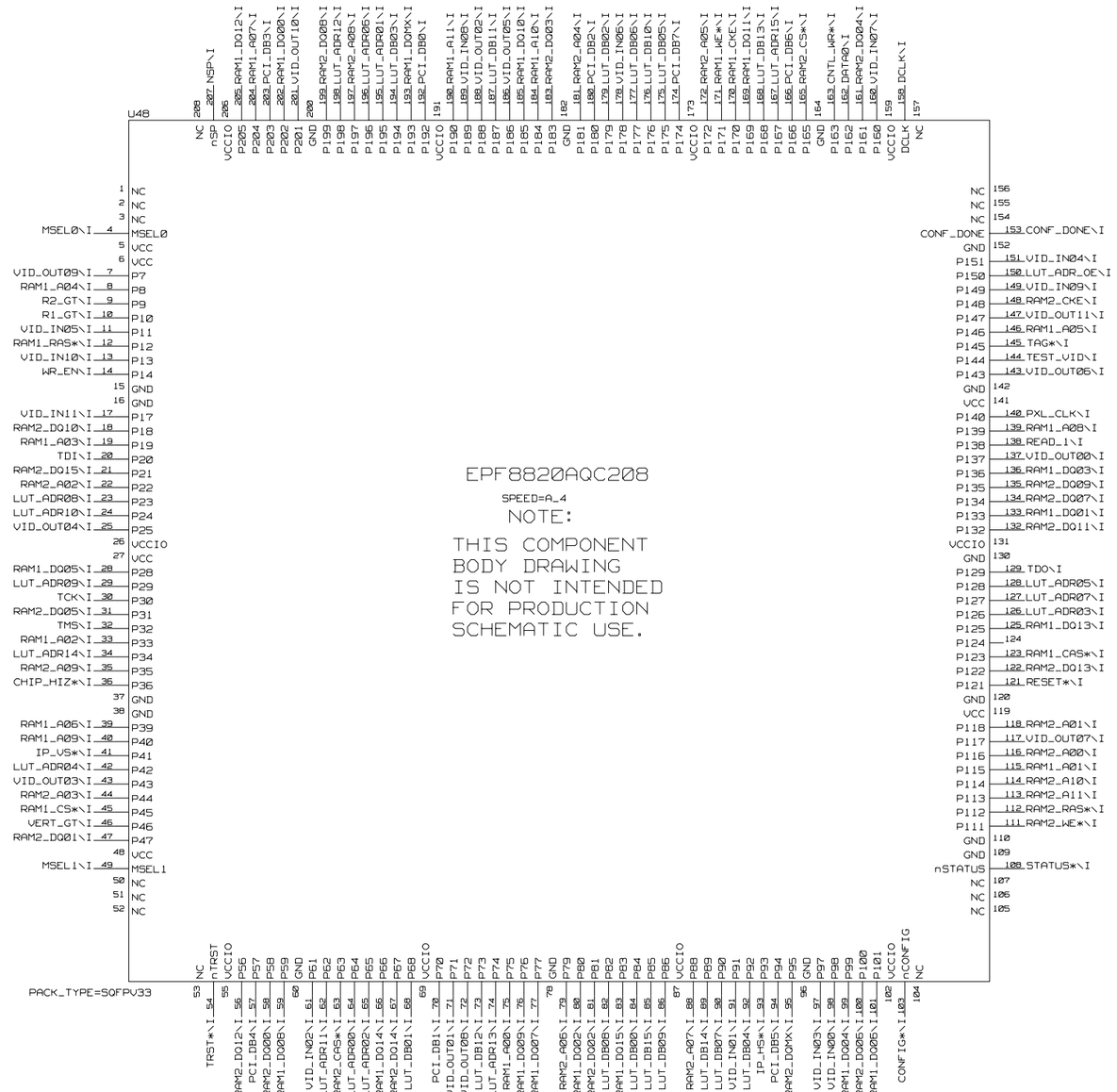
IMGMEM_CNTL FPGA

OEC MEDICAL SYSTEMS, INC.

SIZE	DWG NO.	REV
D	00-879016	A4
SCALE: NONE		SHEET 24

DRAWING LAST_MODIFIED=Wed Apr 5 13:11:45 2000

05-017-9/93



PEAK / FILTER FPGA

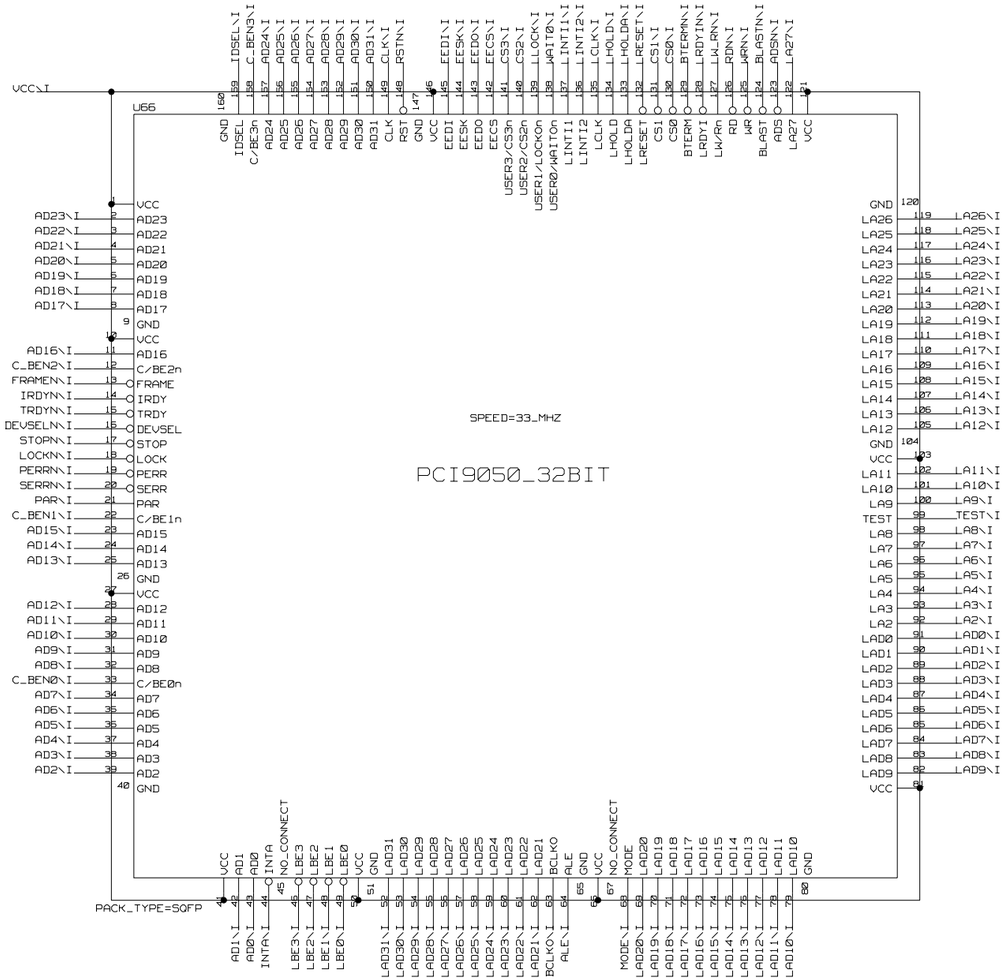
OEC MEDICAL SYSTEMS, INC.

SIZE	DWG NO.	REV
D	00-879016	A4

SCALE: NONE | SHEET 25

DRAWING LAST_MODIFIED=Wed Apr 5 13:11:46 2000

05-017-9/93



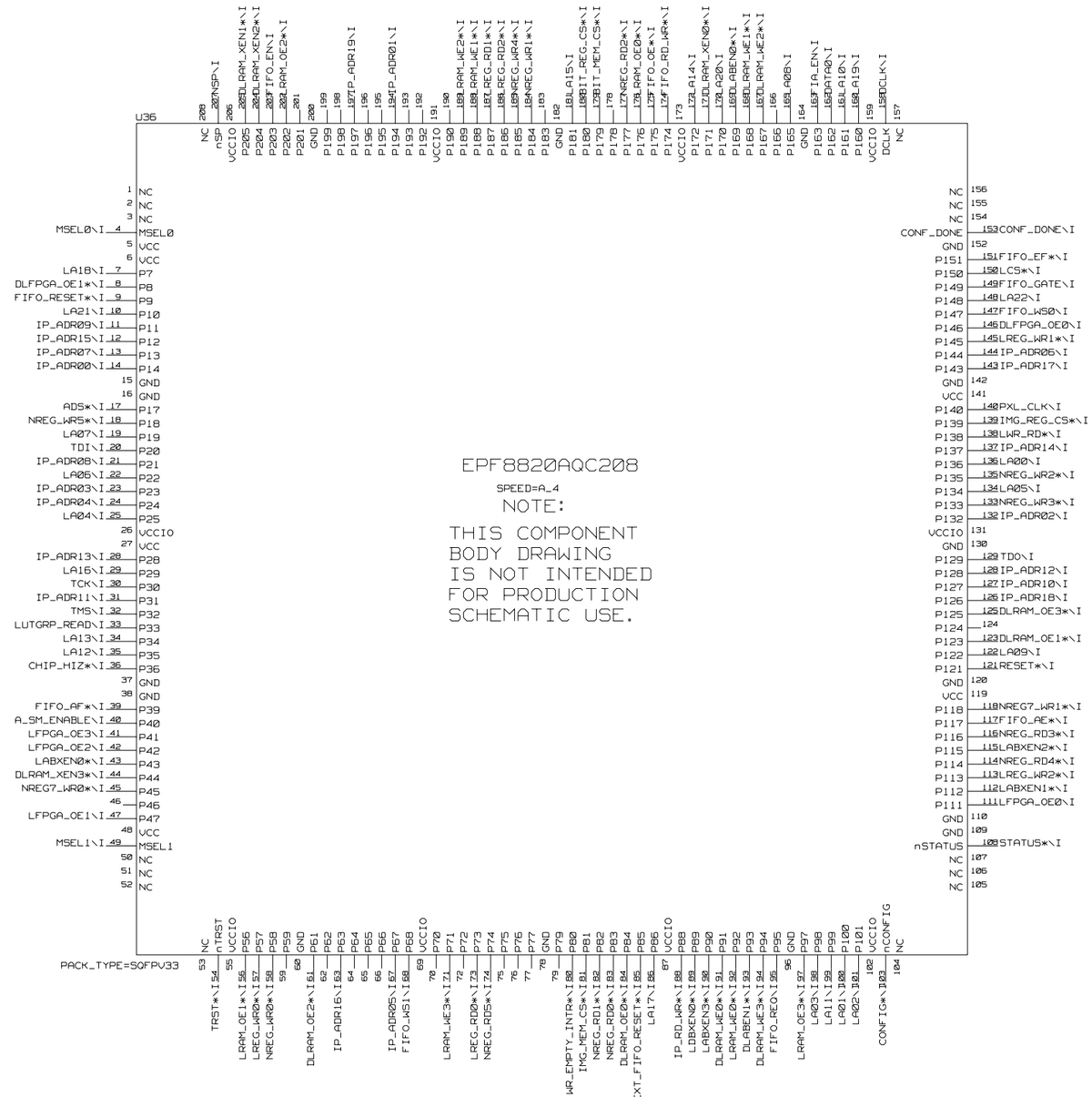
PLX_PCI9050_CONTROLLER PINOUT

DRAWING LAST_MODIFIED=Wed Apr 5 13:11:45 2000

OEC MEDICAL SYSTEMS, INC.

SIZE	DWG NO.	REV
D	00-879016	A4
SCALE: NONE		SHEET 26

05-017-9/93



FIFO_CNTL FPGA

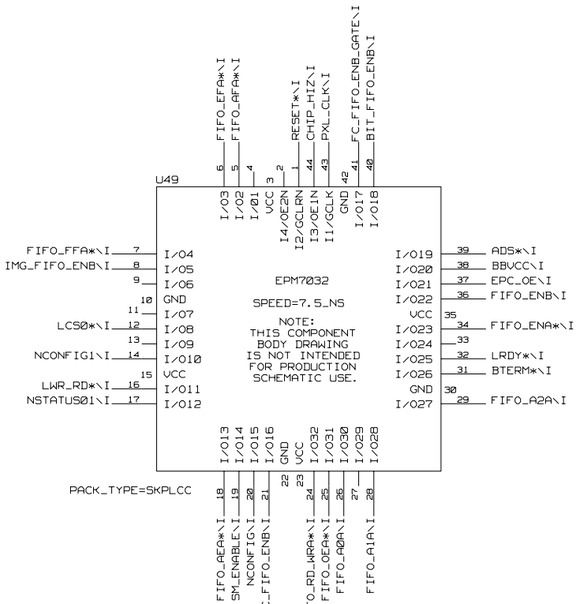
DRAWING LAST_MODIFIED=Wed Apr 5 13:11:47 2000

OEC MEDICAL SYSTEMS, INC.

SIZE	DWG NO.	REV
D	00-879016	A4

SCALE: NONE SHEET 27

05-017-9-93



CONFIG / FIFO-A EPLD

OEC MEDICAL SYSTEMS, INC.

SIZE	DWG NO.	REV
D	00-879016	A4
SCALE: NONE		SHEET 28

DRAWING LAST_MODIFIED=Wed Apr 5 13:11:40 2000

05-017-9/93

*** Signal Cross-Reference ***
--- for the entire design --

+3.3V	1C8
+3.3V_SEN	1C8
+5VDC	1C8
AD0	13A5
AD1	13A5
AD2	13A5
AD3	13A5
AD4	13A5
AD5	13A5
AD6	13B5
AD7	13B5
AD8	13B5
AD9	13B5
AD10	13B5
AD11	13B5
AD12	13B5
AD13	13B5
AD14	13B5
AD15	13B5
AD16	13B5
AD17	13B5
AD18	13B5
AD19	13B5
AD20	13B5
AD21	13B5
AD22	13B5
AD23	13B5
AD24	13B5
AD25	13B5
AD26	13B5
AD27	13B5
AD28	13B5
AD29	13B5
AD30	13B5
AD31	13B5
ADD <7..0>	10B3
AD_D0	10C1
AD_D1	10C1
AD_D2	10C1
AD_D3	10C1
AD_D4	10C1
AD_D5	10C1
AD_D6	10C1
AD_D7	10C1
AD_WREN *	10C1
BBVCC	1D7 10D5 14C3
BIT_CONF_DONE	9D6 1C3
BIT_FIFO_ENB	9D5 14C3
BIT_MEM_CS *	14B5 9C8
BIT_RAMX_A <11..0>	9B6
BIT_RAMX_DQ <15..0>	9A5
BIT_RAMX_SQ <15..0>	9A5
BIT_REG_CS *	14B5 9D8
BIT_TDO	9D5 1C4
BM_COMP_GT	9C6
CINE_D <9..0>	4B7
CINE_D_OE *	4C7
CINE_HDRV *	4B8 4C6
CINE_PIXCLK	3B6 4B8
CINE_TAG *	4B8 4C6
CINE_VDRV *	4B8 4C6
CINE_XBAR <11..2>	4B5
CINE_X_OE	4D4
CLK	13C5
CONF_DONE	1B3 1D7 3C4
CONF_DONE *	1D5 3C3
C_BEN0	13C5
C_BEN1	13C5
C_BEN2	13C5
C_BEN3	13C5

DCLK	1D6 10D5
DC_HDRV *	10C1
DC_VDRV *	10C1
DELAY_RSTW *	5D4 5D8 6C8
DEVSELN	13C5
EDG1D_RSTR *	5D4 6C8
EDG2D_RSTR *	5D4 6B8
EDGE_CONF_DONE	6D4 1C3
EDGE_TDO	6D4 1C4
EDG_ABXEN *	14A5 6D3
EDG_CNTL_RD *	14B5 6C6
EDG_CNTL_WR *	14B5 6C6
EDG_FPGA_OE	14A5 6D6
EDG_LUT_ADR <15..0>	6B3
EDG_LUT_DB <15..0>	6A3
EDG_LUT_OE *	14A5 6C4
EDG_LUT_WE *	14A5 6C4
EDG_VID <11..0>	6B4 4C5 8C8
EMPTY_IRQ_EN	13C3 7C7
EPC_OE	14C2 1D6
EXT_FIFO_RESET *	13C3 14A7
FIFO_A0A	14C1 13C3
FIFO_A1A	14C1 13C3
FIFO_A2A	14C1 13C3
FIFO_AEA *	13B3 14C3
FIFO_AEB *	13B2 9C8 11C7 14C7
FIFO_AFA *	13B3 14C3
FIFO_AFB *	13B2 9C8 11C7 14C7
FIFO_C_CONF_DONE	14D6 1C3
FIFO_C_TDO	14D5 1D4
FIFO_EFA *	13B3 14C3
FIFO_EFB *	13B2 9C8 11C7 14C7
FIFO_EMPTY_IRQ *	14C5 7C7
FIFO_ENA	14C1 13C3 14A7
FIFO_ENB	14D1 13C2
FIFO_FFA *	13B3 14C3
FIFO_FFB *	13B2 9C8 11C7
FIFO_OEA *	14C1 13C3
FIFO_OEB *	14D5 13C2
FIFO_RD_WRA *	14C1 13C3
FIFO_RD_WRB *	14D5 13C2
FIFO_REQB	14C5 13C2
FIFO_RESET *	14A7 13C3
FIFO_WS0	14A7 13C2
FIFO_WS1	14A7 13C2
FLTR_CONF_DONE	7D5 1C3
FLTR_TDO	7D5 1C4
FM_CNTL_RD *	14B5 7A7
FM_CNTL_WR *	14B5 7A7
FM_R1_GT	7C5
FM_R2_GT	7C5
FM_RAM1_A <11..0>	7B5
FM_RAM1_DQ <15..0>	7A3
FM_RAM2_A <11..0>	7A5
FM_RAM2_DQ <15..0>	7A4
FM_READ_1	7D5
FM_VERT_GT	7C5
FM_WR_EN	7D5
FPGA_DATA0A	1D4 3D5 8D8 11D7 12D8 14D7
FPGA_DATA0B	1D4 5D6 6D6 7D7 9D8 10D5
FPGA_DCLKA	1D3 3D5 8D8 11D7 12D8 14D7
FPGA_DCLKB	1D3 5D6 6D6 7D7 9D8
FRAMEN	13C5
FRAME_IRQ *	3D3 7C7
HIST_IN <9..0>	5C5 7B3
HIST_ROI0	9A6 5A6
HIST_ROI1	9A6 5A6
HIST_ROI2	9A6 5A6
HIST_ROI3	9A6 5A6
HIST_ROI4	9A6 5A6
HIST_ROI5	9A6 5A6
HST_CLK	5C4 7C3
HST_FC *	14B5 7C3

HST_LD *	14B5 7C3
HST_RD *	14B6 7C3
HST_START *	5C5 7C3
HST_WR *	14B5 7C3
IDSEL	13C5
IMG_CONF_DONE	11D6 1C3
IMG_FIFO_ENB	11D5 14D3
IMG_MEM_CS *	14B5 11C7
IMG_RAM1_DQ <15..0>	11A4
IMG_RAM2_DQ <15..0>	11A4
IMG_RAMX_A <11..0>	11B6
IMG_RAM_GT	11C5
IMG_REG_CS *	14B5 11C7
IMG_TDO	11D5 1D4
IMG_VERT_GT	11D5
IMG_VID <15..0>	4A5 11C6
IMG_VID_MODE	11D5
INTAN	13C5
IN_PCI_TCK	1D5 13D8
IN_PCI_TMS	1D5 13D8
IN_PCI_TRST *	1D5 13D8
IP_ADR <19..0>	14C5 5C1 6C2 8C3 9A2 9C8 10B8 11C7 12C2
IP_ASIC_ADR <15..0>	14B4 3B5 5D6 6C6 7A7 9C8 10A8
IP_DB <31..0>	13B2 3A4 5C5 6D4 7D2 9B8 10A8 11B7 14A3
IP_DB_BE <3..0> *	13B2 9C8 11C7
IP_DIS_PIXCLK	3B6 10B1
IP_HS *	3C2 4C7 7D7 8C8 9D8 10C4 11D7 12D8
IP_INTR *	7D5 13D3
IP_LUT_DB <15..0>	14A4 5B1 6D2 8B3 9C1 10A8 12A2
IP_RD_WR *	14C5 5C3 5D3 6D3 8B4 9C2 9C8 10C6 11C7 12C3
IP_RESET *	13D3 3D5 5D6 6D6 7D7 8D8 9D8 10D5 11D7 12D8 14D3 14D7
IP_VB_IRQ *	3D3 7C7 9D5
IP_VS *	3D2 4C7 5D6 7D7 8C8 9D8 10C4 11D7 12D8
IRDYN	13C5
ISC_CNTL_RD *	14B5 3B5
ISC_CNTL_WR *	14B5 3B5
ISC_CONF_DONE	3D4 1C3
ISC_RAM1_A <11..0>	3B4
ISC_RAM1_DQ <11..0>	3A3
ISC_RAM2_A <11..0>	3B4
ISC_RAM2_DQ <11..0>	3A4
ISC_RD_ACTIVE	3A6
ISC_RD_END	3A6
ISC_RD_RESET	3A6
ISC_RD_START	3A6
ISC_READ_1	3A6
ISC_SM_IDLE	3A6
ISC_TDO	3D3 1D4
ISC_VID_OUT <11..0>	3C4 4C5
ISC_WR_ACTIVE	3A6
ISC_WR_EN	3A6
ISC_WR_END	3A6
ISC_WR_START	3A6
LDD <7..0>	10D3
LD_D0	10D1
LD_D1	10D1
LD_D2	10D1
LD_D3	10D1
LD_D4	10D1
LD_D5	10D1
LD_D6	10D1
LD_D7	10D1
LD_WREN *	10D1
LOCKN	13C5
MANRS_1LUT_ADR <14..0>	5A3
MANRS_1LUT_DB <7..0>	5A4
MANRS_2LUT_ADR <15..0>	5C3
MANRS_2LUT_DB <15..0>	5C3 6B6

MANRS_ABEN *	14A5 5D2
MANRS_CNTL_RD *	14B5 5C6
MANRS_CNTL_WR *	14B5 5C6
MANRS_CONF_DONE	5D4 1C3
MANRS_DELT_A <12..0>	5A5
MANRS_DELT_B <12..0>	5B6
MANRS_DELT_C <12..0>	5C6
MANRS_FPGA_OE	14A5 5C6
MANRS_IMG_IN <11..0>	4D3 5C6
MANRS_LUT1_OE *	14A5 5B4
MANRS_LUT1_WE *	14A5 5B4
MANRS_LUT1_XEN *	14A5 5C3
MANRS_LUT2_OE *	14A5 5D4
MANRS_LUT2_WE *	14A5 5D4
MANRS_LUT2_XEN *	14A5 5D3
MANRS_RSTR *	5D4 5D8
MANRS_SIGN	5C4 6B6
MANRS_TDO	5D4 1C4
MASK_ABXEN *	14A5 8C4
MASK_CNTL_RD *	14B5 8C8
MASK_CNTL_WR *	14B5 8C8
MASK_CONF_DONE	8D6 1B3
MASK_FPGA_OE	14A5 8C8
MASK_LUT_OE *	14A5 8B5
MASK_LUT_WE *	14A5 8B5
MASK_TDO	8D5 1D4
MSKLUT_ADR <15..0>	8A5
MSKLUT_DB <15..0>	8A5
MSK_RAM_DQ <11..0>	8B5
MSK_RAM_GT	8A6
MSK_VERT_GT	8A6
MSK_WRITE_RAM	8A6
MSK_WR_EN	8A6
NCONFIG	1D7 14C3
NCONFIG1	14C1 1C3
NCONFIG_BIT	1C2 9D8
NCONFIG_EDGE	1C2 6D6
NCONFIG_FIFO_C	1C2 14D7
NCONFIG_FLTR	1C2 7D7
NCONFIG_IMG	1C2 11D7
NCONFIG_ISC	1C2 3D5
NCONFIG_MANRS	1C2 5D6
NCONFIG_MASK	1C2 8D8
NCONFIG_PEAK	1C2 12D8
NCONFIG_TEXT	1C2 10D5
NSTATUS	1D7 10D3 14C3
PAR	13C5
PCI_+3.3V	13B8
PCI_+5V	1D6 13C6
PCI_+5V_IO	13C8
PCI_+12V	13B8
PCI_-12V	13B8
PCI_GND	13A8
PCI_TCK	1D4 3D5 5D6 6D6 7D7 8D8 9D8 10D5 11D7 12D8 14D7
PCI_TDI	13D8 1D4
PCI_TDO	1C3 13D8
PCI_TMS	1D4 3D5 5D6 6D6 7D7 8D8 9D8 10D5 11D7 12D8 14D7
PCI_TRST *	1D4 3D5 5D6 6D6 7D7 8D8 9D8 10D5 11D7 12D8 14D7
PEAK_ABXEN *	14B5 12D3
PEAK_CNTL_RD *	14B5 12B2
PEAK_CNTL_WR *	14B5 12A8
PEAK_CONF_DONE	12D6 1C3
PEAK_DBXEN *	14A7 12C3
PEAK_FPGA_OE	14B5 12A8
PEAK_IN <11..0>	4D3 12D8
PEAK_LUT_OE *	14B5 12D4
PEAK_LUT_WE *	14B5 12D4
PEAK_TDO	12D5 1D4
PEAK_VID <11..0>	12D5 4D5 8B8
PEAK_VID_FX	4B3 12D5

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PERRN	13C5
PIXCLK1	3B6 3B3
PIXCLK2	3B6 12D8 14D3 14D7
PIXCLK3	3B6 4D4 13D3
PIXCLK4	3B6 5D6 7D7 9D8
PIXCLK5	3B6 5D8 6C8
PIXCLK6	3B6 6D6 10D2 10D4
PIXCLK7	3B6 8C6 11C5 11D7
PIXCLK8	3B6 4C7 8C8
PIXCLK_MON	3B7
PKLUTDB <15..0>	12C4
PKR1DQ <15..0>	12A5
PKR2DQ <15..0>	12A5
PK_DB <7..0>	12A5
PK_LUT_ADR <15..0>	12C5
PK_R1_GT	12A8
PK_R2_GT	12A8
PK_RAM1_A <11..0>	12B6
PK_RAM2_A <11..0>	12A6
PK_READ_1	12A8
PK_VERT_GT	12A8
PK_WR_EN	12A8
PLX_ADS *	13D3 14C3 14C7
PLX_BLAST *	13D3
PLX_BTERM *	14C1 13D3
PLX_LA <24..2>	13C4 14C7
PLX_LAD <31..0>	13A3
PLX_LBE <3..0>	13B3
PLX_LCS0 *	13C3 14C3 14C7
PLX_LCS1 *	13C3
PLX_LRDY *	14C1 13D3
PLX_LWAIT *	13C3
PLX_LWR_RD *	13D3 14C3 14C7
PLX_RD *	13D3
PLX_WR *	13D3
PRI_LUT_OE *	14A5 10D6
PRI_LUT_WE *	14A5 10D6
PRI_LUT_XEN *	14A5 10C6
PRI_MASK	9C6 10C4
PRI_SPF	9C6 10B4
PRI_TXT&G0	9C6 10C4
PRI_TXT&G1	9C6 10C4
PRI_WE	9C6 10B4
P_BANK0	10B3 10D7
P_BANK1	10B3 10D7
P_BANK2	10B3 10D7
P_LUT <7..0>	10C5
RDD <7..0>	10C3
RD_D0	10C1
RD_D1	10C1
RD_D2	10C1
RD_D3	10C1
RD_D4	10C1
RD_D5	10C1
RD_D6	10C1
RD_D7	10C1
RD_WREN *	10C1
RECMEM_0L <15..0>	7C5 5C6 6C8
RECMEM_P2L <15..0>	6C6
RECMEM_P4L <15..0>	6B6
REC_VID <15..0>	6B4 4C3 7C7 8C8
REC_VID_FX	4B3 6B4
REVISION <7..0>	7C7
RSTN	13C5
SEC_LUT_OE *	14A5 10B6
SEC_LUT_WE *	14A5 10B6
SEC_LUT_XEN *	14A5 10A6
SEC_MASK	9C6 10B4
SEC_SPF	9C6 10B4
SEC_TXT&G0	9C6 10B4
SEC_TXT&G1	9C6 10B4
SEC_WE	9C6 10B4
SERRN	13C5

STOPN	13C5
SUB_VID <11..0>	8C5 4C3
S_BANK0	10B3 10C7
S_BANK1	10B3 10C7
S_BANK2	10B3 10C7
S_LUT <7..0>	10C5
TAG *	10C1
TAG_DATA <7..0>	9D5 3C5
TAG_LINES *	3C2 4C7 5D6 6C6 8C8 10C2 10C4 12D8
TDI_BIT	1C3 9D8
TDI_EDGE	1C3 6D6
TDI_FIFO_C	1D3 14D7
TDI_FLTR	1C3 7D7
TDI_IMG	1D3 11D7
TDI_ISC	1D3 3D5
TDI_MANRS	1C3 5D6
TDI_MASK	1D3 8D8
TDI_PEAK	1D3 12D8
TDI_TEXT	1D3 10D5
TEXT_ABEN *	14A5 10D8
TEXT_CNTL_RD *	14B5 10A4
TEXT_CNTL_WR *	14B5 10A4
TEXT_CONF_DONE	10D3 1C3
TEXT_TDO	10D3 1C4
TRDYN	13C5
VC_D00	3C8
VC_D01	3C8
VC_D02	3C8
VC_D03	3C8
VC_D04	3C8
VC_D05	3C8
VC_D06	3C8
VC_D07	3C8
VC_D08	3C8
VC_D09	3C8
VC_D10	3C8
VC_D11	3C8
VC_FIELD	3C8
VC_HSYNC *	3C8
VC_PIXCLK	3B8
VC_SPARE1	3C8
VC_SPARE2	3C7
VC_SPARE3	3C7
VC_VID <11..0>	3C5
VC_VSYNC *	3C8
XBAR_ABXEN *	14A7 9C2
XBAR_ADR <14..0>	9D3
XBAR_CNTL_RD *	14A7 9D5
XBAR_CNTL_WR *	14A7 9D5
XBAR_DB <7..0>	9C3
XBAR_FPGA_OE	14A7 9D5
XBAR_IMG_WRITE	4D4 11C7
XBAR_ISC_VID <11..0>	4B5 3C5
XBAR_RAM_OE *	14A7 9C3
XBAR_RAM_WE *	14A7 9C3
XBAR_TCK	9D3 4D4
XBAR_TDI	9D3 4D4
XBAR_TDO	4D3
XBAR_TMS	9D3 4D4
XBAR_TRST *	9D3 4D4
XP <11..4>	4B3 10A3
XPLUT <11..0>	4A2 10C8
XP_IMG_OE *	4D4 10A4
XP_OE *	14A5 4D4 10A4
XSLUT <11..0>	4B2 10A8

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*** Unit Cross-Reference ***
--- for the entire design --

ASM_U10 ADDONS 1D2
ASM_U19 ADDONS 1D2
ASM_U49 ADDONS 1D2
ASM_U65 ADDONS 1D2
C1 CERSMT_1206 3B6
C2 CERSMT_1206 1B7
C3 CERSMT_1206 1A7
C4 CERSMT_1206 1B8
C5 CERSMT_1206 1B7
C6 CERSMT_1206 3A6
C7 CERSMT_1206 1A8
C8 TASMT_68U_41810001 1D7
C9 CERSMT_1206 1B7
C10 CERSMT_1206 3A7
C11 CERSMT_1206 1C5
C12 TASMT_68U_41810001 1D7
C13 TASMT_68U_41810001 1C7
C14 CERSMT_1206 13D6
C15 CERSMT_1206 1B8
C16 CERSMT_1206 1C8
C17 CERSMT_1206 1B8
C18 CERSMT_1206 1A8
C19 CERSMT_1206 1A8
C20 CERSMT_1206 1C8
C21 CERSMT_1206 1A8
C22 CERSMT_1206 3C3
C23 CERSMT_1206 1B8
C24 CERSMT_1206 3C3
C25 CERSMT_1206 1B6
C26 CERSMT_1206 1B7
C27 CERSMT_1206 1B5
C28 CERSMT_1206 1B5
C29 CERSMT_1206 1B7
C30 CERSMT_1206 1B5
C31 CERSMT_1206 1C6
C32 CERSMT_1206 1C5
C33 CERSMT_1206 1C5
C34 CERSMT_1206 1A6
C35 CERSMT_1206 3A6
C36 CERSMT_1206 1C4
C37 CERSMT_1206 1B5
C38 CERSMT_1206 1B8
C39 CERSMT_1206 1B8
C40 CERSMT_1206 1B8
C41 CERSMT_1206 1A8
C42 CERSMT_1206 1A6
C43 CERSMT_1206 1B6
C44 CERSMT_1206 1B6
C45 CERSMT_1206 1C6
C46 CERSMT_1206 1A5
C47 CERSMT_1206 1C6
C48 CERSMT_1206 1B5
C49 CERSMT_1206 1C6
C50 CERSMT_1206 1C4
C51 CERSMT_1206 1B8
C52 CERSMT_1206 1B8
C53 CERSMT_1206 1B8
C54 CERSMT_1206 1B7
C55 CERSMT_1206 1C8
C56 CERSMT_1206 1C8
C57 CERSMT_1206 1C8
C58 CERSMT_1206 1B5
C59 CERSMT_1206 1B6
C60 CERSMT_1206 1B6
C61 CERSMT_1206 1B5
C62 CERSMT_1206 1C6
C63 CERSMT_1206 1B5
C64 CERSMT_1206 1B5
C65 CERSMT_1206 1B5
C66 CERSMT_1206 1C6
C67 CERSMT_1206 1B6
C68 CERSMT_1206 1A6
C69 CERSMT_1206 1C8
C70 CERSMT_1206 1A8
C71 CERSMT_1206 1C8
C72 CERSMT_1206 1B6
C73 CERSMT_1206 1B6
C74 CERSMT_1206 1B5
C75 CERSMT_1206 1B5
C76 CERSMT_1206 1B5
C77 CERSMT_1206 1B5
C78 CERSMT_1206 1C6
C79 CERSMT_1206 3A8
C80 CERSMT_1206 1C5
C81 CERSMT_1206 1B4
C82 TASMT_68U_41810001 1D6
C83 CERSMT_1206 1B8
C84 CERSMT_1206 1B8
C85 CERSMT_1206 1B7
C86 CERSMT_1206 1B8
C87 CERSMT_1206 13D7
C88 CERSMT_1206 3A6
C89 CERSMT_1206 1C8
C90 CERSMT_1206 1B7
C91 CERSMT_1206 1B8
C92 CERSMT_1206 1C8
C93 CERSMT_1206 1C8
C94 CERSMT_1206 1A6
C95 CERSMT_1206 1B5
C96 CERSMT_1206 1B5
C97 CERSMT_1206 1A6
C98 CERSMT_1206 1C6
C99 CERSMT_1206 1C6
C100 CERSMT_1206 1B5
C101 CERSMT_1206 1B7
C102 TASMT_68U_41810001 1C7
C103 CERSMT_1206 1B7
C104 CERSMT_1206 1B8
C105 CERSMT_1206 1B7
C106 CERSMT_1206 1B7
C107 CERSMT_1206 1B8
C108 CERSMT_1206 1B8
C109 CERSMT_1206 1B7
C110 CERSMT_1206 1A8
C111 CERSMT_1206 1A5
C112 CERSMT_1206 1A5
C113 CERSMT_1206 1B4
C114 CERSMT_1206 1C6
C115 CERSMT_1206 1B7
C116 CERSMT_1206 1C6
C117 CERSMT_1206 1A6
C118 CERSMT_1206 1B4
C119 CERSMT_1206 1C4
C120 CERSMT_1206 1C4
C121 CERSMT_1206 1C8
C122 CERSMT_1206 1C8
C123 CERSMT_1206 1B7
C124 CERSMT_1206 1C7
C125 CERSMT_1206 1B5
C126 CERSMT_1206 1B5
C127 CERSMT_1206 1C6
C128 CERSMT_1206 1B5
C129 CERSMT_1206 1C8
C130 CERSMT_1206 1B4
C131 CERSMT_1206 1B5
C132 CERSMT_1206 1B5
C133 CERSMT_1206 1C6
C134 CERSMT_1206 1A7
C135 CERSMT_1206 1A7
C136 CERSMT_1206 1C6
C137 CERSMT_1206 1C6
C138 CERSMT_1206 1A7
C139 CERSMT_1206 1B4
C140 CERSMT_1206 1B4
C141 CERSMT_1206 1B4
C142 CERSMT_1206 1B4
C143 CERSMT_1206 1C4
C144 CERSMT_1206 1B4
C145 CERSMT_1206 1B4
C146 CERSMT_1206 1C5
C147 CERSMT_1206 3A6
C148 TASMT_68U_41810001 1D7
C149 CERSMT_1206 1B7
C150 CERSMT_1206 1B8
C151 CERSMT_1206 1B7
C152 CERSMT_1206 1A8
C153 CERSMT_1206 1C7
C154 CERSMT_1206 1C8
C155 CERSMT_1206 1C7
C156 CERSMT_1206 1C7
C157 CERSMT_1206 1A7
C158 CERSMT_1206 1B4
C159 CERSMT_1206 1C8
C160 CERSMT_1206 1C8
C161 CERSMT_1206 1C8
C162 CERSMT_1206 1A7
C163 TASMT_68U_41810001 1C7
C164 CERSMT_1206 1B7
C165 CERSMT_1206 1B7
C166 CERSMT_1206 1A7
C167 CERSMT_1206 1C8
C168 CERSMT_1206 1C7
C169 CERSMT_1206 1A7
C170 CERSMT_1206 1C6
C171 CERSMT_1206 1C5
C172 CERSMT_1206 1B4
C173 CERSMT_1206 13D7
C174 TASMT_68U_41810001 13C7
C175 CERSMT_1206 3A6
C176 CERSMT_1206 1C7
C177 CERSMT_1206 1C7
C178 CERSMT_1206 1C7
C179 CERSMT_1206 1C7
C180 CERSMT_1206 1B4
C181 CERSMT_1206 1C5
C182 CERSMT_1206 1C5
C183 CERSMT_1206 1C7
C184 CERSMT_1206 1A7
C185 CERSMT_1206 13B8
C186 CERSMT_1206 13B8
C187 CERSMT_1206 13D7
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C202 CERSMT_1206 1B7
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C205 CERSMT_1206 1A7
C206 CERSMT_1206 1B7
C207 CERSMT_1206 1B7
C208 CERSMT_1206 1A7
C209 CERSMT_1206 3B6
C210 CERSMT_1206 3B6
C211 CERSMT_1206 3D7
C212 CERSMT_1206 3B6
C213 CERSMT_1206 3D7
C214 CERSMT_1206 3B8
C215 CERSMT_1206 3C6
C216 CERSMT_1206 3B8
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C229 CERSMT_1206 3C8
C230 CERSMT_1206 3D7
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C239 CERSMT_1206 1B6
C240 CERSMT_1206 1C6
C242 CERSMT_1206 4A6
C243 CERSMT_1206 4A6
C246 CERSMT_1206 4A6
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C258 CERSMT_1206 1C5
C259 CERSMT_1206 1B6
C260 CERSMT_1206 1A6
C263 CERSMT_1206 1B6
C264 CERSMT_1206 1B6
C265 CERSMT_1206 1A6
C266 CERSMT_1206 1B6
C267 CERSMT_1206 1C5
C268 CERSMT_1206 1A6
C269 CERSMT_1206 1B6
C271 CERSMT_1206 1A6
C272 CERSMT_1206 1B6
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C296 CERSMT_1206 1C7
C298 CERSMT_1206 1B6
C299 CERSMT_1206 1A7
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C314 CERSMT_1206 1C5
C315 CERSMT_1206 1A6
C316 CERSMT_1206 1B5
C318 CERSMT_1206 1B5
C319 CERSMT_1206 1C4
C322 CERSMT_1206 1A5
C323 CERSMT_1206 1B8
C324 CERSMT_1206 1A8
C325 CERSMT_1206 1A8
C326 CERSMT_1206 1A8
C327 CERSMT_1206 1B8
C329 CERSMT_1206 1A8
C330 CERSMT_1206 1B5
C331 CERSMT_1206 1C6

OEC MEDICAL SYSTEMS, INC.

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C332	CERSMT_1206	1B5
C333	CERSMT_1206	1A5
C334	CERSMT_1206	1C7
C335	CERSMT_1206	1B5
C336	CERSMT_1206	1B5
C337	CERSMT_1206	1C6
C338	CERSMT_1206	1B6
C341	CERSMT_1206	1B6
C342	CERSMT_1206	1A5
C343	CERSMT_1206	1B5
C344	CERSMT_1206	1A5
C345	CERSMT_1206	1A7
C346	CERSMT_1206	1B6
C347	CERSMT_1206	1A7
C348	CERSMT_1206	1B6
C349	CERSMT_1206	1B6
C351	CERSMT_1206	1B7
C352	CERSMT_1206	1C6
C353	CERSMT_1206	1C7
C354	CERSMT_1206	1B7
C355	CERSMT_1206	1B6
C356	CERSMT_1206	1A6
C357	CERSMT_1206	1A6
C358	CERSMT_1206	1B6
C359	CERSMT_1206	1B6
C360	CERSMT_1206	1B6
C362	CERSMT_1206	1B6
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C364	CERSMT_1206	1A6
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C367	CERSMT_1206	1A6
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C369	CERSMT_1206	1A6
C371	CERSMT_1206	1A6
C372	CERSMT_1206	1A7
C373	CERSMT_1206	1C5
C374	CERSMT_1206	1B5
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C379	CERSMT_1206	1C8
C380	CERSMT_1206	1B6
C381	CERSMT_1206	1A6
C382	CERSMT_1206	1A6
C383	CERSMT_1206	1B5
C384	CERSMT_1206	1C6
C387	CERSMT_1206	1A5
C388	CERSMT_1206	1B5
C389	CERSMT_1206	1B5
C390	CERSMT_1206	1B6
C391	CERSMT_1206	1C6
C392	CERSMT_1206	1B7
C393	CERSMT_1206	1C6
C394	CERSMT_1206	1B7
C395	CERSMT_1206	1B6
C396	CERSMT_1206	1C6
C398	CERSMT_1206	1B6
C399	CERSMT_1206	1B4
C404	CERSMT_1206	1B4
C405	CERSMT_1206	1A4
C407	CERSMT_1206	1B6
C408	CERSMT_1206	1A6
C409	CERSMT_1206	1C4
C410	CERSMT_1206	1A6
C411	CERSMT_1206	1C5
C412	CERSMT_1206	1C5
C413	CERSMT_1206	1C5
C414	CERSMT_1206	1C5
C418	CERSMT_1206	1B5
C419	CERSMT_1206	1C5
C420	CERSMT_1206	1C5
C421	CERSMT_1206	1C5
C422	CERSMT_1206	1A6
C423	CERSMT_1206	1B8
C424	CERSMT_1206	1B8
C425	CERSMT_1206	1B8
C430	CERSMT_1206	1B8
C431	CERSMT_1206	1B8
C432	CERSMT_1206	1B8
C433	CERSMT_1206	1B6
C434	CERSMT_1206	1A8
C437	CERSMT_1206	1B8
C438	CERSMT_1206	1B6
C439	CERSMT_1206	1B5
C440	CERSMT_1206	1B5
C441	CERSMT_1206	1B5
C442	CERSMT_1206	1A5
C444	CERSMT_1206	1A5
C445	CERSMT_1206	1B6
C446	CERSMT_1206	1B5
C447	CERSMT_1206	1B7
C448	CERSMT_1206	1A7
C449	CERSMT_1206	1B6
C451	CERSMT_1206	1B6
C453	CERSMT_1206	1A6
C454	CERSMT_1206	1B4
C455	CERSMT_1206	1B5
C457	CERSMT_1206	1A4
C458	CERSMT_1206	1B4
C459	CERSMT_1206	1B6
C460	CERSMT_1206	1A5
C461	CERSMT_1206	1C5
C462	CERSMT_1206	1C4
C464	CERSMT_1206	1B3
C465	CERSMT_1206	1C5
C466	CERSMT_1206	1C5
C467	CERSMT_1206	1B5
C469	CERSMT_1206	1C5
C470	CERSMT_1206	1C5
C473	CERSMT_1206	1B5
C474	CERSMT_1206	1B7
C475	CERSMT_1206	1A8
C476	CERSMT_1206	1C8
C477	CERSMT_1206	1A8
C478	CERSMT_1206	1B8
C479	CERSMT_1206	1C8
C480	CERSMT_1206	1B5
C481	CERSMT_1206	1A6
C483	CERSMT_1206	1B6
C484	CERSMT_1206	1B4
C485	CERSMT_1206	1A4
C488	CERSMT_1206	1B4
C490	CERSMT_1206	1A4
C491	CERSMT_1206	1C6
C492	CERSMT_1206	1B4
C493	CERSMT_1206	1B5
C494	CERSMT_1206	1B7
C495	CERSMT_1206	1A5
C496	CERSMT_1206	1C7
C497	CERSMT_1206	1C7
C498	CERSMT_1206	1B7
C499	CERSMT_1206	1C7
C500	CERSMT_1206	1C7
C501	CERSMT_1206	1B7
C502	CERSMT_1206	1C6
C503	CERSMT_1206	1C6
C504	CERSMT_1206	1A4
C505	CERSMT_1206	1B4
C506	CERSMT_1206	1A4
C512	CERSMT_1206	1B4
C515	CERSMT_1206	1A5
C517	CERSMT_1206	1A7
C518	CERSMT_1206	1A5
C519	CERSMT_1206	1B6
C522	CERSMT_1206	1C5
C523	CERSMT_1206	1A6
C524	CERSMT_1206	1A3
C525	CERSMT_1206	1A6
C526	CERSMT_1206	1B4
C527	CERSMT_1206	1A7
C528	CERSMT_1206	1B3
C529	CERSMT_1206	1A6
C530	CERSMT_1206	1B5
C531	CERSMT_1206	1C5
C532	CERSMT_1206	1C5
C533	CERSMT_1206	1B5
C534	CERSMT_1206	1C5
C535	CERSMT_1206	1C5
C537	CERSMT_1206	1B5
C538	CERSMT_1206	1B7
C540	CERSMT_1206	1B7
C542	CERSMT_1206	1B7
C543	CERSMT_1206	1A8
C544	CERSMT_1206	1A8
C545	CERSMT_1206	1B5
C547	CERSMT_1206	1B5
C548	CERSMT_1206	1C6
C551	CERSMT_1206	1A4
C552	CERSMT_1206	1B7
C553	CERSMT_1206	1B6
C554	CERSMT_1206	1A5
C555	CERSMT_1206	1A6
C556	CERSMT_1206	1A5
C557	CERSMT_1206	1B7
C558	CERSMT_1206	1C7
C560	CERSMT_1206	1C7
C561	CERSMT_1206	1C6
C562	CERSMT_1206	1C7
C566	CERSMT_1206	1B4
C570	CERSMT_1206	1B4
C571	CERSMT_1206	1A4
C572	CERSMT_1206	1A4
C573	CERSMT_1206	1A7
C574	CERSMT_1206	1B4
C576	CERSMT_1206	1A7
C577	CERSMT_1206	1B4
C578	CERSMT_1206	1B4
C579	CERSMT_1206	1B3
C580	CERSMT_1206	1C5
C582	CERSMT_1206	1C5
C583	CERSMT_1206	1B7
C584	CERSMT_1206	1B8
C586	CERSMT_1206	1B7
C587	CERSMT_1206	1B7
C588	CERSMT_1206	1B8
C589	CERSMT_1206	1B8
C591	CERSMT_1206	1B7
C594	CERSMT_1206	1A7
C595	CERSMT_1206	1C8
C596	CERSMT_1206	1C8
C597	CERSMT_1206	1B4
C598	CERSMT_1206	1B4
C599	CERSMT_1206	1A4
C604	CERSMT_1206	1A4
C606	CERSMT_1206	1B4
C608	CERSMT_1206	1B5
C609	CERSMT_1206	1A4
C610	CERSMT_1206	1B7
C612	CERSMT_1206	1B7
C613	CERSMT_1206	1C7
C615	CERSMT_1206	1B7
C616	CERSMT_1206	1B4
C617	CERSMT_1206	1A4
C620	CERSMT_1206	1A3
C621	CERSMT_1206	1A3
C622	CERSMT_1206	1B6
C623	CERSMT_1206	1B4
C624	CERSMT_1206	1C4
C625	CERSMT_1206	1C5
C627	CERSMT_1206	1C5
C628	CERSMT_1206	1C5
C629	CERSMT_1206	1C5
C630	CERSMT_1206	1A8
C631	CERSMT_1206	1C8
C632	CERSMT_1206	1C8
C633	CERSMT_1206	1B8
C635	CERSMT_1206	1C7
C637	CERSMT_1206	1C7
C638	CERSMT_1206	1B8
C642	CERSMT_1206	1C7
C643	CERSMT_1206	1B7
C644	CERSMT_1206	1B7
C646	CERSMT_1206	1B7
C648	CERSMT_1206	1A7
C649	CERSMT_1206	1C7
C650	CERSMT_1206	1A7
C651	CERSMT_1206	1A7
C652	CERSMT_1206	1B7
C653	CERSMT_1206	1A7
C654	CERSMT_1206	1C7
C655	CERSMT_1206	1A7
C656	CERSMT_1206	1C7
C657	CERSMT_1206	1A7
C658	CERSMT_1206	1C7
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C660	CERSMT_1206	1A3
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C663	CERSMT_1206	1B4
C665	CERSMT_1206	1B3
C666	CERSMT_1206	1B3
C668	CERSMT_1206	1B4
C669	CERSMT_1206	1A3
C670	CERSMT_1206	1B6
C671	CERSMT_1206	1C5
C672	CERSMT_1206	1A8
C673	CERSMT_1206	1A7
C674	CERSMT_1206	1A7
C675	CERSMT_1206	13D7
C676	CERSMT_1206	1C7
C677	CERSMT_1206	13C7
C678	CERSMT_1206	13D6
C679	CERSMT_1206	13C7
C680	CERSMT_1206	1C7
C682	CERSMT_1206	1C7
C685	CERSMT_1206	1C7
C686	CERSMT_1206	1C7
C687	CERSMT_1206	1C7
C688	CERSMT_1206	1A7
C689	CERSMT_1206	1B7
C690	CERSMT_1206	1A7
C691	CERSMT_1206	1C5
C692	CERSMT_1206	1C6
C693	CERSMT_1206	1C6
C695	CERSMT_1206	1C6
C696	CERSMT_1206	1C6
C698	CERSMT_1206	1C6
C699	CERSMT_1206	1C5
C700	CERSMT_1206	1B6
C702	CERSMT_1206	1B5
C703	CERSMT_1206	1C6
C704	CERSMT_1206	1A3
C707	CERSMT_1206	1A3
C708	CERSMT_1206	1B4
C709	CERSMT_1206	1B4
C710	CERSMT_1206	1B3
C711	CERSMT_1206	1B3
C712	CERSMT_1206	1B4
C714	CERSMT_1206	1A8
C715	CERSMT_1206	13C7
C716	CERSMT_1206	13D7

OEC MEDICAL SYSTEMS, INC.

SIZE	DWG NO.	REV
D	00-879016	A4
SCALE:		SHEET 32

05-017-9/93

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C718  CERSMT_1206 13C7
C719  CERSMT_1206 1C7
C720  CERSMT_1206 1C7
C721  CERSMT_1206 1C7
C722  CERSMT_1206 1B7
C723  CERSMT_1206 1C7
C724  CERSMT_1206 1A7
C728  CERSMT_1206 1B7
C733  CERSMT_1206 1B7
C734  CERSMT_1206 1A7
C735  CERSMT_1206 1A7
C736  CERSMT_1206 1C7
C737  CERSMT_1206 1A6
C738  CERSMT_1206 1C7
C740  CERSMT_1206 1C7
C741  CERSMT_1206 1A7
C742  CERSMT_1206 1B6
C744  CERSMT_1206 1B6
C745  CERSMT_1206 1C5
C746  CERSMT_1206 1C6
C747  CERSMT_1206 1B6
C748  CERSMT_1206 1C6
C749  CERSMT_1206 1B3
C750  CERSMT_1206 1B5
C751  CERSMT_1206 1A3
C752  CERSMT_1206 1B4
C753  CERSMT_1206 1B3
C754  CERSMT_1206 1B4
C755  CERSMT_1206 1C6
C756  CERSMT_1206 1A4
C757  CERSMT_1206 1B7
C758  CERSMT_1206 1B3
C759  CERSMT_1206 1B3
C760  CERSMT_1206 1A3
C762  CERSMT_1206 1B3
C763  CERSMT_1206 1A7
C764  CERSMT_1206 3A6
C765  CERSMT_1206 13C7
C766  CERSMT_1206 13C7
C767  CERSMT_1206 13D7
C768  CERSMT_1206 1B6
C769  CERSMT_1206 13B7
C770  CERSMT_1206 13C7
C771  CERSMT_1206 13C7
C773  CERSMT_1206 13B7
C774  CERSMT_1206 13C7
C775  CERSMT_1206 13C7
C776  CERSMT_1206 1D4
C777  CERSMT_1206 1D4
DS1   LED_RA_67599204 1D4
DS2   LED_RA_67599204 10B2
DS3   LED_RA_67599204 10B2
DS4   LED_RA_67599204 10B2
DS5   LED_RA_67599204 10B2
DS6   LED_RA_67599204 10B2
DS7   LED_RA_67599204 10B2
DS8   LED_RA_67599204 10B2
DS9   LED_RA_67599204 10B2
E30   JMPST_1X2_90012601 1C8
E31   JMPST_1X2_90012601 1D7
FL1   EMI_FLTR_43600000 1D7
FL2   EMI_FLTR_43600000 1C7
MISC1 ADDONS    1D2
MISC7 ADDONS    1C2
MISC8 ADDONS    1C2
MISC9 ADDONS    1C2
MISC10 ADDONS    1C2
MISC11 ADDONS    1C2
MISC12 ADDONS    1C2
MISC??? ADDONS    1D2
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P1    CONN_EDGE_PCI_124_5V 13A6 13A6 13A6 13A8 13A8
                13A8 13A8 13A8 13A8 13A8 13A8 13A8
                13A8 13A8 13A8 13A8 13A8 13A8 13A8
                13B6 13B6 13B6 13B6 13B6 13B6 13B6
                13B8 13B8 13B8 13B8 13B8 13B8 13B8
                13B8 13B8 13B8 13B8 13B8 13B8 13C6
                13C6 13C6 13C8 13C8 13C8 13C8 13C8
                13C8 13C8 13C8 13C8 13C8 13D8 13D8
                13D8 13D8 13D8 13D8 13D8 13D8 13D8
                13D8 13D8 13D8 13D8 13D8 13D8
P3    MINJRRA_2X4_51411109 1C8
P4    D50RA_40P_51180007 3B8 3B8 3C8 3C8
P5    D50RA_80P_51180008 10A1 10A1 10A1 10A1 10B1 10B1
                10B1 10C1 10C1 10D1 10D1 10D1 10D1
P6    D50RA_40P_51180007 4A8 4B8 4B8 4C8 4C8
P8    HDBKST_2X5_90012602 1D8
R1    RESSMT_1206 3B6
R2    RESSMT_1206 11B4
R3    RESSMT_1206 11A4
R4    RESSMT_1206 8C5
R5    RESSMT_1206 8C5
R6    RESSMT_1206 8C5
R7    RESSMT_1206 3A6
R8    RESSMT_1206 10D1
R9    RESSMT_1206 3B7
R10   RESSMT_1206 3B7
R11   RESSMT_1206 3D7
R12   RESSMT_1206 3B7
R13   RESSMT_1206 3D7
R14   RESSMT_1206 3B8
R15   RESSMT_1206 3C7
R16   RESSMT_1206 3B8
R17   RESSMT_1206 3B7
R18   RESSMT_1206 3A6
R19   RESSMT_1206 3C8
R20   RESSMT_1206 3D7
R21   RESSMT_1206 3D8
R22   RESSMT_1206 3D7
R23   RESSMT_1206 3D8
R24   RESSMT_1206 3D8
R25   RESSMT_1206 3D8
R26   RESSMT_1206 11B4
R27   RESSMT_1206 8B5
R28   RESSMT_1206 1D5
R29   RESSMT_1206 4B7
R30   RESSMT_1206 4A6
R31   RESSMT_1206 4A6
R32   RESSMT_1206 4A6
R33   RESSMT_1206 4A6
R34   RESSMT_1206 4A6
R35   RESSMT_1206 4A6
R36   RESSMT_1206 4A6
R37   RESSMT_1206 4A6
R38   RESSMT_1206 4A6
R39   RESSMT_1206 4C7
R40   RESSMT_1206 4A6
R41   RESSMT_1206 4D6
R42   RESSMT_1206 3A7
R43   RESSMT_1206 3D6
R44   RESSMT_1206 3D4
R45   RESSMT_1206 3C3
R46   RESSMT_1206 3C3
R47   RESSMT_1206 11D6
R48   RESSMT_1206 4D6
R49   RESSMT_1206 1D4
R50   RESSMT_1206 1D5
R51   RESSMT_1206 1C5
R52   RESSMT_1206 15B8
R53   RESSMT_1206 10B4
R54   RESSMT_1206 10B4
R55   RESSMT_1206 10D2
R56   RESSMT_1206 10D3
R57   RESSMT_1206 1D8
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R58   RESSMT_1206 3A6
R59   RESSMT_1206 3C2
R60   RESSMT_1206 3C2
R61   RESSMT_1206 10D7
R62   RESSMT_1206 9D8
R63   RESSMT_1206 6D6
R64   RESSMT_1206 6D3
R65   RESSMT_1206 1D8
R66   RESSMT_1206 1D7
R67   RESSMT_1206 3C2
R68   RESSMT_1206 3C2
R69   RESSMT_1206 14B4
R70   RESSMT_1206 10A4
R71   RESSMT_1206 6D4
R72   RESSMT_1206 3A2
R73   RESSMT_1206 3A2
R74   RESSMT_1206 15C8
R75   RESSMT_1206 13D4
R76   RESSMT_1206 3B8
R77   RESSMT_1206 3A8
R78   RESSMT_1206 14D6
R79   RESSMT_1206 14B3
R80   RESSMT_1206 8D6
R81   RESSMT_1206 8D6
R82   RESSMT_1206 13D3
R83   RESSMT_1206 12B2
R84   RESSMT_1206 6D5
R85   RESSMT_1206 3A2
R86   RESSMT_1206 3A2
R87   RESSMT_1206 3A6
R88   RESSMT_1206 12D6
R89   RESSMT_1206 14D6
R90   RESSMT_1206 14A5
R91   RESSMT_1206 5B4
R92   RESSMT_1206 14D3
R93   RESSMT_1206 13A3
R94   RESSMT_1206 13A3
R95   RESSMT_1206 13A3
R96   RESSMT_1206 14D6
R97   RESSMT_1206 15D8
R98   RESSMT_1206 4D5
R99   RESSMT_1206 9D3
R100  RESSMT_1206 9D6
R101  RESSMT_1206 3A6
R102  RESSMT_1206 7C8
R103  RESSMT_1206 7C8
R104  RESSMT_1206 7C8
R105  RESSMT_1206 7B8
R106  RESSMT_1206 12D6
R107  RESSMT_1206 13A3
R108  RESSMT_1206 13A3
R109  RESSMT_1206 13A3
R110  RESSMT_1206 13A3
R111  RESSMT_1206 13A3
R112  RESSMT_1206 13A3
R113  RESSMT_1206 13A3
R114  RESSMT_1206 13C2
R115  RESSMT_1206 14D6
R116  RESSMT_1206 5C5
R117  RESSMT_1206 9D3
R118  RESSMT_1206 7D5
R119  RESSMT_1206 5D4
R120  RESSMT_1206 5D4
R121  RESSMT_1206 5D4
R122  RESSMT_1206 7B8
R123  RESSMT_1206 7B8
R124  RESSMT_1206 7B8
R125  RESSMT_1206 7B8
R126  RESSMT_1206 12D4
R127  RESSMT_1206 12D7
R128  RESSMT_1206 13D4
R129  RESSMT_1206 13A3
R130  RESSMT_1206 13A3
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R131  RESSMT_1206 13A3
R132  RESSMT_1206 13A3
R133  RESSMT_1206 13A3
R134  RESSMT_1206 13A3
R135  RESSMT_1206 9D6
R136  RESSMT_1206 13D4
R137  RESSMT_1206 14D5
R138  RESSMT_1206 3A6
R139  RESSMT_1206 13B3
R140  RESSMT_1206 9C3
R141  RESSMT_1206 7D6
R142  RESSMT_1206 3A6
R143  RESSMT_1206 13A3
R144  RESSMT_1206 13B3
R145  RESSMT_1206 13B3
R146  RESSMT_1206 13A3
R147  RESSMT_1206 13B3
R148  RESSMT_1206 13B3
R149  RESSMT_1206 13B3
R150  RESSMT_1206 13B3
R151  RESSMT_1206 13B3
R152  RESSMT_1206 9C5
R153  RESSMT_1206 9C5
R154  RESSMT_1206 7D7
R155  RESSMT_1206 1D4
R156  RESSMT_1206 1D4
R203  RESSMT_1206 11A4
R204  RESSMT_1206 11A4
R205  RESSMT_1206 8C5
R206  RESSMT_1206 11B4
R208  RESSMT_1206 10D6
R209  RESSMT_1206 10B6
R210  RESSMT_1206 10B4
R211  RESSMT_1206 10D4
R215  RESSMT_1206 15C8
R217  RESSMT_1206 10D3
R218  RESSMT_1206 3D4
R219  RESSMT_1206 3D5
R220  RESSMT_1206 8D7
R221  RESSMT_1206 13D3
R222  RESSMT_1206 11D6
R223  RESSMT_1206 11D7
R224  RESSMT_1206 6C8
R225  RESSMT_1206 6B8
R226  RESSMT_1206 13D4
R227  RESSMT_1206 5C8
R228  RESSMT_1206 9D8
R229  RESSMT_1206 5D6
R230  RESSMT_1206 13D3
R231  RESSMT_1206 14D7
R232  RESSMT_1206 5D8
R233  RESSMT_1206 7B8
R234  RESSMT_1206 7C8
R235  RESSMT_1206 7B8
R236  RESSMT_1206 7C8
R237  RESSMT_1206 7C8
R238  RESSMT_1206 13D4
R239  RESSMT_1206 13D4
R240  RESSMT_1206 7B8
R241  RESSMT_1206 7B8
R242  RESSMT_1206 7B8
R243  RESSMT_1206 9D7
R244  RESSMT_1206 13D6
R245  RESSMT_1206 13D6
R246  RESSMT_1206 13B3
R247  RESSMT_1206 13B3
R248  RESSMT_1206 13B3
R249  RESSMT_1206 13B3
R250  RESSMT_1206 13B3
R251  RESSMT_1206 13B3
R252  RESSMT_1206 7C3
TP1   TEST_POINT_COLOR 1D7
TP2   TEST_POINT_COLOR 1C7
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OEC MEDICAL SYSTEMS, INC.

SIZE	DWG NO.	REV
D	00-879016	A4
SCALE:		SHEET 33

TP3	TEST_POINT_COLOR 3B6
TP4	TEST_POINT_COLOR 3D4
TP5	TEST_POINT_COLOR 3D4
TP6	TEST_POINT_COLOR 1D6
TP7	TEST_POINT_COLOR 1D6
TP8	TEST_POINT_COLOR 3D4
TP9	TEST_POINT_COLOR 1D6
TP10	TEST_POINT_COLOR 1D6
TP11	TEST_POINT_COLOR 13C7
TP12	TEST_POINT_COLOR 13D4
TP13	TEST_POINT_COLOR 13D3
TP14	TEST_POINT_COLOR 1D6
U1	74LCX16374 3D7
U2	SDRAM_1MX16 11B4
U3	SDRAM_1MX16 11C4
U4	TC551664 8B5
U5	SDRAM_1MX16 8C5
U6	74LPT16652_S 4B6 4C6
U7	SRAM_32KX8 10D6
U8	74LCX16374 10D2
U9	74LCX16374 10C2
U10	EPC1 1D5
U11	74LCX16245_S 7D3 15C7
U12	74LCX16245 8C4
U13	74LCX16245_S 1D4 15C7
U14	74LCX16374 4C6 15B7
U15	74LCX16245 10D7
U16	74LCX16245_S 10A6 10C6
U17	SRAM_32KX8 10B6
U19	EPC1 1C5
U20	SDRAM_1MX16 3C3
U21	SDRAM_1MX16 3B3
U23	74LCX16245 14C4
U25	49FCT3806 3B8
U26	74LCX16245 8B4
U28	74LCX16245 10C7
U30	485506 6C7
U31	485506 6B7
U32	TC551664 6C3
U33	SDRAM_1MX16 12C5
U34	74LCX16245 12D3
U35	74LCX16245 12C3
U37	74LCX16245 14B4
U38	74LCX16245 9B3
U40	74LCX16245 6C3
U41	74LCX16245 5D2
U42	74LCX16245 6D3
U43	74LCX16245_S 5C3 12B3
U44	485506 5D7
U45	485506 5C7
U46	SRAM_32KX8 5B4
U47	SDRAM_1MX16 12B5
U50	74LCX16245_S 9C2 15D7
U51	74LCX16245 5B3
U52	74LCX16245 5D3
U54	TC551664 5D4
U55	TC551664 12D4
U56	VREG_3X3V_62601971 1C6
U57	FIFO_512X36X2_BMBS 13C3
U58	48410 7C3
U60	VRAM_256KX16 9B5
U61	VRAM_256KX16 9C4
U63	SDRAM_1MX16 7B5
U64	SDRAM_1MX16 7C5
U65	NM93CS46_VCC 13D5
U67	SRAM_32KX8 9C3
XU56	HTSNK_TO220HU_66899846 1C6

OEC MEDICAL SYSTEMS, INC.

SIZE D | DWG NO. 00-879016 | REV A4

SCALE: | SHEET 34

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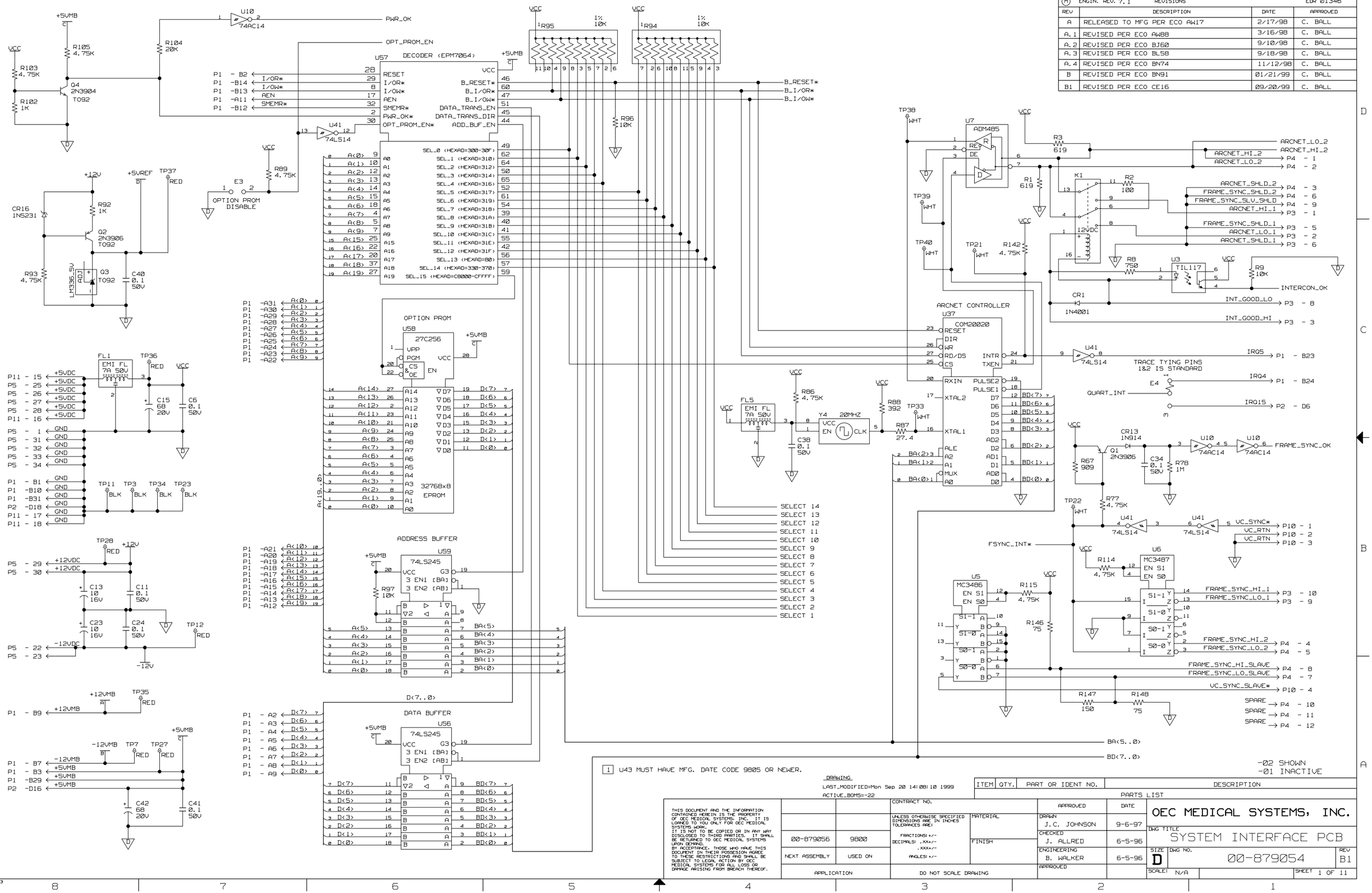
DWG NO. 00-879054	SHT 1	REV B1

M	ENGIN. REV. 7.1 REVISIONS		EDR 01346
REV	DESCRIPTION	DATE	APPROVED
A	RELEASED TO MFG PER ECO AW17	2/17/98	C. BALL
A.1	REVISED PER ECO AW88	3/16/98	C. BALL
A.2	REVISED PER ECO BJ60	9/10/98	C. BALL
A.3	REVISED PER ECO BL58	9/18/98	C. BALL
A.4	REVISED PER ECO BN74	11/12/98	C. BALL
B	REVISED PER ECO BN91	01/21/99	C. BALL
B1	REVISED PER ECO CE16	09/20/99	C. BALL



1 U43 MUST HAVE MFG. DATE CODE 9805 OR NEWER.

-02 SHOWN
-01 INACTIVE

DRAWING
LAST_MODIFIED=Mon Sep 20 14:08:10 1999
ACTIVE_BOMS=-22

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ITEM	QTY.	PART OR IDENT NO.	DESCRIPTION

PARTS LIST

		CONTRACT NO.		APPROVED	DATE
		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS=+/- DECIMALS= .XX+/- .XXX+/- ANGLES=+/-	MATERIAL	DRAWN J.C. JOHNSON	9-6-97
				CHECKED J. ALLRED	6-5-96
00-879056	9800		FINISH	ENGINEERING B. WALKER	6-5-96
NEXT ASSEMBLY	USED ON			APPROVED	
APPLICATION		DO NOT SCALE DRAWING			

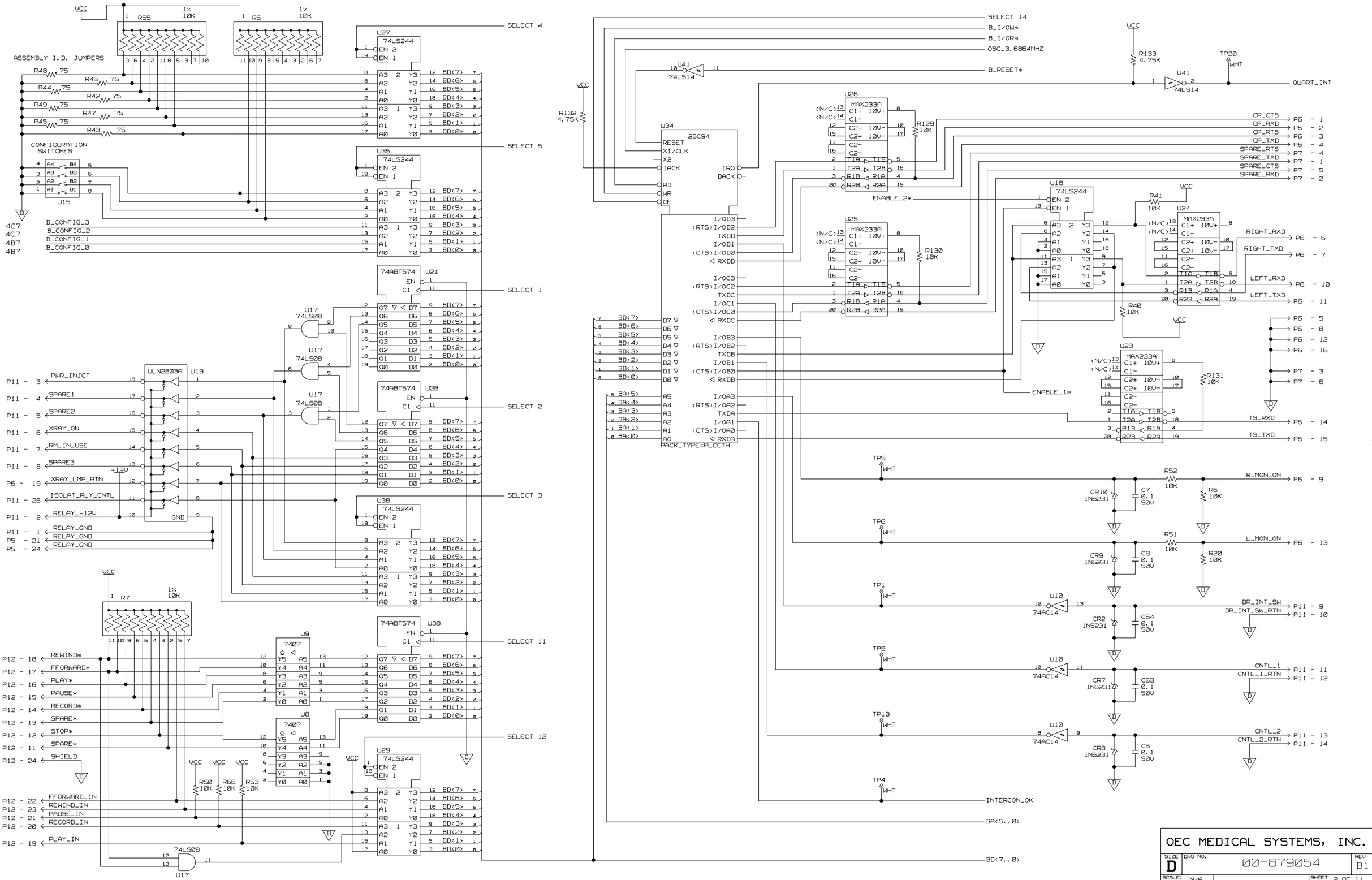
OEC MEDICAL SYSTEMS, INC.

DWG TITLE: SYSTEM INTERFACE PCB

SIZE D | DWG NO. 00-879054 | REV B1

SCALE: N/A | SHEET 1 OF 11

05-016-9/93


ASSEMBLY I.D. JUMPERS
CONFIGURATION SWITCHES
B_CONFIG_3
B_CONFIG_2
B_CONFIG_1
B_CONFIG_0
SELECT 4
SELECT 5
SELECT 1
SELECT 2
SELECT 3
SELECT 11
SELECT 12
SELECT 14
B_I/OW*
B_I/OR*
OSC_3.6864MHZ
B_RESET*
QUART_INT
INTERCON_OK
BA<5..0>
BD<7..0>
ENABLE_2*
ENABLE_1*
PACK_TYPE=PLCCTH
CP_CTS
CP_RXD
CP_RTS
CP_TXD
SPARE_RTS
SPARE_TXD
SPARE_CTS
SPARE_RXD
RIGHT_RXD
RIGHT_TXD
LEFT_RXD
LEFT_TXD
TS_RXD
TS_TXD
R_MON_ON
L_MON_ON
DR_INT_SW
DR_INT_SW_RTN
CNTL_1
CNTL_1_RTN
CNTL_2
CNTL_2_RTN
PWR_INJCT
SPARE1
SPARE2
XRAY_ON
RM_IN_USE
SPARE3
XRAY_LMP_RTN
ISOLAT_RLY_CNTL
RELAY_+12V
RELAY_GND
REWIND*
FFORWARD*
PLAY*
PAUSE*
RECORD*
SPARE*
STOP*
SPARE*
SHIELD
FFORWARD_IN
REWIND_IN
PAUSE_IN
RECORD_IN
PLAY_IN
26C94
MAX233A
74LS244
74ABT574
74AC14
74LS08
74LS14
ULN2803A
7407

R27 1% 10K

EMI FL 7A 50V — FL4

C130 0.1 50V

R141 4.75K

Y3 3.6864MHZ

TP29 WHT

P5 - 2 ← CINE_+5V_SEN — R22 1K
P5 - 3 ← CINE_+3.3V_SEN — R23 1K
P5 - 4 ← VIDCNT_+5V_SEN — R24 1K
P5 - 5 ← VIDCNT_+3.3V_SEN — R25 1K
P5 - 6 ← DSPCNT_+5V_SEN — R26 1K
P5 - 7 ← DSPCNT_+3.3V_SEN — R28 1K
P5 - 8 ← IP_+5V_SEN — R29 1K
P5 - 9 ← IP_+3.3V_SEN — R31 1K
P5 - 10 ← PCIDA_+5V_SEN — R32 1K
P5 - 11 ← CPP_+5V_SEN — R33 1K

C54 0.1 50V, C53 0.1 50V, C52 0.1 50V, C51 0.1 50V, C50 0.1 50V, C49 0.1 50V, C48 0.1 50V, C47 0.1 50V, C46 0.1 50V, C45 0.1 50V

R107 10K, R108 10K, R109 10K, R110 10K

P5 - 12 ← CPP_+12V_SEN — R34 15K
P5 - 13 ← PCIDA_+12V_SEN — R35 15K
P5 - 14 ← SPARE_+12V_SEN — R37 15K
P5 - 16 ← SPARE_+12V_SEN — R38 15K

C44 0.1 50V, C62 0.1 50V, C61 0.1 50V, C43 0.1 50V

R21 10K

B_I/OR*
B_I/OW*
SELECT 8
OSC_3.6864MHZ
SELECT 9
SELECT 10

U42 ADC10158 — C127 0.1 50V, C27 10 25V
U44 ADC10158 — C123 0.1 50V, C28 10 25V
U45 ADC10158 — C114 0.1 50V, C33 10 25V

+5VREF, VCC

BD<7>
BD<6>
BD<5>
BD<4>
BD<3>
BD<2>
BD<1>
BD<0>

R4 10K

JUMPER TYING PINS 1&2 IS STANDARD — E2

R69 10K — CS_LED

U4 74ABT574 — SELECT 13
U31 74ABT574
U2 TIL311
U1 TIL311

DATA<7>
DATA<6>
DATA<5>
DATA<4>
DATA<3>
DATA<2>
DATA<1>
DATA<0>

U13 ULN2803A

PWR_OK
INTERCON_OK
OPT_PROM_EN
FRAME_SYNC_OK

SELECT 6 — U22 74ABT574
SELECT 7 — U14 74ABT574

BD<7..0>

DS1 LED_10BAR_YEL — R125 243, R10 243, R124 243, R11 243, R123 243, R12 243, R122 243, R13 243, R121 243, R14 243
DS2 LED_10BAR_YEL — R120 243, R15 243, R119 243, R16 243, R118 243, R17 243, R117 243, R18 243, R116 243, R19 243

E1

+12V, -12V, VCC

R55 39.2 — C12 0.1 50V
C9 0.1 50V — R56 110K — R58 200K — R59 20K — R57 210K
TEMP_SEN_1_+ — P5 - 17
TEMP_SEN_1_- — P5 - 18
U12 TL082B — R30 8.25K — CR11 1N914

C14 0.1 50V — R63 110K — R64 200K — R62 20K — R61 210K
TEMP_SEN_2_+ — P5 - 19
TEMP_SEN_2_- — P5 - 20
U12 TL082B — R36 8.25K — CR15 1N914

R60 39.2 — C10 0.1 50V

+12VMB, -12VMB, +5VMB

R145 12.7K — C141 0.1 50V — R144 6.81K
R143 2K — C140 0.1 50V — R83 10K
R139 12.7K — C129 0.1 50V — R140 6.81K
R138 2K — C121 0.1 50V — R136 10K

XRAY_LMP — P6 - 18
AMB_LIGHT_2 — P6 - 21
AMB_LIGHT_1 — P6 - 20

C122 0.1 50V — R137 1K

C74 0.1 — R113 10K
R126 39.2 — C80 0.1 50V — C81 0.01 50V — R128 39.2
R112 28K — U11 TL082B — R111 8.25K — CR12 1N914
R54 28K — U11 TL082B — R135 8.25K — CR14 1N914
C75 0.1 — R134 10K

OEC MEDICAL SYSTEMS, INC.

SIZE D | DWG NO. 00-879054 | REV B1 | SCALE: N/A | SHEET 3 OF 11

TP15 WHT
VCC
R70 4.75K
B_RESET*
TP14 WHT
TP18 WHT
VCC
U33 MAX1232
PBRST
ST RST
TOL RST
TD
WD_STRB
R76 0
TP19 WHT
16MHZ_CLK
VCC
FL3 EMI FL 7A 50V
Y1 16MHZ
EN CLK
VCC
C17 0.1 50V
R75 27.4
VCC
R71 0.25W 2% 10K
VCC
R74 0.25W 2% 10K
U43 MC68HC16Z1
XTAL
CLKOUT
RESET
VCC
R73 1K
TP25 WHT
RESET*
TP26 WHT
R81 392
U52 EPM7032
TRI_STATE
16 MHZ CLK
CS_8BIT
ARC_INT
RESET
HC_DS
RD_WR
DS
FSYNC_INT
A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
INT_FS READ WRITE1 WRITE2 ARC_DS CS_ARCNET INTR_ARC
REMOTE
TP16 WHT
TP17 WHT
INT_ARC*
INT_FS*
EXTAL
MODCLK/XX
TSC TSTME IRQ7/XX IRQ6/XX IRQ5/XX IRQ4/XX IRQ3/XX IRQ2/XX IRQ1/XX HALT DSACK1/XX DSACK0/XX DSCLK BKPT BERR XFC VSYN PAI PCLK
FREEZE/QUOT IPIPE1/DSI IPIPE0/DSO
FREEZE DSI DSO
XX/CS10 XX/CS9 XX/CS8 XX/CS7 XX/CS6 XX/CS5 XX/CS4 XX/CS3 XX/CS2 XX/CS1 XX/CS0 CSBOOT WR RD DS AS
CS_8BIT*
CS_LED
CS_SRAM1_UB*
CS_SRAM1_LB*
CS_BOOT*
RD_WR*
DS*
VCC
R91 10K
R84 10K
TP31 WHT TP32 WHT TP30 WHT
FSYNC_INT*
OUT WD_STRB
OUT MODEM/SERIAL*
PGP7/XX PGP6/XX PGP5/XX PGP4/XX PGP3/XX PGP2/XX PGP1/XX PGP0/XX
B_CONFIG_3 B_CONFIG_2 B_CONFIG_1 B_CONFIG_0
PWMA PWMB VSTBY AVEC
OUT P055
OUT P056
OUT MOD_TXD
R72 392
MOD_RXD
RXD PQS7/TXD PQS6/PCS3 PQS5/PCS2 PQS4/PCS1 PCS0 SCK MOSI MISO
P054
PC50
SCK IN
MOSI
VCC
VDDA VRH AN7/PADA7 AN6/PADA6 AN5/PADA5 AN4/PADA4 AN3/PADA3 AN2/PADA2 AN1/PADA1 AN0/PADA0 VRL VSSA
DS0 → P14 - 10
DSI → P14 - 9
RESET* → P14 - 8
FREEZE → P14 - 7
BKPT → P14 - 6
BERR → P14 - 5
DS* → P14 - 4
P14 - 3
P14 - 2
P14 - 1
NO_STUFF=REF
DO NOT STUFF
UC_ADDR<18..0>
A18 A17 A16 A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0
PE6 PE7
U40 74HCT245
U49 74HCT245
G3
3 EN1 [BA]
3 EN2 [AB]
UC_DATA<15..0>
DATA<15..0>
RD_WR*
VCC
R82 2.2K
R85 2.2K
DATA<15..0>
U53 74HC244
U55 74HC244
U54 74HC244
EN 2
EN 1
A3 A2 A1 A0
Y3 Y2 Y1 Y0
R90 392
ADDRESS<17..0>

00-879054-02 SCH, PCB, SYSTEM INTERFACE, 9800
00-879055-02 PCB, SYSTEM INTERFACE, A/F
00-879056-60 SPEC, PERF, PCB, SYS INTERFACE 9800
ASM_U57
00-879719-01 ASM, FW, DECODER, SYS INTF
ASM_U51
00-881343-06 ASM, FW, HIGH ORDER, SERVICE PROCESSOR, 9800
ASM_U50
00-881343-05 ASM, FW, LOW ORDER, SERVICE PROCESSOR, 9800
ASM_U52
00-880908-01 ASM, FW, RMT DIAG, SYS-INT, 9800
ASM_U58
00-879413-01 ASM, FW, OPT ROM, SYS INTF, 9800
00-900985-01 BRACKET, PCI-PCB, ISA
12-225104-04 SCR, SEMS SPR, PAN, TRX, 4-40, 1/4, SZC 4
00-900456-01 BRKT, END, PCB

OEC MEDICAL SYSTEMS, INC.

SIZE	DWG NO.	REV
D	00-879054	B1
SCALE:	SHEET 4 OF 11	

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CS_SRAM1_UB*
CS_SRAM1_LB*
WRITE2*
CS_BOOT*
WRITE1*
READ*

U51 AM29F010 SPEED=70_NS
U50 AM29F010 SPEED=70_NS
U48 PD431000
U47 PD431000
128K X8 FLASH
128K x8 SRAM

DATA<15..0>
ADDRESS<17..0>

VCC

C108 C143 C165 C78 C87 C60 C32 C115 C124 C73 C106 C105 C104 C103 C68 C67 C91 C85 C99 C94 C89 C102 C95 C58 C71 C117 C118 C55 0.1
C107 C142 C167 C79 C88 C59 C119 C120 C168 C116 C30 C126 C125 C84 C100 C93 C4 C18 C19 C20 C21 C2 C3 C92 C86 C96 C90 C101 0.01

C29 C31 C113 C83 C82 0.1
C22 C1 C72 C26 C25 0.01

C144 C174 C173 0.01

+5VMB
C157 C169 C156 C159 C182 C181 C161 0.1
U213 U212

C158 C170 C155 C172 C183 C171 C160 0.01

C150 C162 C164 C175 C177 C179 C151 C153 C97 C138 C135 C109 C137 C76 C131 C145 C147 C133 C112 C69 0.1
C149 C163 C166 C176 C178 C180 C152 C154 C98 C139 C128 C110 C136 C77 C132 C146 C148 C134 C111 C70 0.01

REFERENCE DESIGNATIONS

HIGHEST	UNUSED
C183	
CR16	
DS2	
E4	
FL5	
K1	
P14	
Q4	
R148	
TP43	
U59	
Y4	

P11 - 25 CONFIG_3 C65 0.01 CR6 1N5231
P11 - 24 CONFIG_2 C56 0.01 CR5 1N5231
P11 - 23 CONFIG_1 C66 0.01 CR3 1N5231
P11 - 22 CONFIG_0 C57 0.01 CR4 1N5231

U39 74AC14

ENABLE_1*
B_CONFIG_3
B_CONFIG_2
B_CONFIG_1
B_CONFIG_0
ENABLE_2*

REMOTE DIAGNOSTICS NODE

RESET*
RD_WR*
ARC_DS*
CS_ARCNET*
ARCNET_HI_2
ARCNET_LO_2
ARC_INT*

U20 ADM485
U36 COM20020
R39 392
TP2 TP8 TP41 TP42 TP43 TP24 WHT

VCC
R68 10K
R79 392
R80 27.4
FL2 EMI FL 7A 50V
Y2 20MHZ
C16 0.1 50V
TP13

U32 74LS244

MODEM/SERIAL*
MOD_TXD
MOD_RXD
TXD
RXD

U16 MAX233A

R127 10K
DIAG_TXD
DIAG_RXD
DIAG_RTN
P11 - 19
P11 - 20
P11 - 21

+12V
C36 1 35V
C35 1 35V
C39 1 35V
C37 1 35V

U46 MAX239

MD_TXD P12 - 3
MD_DTR P12 - 4
MD_RTS P12 - 7
MD_DCD P12 - 1
MD_RXD P12 - 2
MD_DSR P12 - 6
MD_CTS P12 - 8
MD_RI P12 - 9
P12 - 5

P056
P055
P054
PC50
SCK
MOSI

OEC MEDICAL SYSTEMS, INC.

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```
      *** Signal Cross-Reference ***
         --- for the entire design --

16MHZ_CLK         4D5 4D2
A <19..0>         1A6 1B6 1B7 1C7 1B6 1C6 1D6
ADDRESS <17..0>   4A1 5A7 5C8
ARCNET_HI_2       1D1 5B8
ARCNET_LO_2       1D1 5A8
ARC_DS *          4D1 5B7
ARC_INT *         5A5 4D2
BA <5..0>         1A2 1A6 1B6 2A3 1B3 2C5
BD <7..0>         1A2 1A5 1B2 1C2 2A3 2A6 2B6 2C5 2C6
                  2D6 3B4 3C4 3D4 2A6 2B6 2C6 3A3 3A4
                  3B3 3D3
BERR              4A8
BKPT              4A8
B_CONFIG_0        5B3 2C8 4B7
B_CONFIG_1        5B3 2C8 4B7
B_CONFIG_2        5B3 2C8 4C7
B_CONFIG_3        5C3 2C8 4C7
B_I/OR *          1D4 2D3 3C5
B_I/OW *          1D4 2D3 3C5
B_RESET *         1D4 4D5 2D3
CONFIG_0          5B7
CONFIG_1          5B6
CONFIG_2          5B5
CONFIG_3          5C5
CS_8BIT *         4C5
CS_ARCNET *       4D1 5B7
CS_BOOT *         4C5 5D8
CS_LED            4C5 3D2
CS_SRAM1_LB *     4C5 5D8
CS_SRAM1_UB *     4C5 5D8
D <7..0>          1A6 1A7 1B5 1C5 1A6
DATA <15..0>      4B4 5A5 3C2 3D2 4A3 5C8
DIAG_RTN          5A2
DIAG_RXD          5A2
DIAG_TXD          5A2
DS *              4A8 4C3
DSI               4A8 4C5
DSO               4B8 4C5
ENABLE_1 *        2C2 5B4
ENABLE_2 *        5B3 2D3
FRAME_SYNC_OK     1B1 3C3
FREEZE            4A8 4D5
FSYNC_INT *       1B2 4D3
INTERCON_OK       1C1 2A3 3C3
INT_ARC *         4C8 4D1
INT_FS *          4C8 4D1
ISOLAT_RLY_CNTL   2B8
MD_CTS            5B1
MD_DCD            5B1
MD_DSR            5B1
MD_DTR            5B1
MD_RI             5B1
MD_RTS            5B1
MD_RXD            5B1
MD_TXD            5B1
MODEM/SERIAL *    4C7 5A4
MOD_RXD           5A4 4B7
MOD_TXD           4B7 5A4
MOSI              5A2 4B7
OPT_PROM_EN       1D6 3C3
OSC_3.6864MHZ     3C5 2D3
PC50              5A2 4B7
PO54              5A2 4B7
PO55              4B7 5B2
PO56              4B7 5B2
PWR_OK            1D6 3C3
QUART_INT         1C2 2D1
RD_WR *           4C3 4B4 5B7
READ *            4D1 5D8
RESET *           4A8 4D4 5B7
SCK               5A2 4B7
SELECT 1          1B4 2C5
SELECT 2          1B4 2C5
SELECT 3          1B4 2B5
SELECT 4          1B4 2D5
SELECT 5          1B4 2D5
SELECT 6          1B4 3C3
SELECT 7          1B4 3B3
SELECT 8          1B4 3C5
SELECT 9          1B4 3C5
SELECT 10         1B4 3C5
SELECT 11         1B4 2B5
SELECT 12         1B4 2A5
SELECT 13         1B4 3D2
SELECT 14         1B4 2D3
UC_ADDR <18..0>   4C5
UC_DATA <15..0>   4B5
WD_STRB           4C7 4D5
WRITE1 *          4D1 5D8
WRITE2 *          4D1 5D8
```

OEC MEDICAL SYSTEMS, INC.

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*** Unit Cross-Reference ***
--- for the entire design --

C1	CERSMT_1206	5C4
C2	CERSMT_1206	5D1
C3	CERSMT_1206	5D1
C4	CERSMT_1206	5D2
C5	CERSMT_1206	2A2
C6	CERSMT_1206	1C7
C7	CERSMT_1206	2B2
C8	CERSMT_1206	2B2
C9	CERSMT_1206	3B7
C10	CERSMT_1206	3A8
C11	CERSMT_1206	1B8
C12	CERSMT_1206	3B8
C13	TASMT_6032	1B8
C14	CERSMT_1206	3B7
C15	TAR_68U_41609452	1C7
C16	CERSMT_1206	5A7
C17	CERSMT_1206	4D6
C18	CERSMT_1206	5D2
C19	CERSMT_1206	5D2
C20	CERSMT_1206	5D2
C21	CERSMT_1206	5D2
C22	CERSMT_1206	5C4
C23	TASMT_6032	1B8
C24	CERSMT_1206	1B8
C25	CERSMT_1206	5C4
C26	CERSMT_1206	5C4
C27	TAR_10U_41547902	3D4
C28	TAR_10U_41547902	3C4
C29	CERSMT_1206	5D5
C30	CERSMT_1206	5D3
C31	CERSMT_1206	5D4
C32	CERSMT_1206	5D4
C33	TAR_10U_41547902	3B4
C34	CERSMT_1206	1B2
C35	TAR_1U_41547921	5B2
C36	TAR_1U_41547921	5B1
C37	TAR_1U_41547921	5B2
C38	CERSMT_1206	1C4
C39	TAR_1U_41547921	5B1
C40	CERSMT_1206	1C7
C41	CERSMT_1206	1A7
C42	TAR_68U_41609452	1A8
C43	CERSMT_1206	3B6
C44	CERSMT_1206	3B6
C45	CERSMT_1206	3C6
C46	CERSMT_1206	3C6
C47	CERSMT_1206	3C6
C48	CERSMT_1206	3C6
C49	CERSMT_1206	3C6
C50	CERSMT_1206	3C6
C51	CERSMT_1206	3C7
C52	CERSMT_1206	3C7
C53	CERSMT_1206	3C7
C54	CERSMT_1206	3C7
C55	CERSMT_1206	5D1
C56	CERSMT_1206	5B5
C57	CERSMT_1206	5B6
C58	CERSMT_1206	5D1
C59	CERSMT_1206	5D4
C60	CERSMT_1206	5D4
C61	CERSMT_1206	3B6
C62	CERSMT_1206	3B6
C63	CERSMT_1206	2A2
C64	CERSMT_1206	2B2
C65	CERSMT_1206	5B5
C66	CERSMT_1206	5B6
C67	CERSMT_1206	5D2
C68	CERSMT_1206	5D3
C69	CERSMT_1206	5C2
C70	CERSMT_1206	5C2
C71	CERSMT_1206	5D1
C72	CERSMT_1206	5C4
C73	CERSMT_1206	5D3
C74	CERSMT_1206	3A6
C75	CERSMT_1206	3A5
C76	CERSMT_1206	5C3
C77	CERSMT_1206	5C3
C78	CERSMT_1206	5D4
C79	CERSMT_1206	5D4
C80	CERSMT_1206	3A7
C81	CERSMT_1206	3A7
C82	CERSMT_1206	5D4
C83	CERSMT_1206	5D4
C84	CERSMT_1206	5D3
C85	CERSMT_1206	5D2
C86	CERSMT_1206	5D1
C87	CERSMT_1206	5D4
C88	CERSMT_1206	5D4
C89	CERSMT_1206	5D2
C90	CERSMT_1206	5D1
C91	CERSMT_1206	5D2
C92	CERSMT_1206	5D1
C93	CERSMT_1206	5D2
C94	CERSMT_1206	5D2
C95	CERSMT_1206	5D1
C96	CERSMT_1206	5D1
C97	CERSMT_1206	5C4
C98	CERSMT_1206	5C3
C99	CERSMT_1206	5D2
C100	CERSMT_1206	5D3
C101	CERSMT_1206	5D1
C102	CERSMT_1206	5D2
C103	CERSMT_1206	5D3
C104	CERSMT_1206	5D3
C105	CERSMT_1206	5D3
C106	CERSMT_1206	5D3
C107	CERSMT_1206	5D5
C108	CERSMT_1206	5D5
C109	CERSMT_1206	5C3
C110	CERSMT_1206	5C3
C111	CERSMT_1206	5C2
C112	CERSMT_1206	5C2
C113	CERSMT_1206	5D4
C114	CERSMT_1206	3B4
C115	CERSMT_1206	5D4
C116	CERSMT_1206	5D3
C117	CERSMT_1206	5D1
C118	CERSMT_1206	5D1
C119	CERSMT_1206	5D4
C120	CERSMT_1206	5D4
C121	CERSMT_1206	3B5
C122	CERSMT_1206	3A8
C123	CERSMT_1206	3C4
C124	CERSMT_1206	5D3
C125	CERSMT_1206	5D3
C126	CERSMT_1206	5D3
C127	CERSMT_1206	3D4
C128	CERSMT_1206	5C3
C129	CERSMT_1206	3B6
C130	CERSMT_1206	3D5
C131	CERSMT_1206	5C3
C132	CERSMT_1206	5C3
C133	CERSMT_1206	5C3
C134	CERSMT_1206	5C2
C135	CERSMT_1206	5C3
C136	CERSMT_1206	5C3
C137	CERSMT_1206	5C3
C138	CERSMT_1206	5C3
C139	CERSMT_1206	5C3
C140	CERSMT_1206	3B6
C141	CERSMT_1206	3B6
C142	CERSMT_1206	5D4
C143	CERSMT_1206	5D4
C144	CERSMT_1206	5D4
C145	CERSMT_1206	5C3
C146	CERSMT_1206	5C3
C147	CERSMT_1206	5C3
C148	CERSMT_1206	5C2
C149	CERSMT_1206	5C5
C150	CERSMT_1206	5C5
C151	CERSMT_1206	5C4
C152	CERSMT_1206	5C4
C153	CERSMT_1206	5C4
C154	CERSMT_1206	5C4
C155	CERSMT_1206	5D2
C156	CERSMT_1206	5D3
C157	CERSMT_1206	5D3
C158	CERSMT_1206	5D2
C159	CERSMT_1206	5D3
C160	CERSMT_1206	5D1
C161	CERSMT_1206	5D2
C162	CERSMT_1206	5C4
C163	CERSMT_1206	5C4
C164	CERSMT_1206	5C4
C165	CERSMT_1206	5D4
C166	CERSMT_1206	5C4
C167	CERSMT_1206	5D4
C168	CERSMT_1206	5D3
C169	CERSMT_1206	5D3
C170	CERSMT_1206	5D2
C171	CERSMT_1206	5D1
C172	CERSMT_1206	5D2
C173	CERSMT_1206	5D3
C174	CERSMT_1206	5D4
C175	CERSMT_1206	5C4
C176	CERSMT_1206	5C4
C177	CERSMT_1206	5C4
C178	CERSMT_1206	5C4
C179	CERSMT_1206	5C4
C180	CERSMT_1206	5C4
C181	CERSMT_1206	5D2
C182	CERSMT_1206	5D3
C183	CERSMT_1206	5D1
CR1	1N4001	1C2
CR2	1N5231	2B2
CR3	1N5231	5B6
CR4	1N5231	5B6
CR5	1N5231	5B5
CR6	1N5231	5B5
CR7	1N5231	2A2
CR8	1N5231	2A2
CR9	1N5231	2B2
CR10	1N5231	2B2
CR11	1N914	3B7
CR12	1N914	3A6
CR13	1N914	1C2
CR14	1N914	3A5
CR15	1N914	3A7
CR16	1N5231	1D8
DS1	LED_10BAR_YEL	3C1
DS2	LED_10BAR_YEL	3B1
E1	JMPST_2X10_90012602	3B2
E2	JMPST_1X3_90012601	3D3
E3	JMPST_1X2_90012601	1D7
E4	JMPST_1X3_90012601	1C2
FL1	EMI_FLTR_43600000	1C8
FL2	EMI_FLTR_43600000	5A7
FL3	EMI_FLTR_43600000	4D6
FL4	EMI_FLTR_43600000	3D6
FL5	EMI_FLTR_43600000	1C4
K1	RLYDPDT_12DC_72919716	1D2
P1	CONN_EDG_AB31	1A7 1A8 1B7 1B8 1C1 1C1 1C7 1D7
P2	CONN_EDG_CD18	1A8 1B8 1C1
P3	HDMLXMFLKRA_2X5_51411328	1B1 1C1 1D1
P4	HDMLXMFLKRA_2X6_51411329	1A1 1A1 1B1 1D1 1D1 1D1
P5	HDRIBRA_2X17_51190176	1B8 1B8 1C8 1C8 2B8 3A8 3B8 3B8 3C8 3C8 3C8 3D8
P6	HDMLXMFLKRA_2X11_51411334	2B1 2B8 2C1 2C1 2D1 3A8
P7	HDMLXMFLKRA_2X3_51411326	2C1 2D1
P10	HDMLXMFLKRA_2X2_51411325	1A1 1B1
P11	HDRIBRA_2X13_51190174	1B8 1C8 2A1 2A1 2B1 2B8 2B8 2B8 2C8 2C8 5A2 5A2 5B5 5B6 5B7
P12	HDMLXMFLKRA_2X12_51411335	2A8 2B8 5A1 5B1
P14	HDRIBRA_2X5_51408751	4A7 4B7
Q1	2N3906	1B2
Q2	2N3906	1C8
Q3	LM336_5V	1C8
Q4	2N3904	1D8
R1	RESSMT_1206	1D2
R2	RESSMT_1206	1D2
R3	RESSMT_1206	1D2
R4	RESSMT_1206	3D3
R5	RES11SIP10X	2D7
R6	RESSMT_1206	2B1
R7	RES11SIP10X	2B8
R8	RESSMT_1206	1C2
R9	RESSMT_1206	1C1
R10	RESSMT_1206	3C1
R11	RESSMT_1206	3C1
R12	RESSMT_1206	3B1
R13	RESSMT_1206	3B1
R14	RESSMT_1206	3B1
R15	RESSMT_1206	3B1
R16	RESSMT_1206	3B1
R17	RESSMT_1206	3B1
R18	RESSMT_1206	3A1
R19	RESSMT_1206	3A1
R20	RESSMT_1206	2B1
R21	RESSMT_1206	3B5
R22	RESSMT_1206	3D7
R23	RESSMT_1206	3D7
R24	RESSMT_1206	3D7
R25	RESSMT_1206	3D7
R26	RESSMT_1206	3D7
R27	RES11SIP10X	3D7
R28	RESSMT_1206	3D7
R29	RESSMT_1206	3D7
R30	RESSMT_1206	3B7
R31	RESSMT_1206	3D7
R32	RESSMT_1206	3D7
R33	RESSMT_1206	3D7
R34	RESSMT_1206	3C7
R35	RESSMT_1206	3C8
R36	RESSMT_1206	3B7
R37	RESSMT_1206	3C8
R38	RESSMT_1206	3C8
R39	RESSMT_1206	5B7
R40	RESSMT_1206	2C2
R41	RESSMT_1206	2C2
R42	RESSMT_1206	2D8
R43	RESSMT_1206	2D8
R44	RESSMT_1206	2D8
R45	RESSMT_1206	2D8
R46	RESSMT_1206	2D8
R47	RESSMT_1206	2D8
R48	RESSMT_1206	2D8
R49	RESSMT_1206	2D8
R50	RESSMT_1206	2A7
R51	RESSMT_1206	2B2
R52	RESSMT_1206	2B2
R53	RESSMT_1206	2A7
R54	RESSMT_1206	3A6
R55	RESSMT_1206	3B8
R56	RESSMT_1206	3B7
R57	RESSMT_1206	3B7

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R58	RESSMT_1206	3B7
R59	RESSMT_1206	3B8
R60	RESSMT_1206	3A8
R61	RESSMT_1206	3B7
R62	RESSMT_1206	3B8
R63	RESSMT_1206	3B7
R64	RESSMT_1206	3B7
R65	RES11SIP10X	2D8
R66	RESSMT_1206	2A7
R67	RESSMT_1206	1B2
R68	RESSMT_1206	5A7
R69	RESSMT_1206	3D2
R70	RESSMT_1206	4D4
R71	RES10SIP9X	4D7
R72	RESSMT_1206	4B6
R73	RESSMT_1206	4D5
R74	RES10SIP9X	4D7
R75	RESSMT_1206	4D6
R76	RESSMT_1206	4D5
R77	RESSMT_1206	1B2
R78	RESSMT_1206	1B2
R79	RESSMT_1206	5A7
R80	RESSMT_1206	5A7
R81	RESSMT_1206	4D3
R82	RES10SIP9X	4A4
R83	RESSMT_1206	3B6
R84	RESSMT_1206	4C4
R85	RES10SIP9X	4A4
R86	RESSMT_1206	1C4
R87	RESSMT_1206	1C3
R88	RESSMT_1206	1C3
R89	RESSMT_1206	1D7
R90	RESSMT_1206	4C3
R91	RESSMT_1206	4C5
R92	RESSMT_1206	1D8
R93	RESSMT_1206	1C8
R94	RES11SIP10X	1D5
R95	RES11SIP10X	1D5
R96	RESSMT_1206	1D5
R97	RESSMT_1206	1B6
R102	RESSMT_1206	1D8
R103	RESSMT_1206	1D8
R104	RESSMT_1206	1D7
R105	RESSMT_1206	1D8
R107	RESSMT_1206	3C7
R108	RESSMT_1206	3C7
R109	RESSMT_1206	3C7
R110	RESSMT_1206	3C7
R111	RESSMT_1206	3A6
R112	RESSMT_1206	3A7
R113	RESSMT_1206	3A6
R114	RESSMT_1206	1B2
R115	RESSMT_1206	1B2
R116	RESSMT_1206	3A1
R117	RESSMT_1206	3B1
R118	RESSMT_1206	3B1
R119	RESSMT_1206	3B1
R120	RESSMT_1206	3B1
R121	RESSMT_1206	3B1
R122	RESSMT_1206	3B1
R123	RESSMT_1206	3B1
R124	RESSMT_1206	3C1
R125	RESSMT_1206	3C1
R126	RESSMT_1206	3A7
R127	RESSMT_1206	5A2
R128	RESSMT_1206	3A7
R129	RESSMT_1206	2D3
R130	RESSMT_1206	2C3
R131	RESSMT_1206	2C1
R132	RESSMT_1206	2D5
R133	RESSMT_1206	2D2
R134	RESSMT_1206	3A5
R135	RESSMT_1206	3A5

R136	RESSMT_1206	3B5
R137	RESSMT_1206	3A7
R138	RESSMT_1206	3B5
R139	RESSMT_1206	3B6
R140	RESSMT_1206	3B5
R141	RESSMT_1206	3D5
R142	RESSMT_1206	1C3
R143	RESSMT_1206	3B6
R144	RESSMT_1206	3B6
R145	RESSMT_1206	3B6
R146	RESMF1_4W	1B2
R147	RESMF1_4W	1A2
R148	RESMF1_4W	1A2
TP1	TEST_POINT_COLOR	2B3
TP2	TEST_POINT_COLOR	5B7
TP3	TEST_POINT_COLOR	1B8
TP4	TEST_POINT_COLOR	2A3
TP5	TEST_POINT_COLOR	2B3
TP6	TEST_POINT_COLOR	2B3
TP7	TEST_POINT_COLOR	1A8
TP8	TEST_POINT_COLOR	5B7
TP9	TEST_POINT_COLOR	2B3
TP10	TEST_POINT_COLOR	2A3
TP11	TEST_POINT_COLOR	1B8
TP12	TEST_POINT_COLOR	1B7
TP13	TEST_POINT_COLOR	5A6
TP14	TEST_POINT_COLOR	4D7
TP15	TEST_POINT_COLOR	4D5
TP16	TEST_POINT_COLOR	4D8
TP17	TEST_POINT_COLOR	4D8
TP18	TEST_POINT_COLOR	4D5
TP19	TEST_POINT_COLOR	4D6
TP20	TEST_POINT_COLOR	2D1
TP21	TEST_POINT_COLOR	1C3
TP22	TEST_POINT_COLOR	1B2
TP23	TEST_POINT_COLOR	1B7
TP24	TEST_POINT_COLOR	5B5
TP25	TEST_POINT_COLOR	4D5
TP26	TEST_POINT_COLOR	4D2
TP27	TEST_POINT_COLOR	1A7
TP28	TEST_POINT_COLOR	1B8
TP29	TEST_POINT_COLOR	3D5
TP30	TEST_POINT_COLOR	4C4
TP31	TEST_POINT_COLOR	4C4
TP32	TEST_POINT_COLOR	4C4
TP33	TEST_POINT_COLOR	1C3
TP34	TEST_POINT_COLOR	1B7
TP35	TEST_POINT_COLOR	1A8
TP36	TEST_POINT_COLOR	1C7
TP37	TEST_POINT_COLOR	1D7
U1	TIL311	3D1
U2	TIL311	3D1
U3	TIL117	1C2
U4	74ABT574	3D2
U5	MC3486	1B3
U6	MC3487	1B2
U7	ADM485	1D3
U8	7407	2A7
U9	7407	2B7
U10	74AC14	1C1 1D7 2A2 2B2
U11	TL082B	3A5 3A6
U12	TL082B	3B7
U13	ULN2803A	3C2
U14	74ABT574	3B3
U15	SW_DIP4_71996988	2D8
U16	MAX233A	5A3
U17	74LS08	2A7 2C6
U18	74LS244	2D2
U19	ULN2803A	2C7
U20	ADM485	5B7
U21	74ABT574	2C6
U22	74ABT574	3C3
U23	MAX233A	2C2

U24	MAX233A	2D2
U25	MAX233A	2D4
U26	MAX233A	2D4
U27	74LS244	2D6
U28	74ABT574	2C6
U29	74LS244	2A6
U30	74ABT574	2B6
U31	74ABT574	3D2
U32	74LS244	5A3
U33	MAX1232	4D4
U34	26C94	2D4
U35	74LS244	2D6
U36	COM20020	5B6
U37	COM20020	1C3
U38	74LS244	2B6
U39	74AC14	5C4
U40	74HCT245	4B4
U41	74LS14	1B1 1B2 1C2 1D6 2D2 2D4
U42	ADC10158	3D5
U44	ADC10158	3C5
U45	ADC10158	3B5
U46	MAX239	5B2
U47	SRAM_128KX8	5D5
U48	SRAM_128KX8	5D6
U49	74HCT245	4B4
U50	AM29F010	5D7
U51	AM29F010	5D7
U53	74HC244	4C3
U54	74HC244	4B3
U55	74HC244	4B3
U56	74LS245_VCC	1A6
U58	27C256_150_VCC	1C6
U59	74LS245_VCC	1B6
Y1	OSC_8P_EN_VCC_10TTL	4D6
Y2	OSC_8P_EN_VCC_10TTL	5A7
Y3	OSC_14P_EN_VCC_10TTL	3D5
Y4	OSC_8P_EN_VCC_10TTL	1C4

OEC MEDICAL SYSTEMS, INC.

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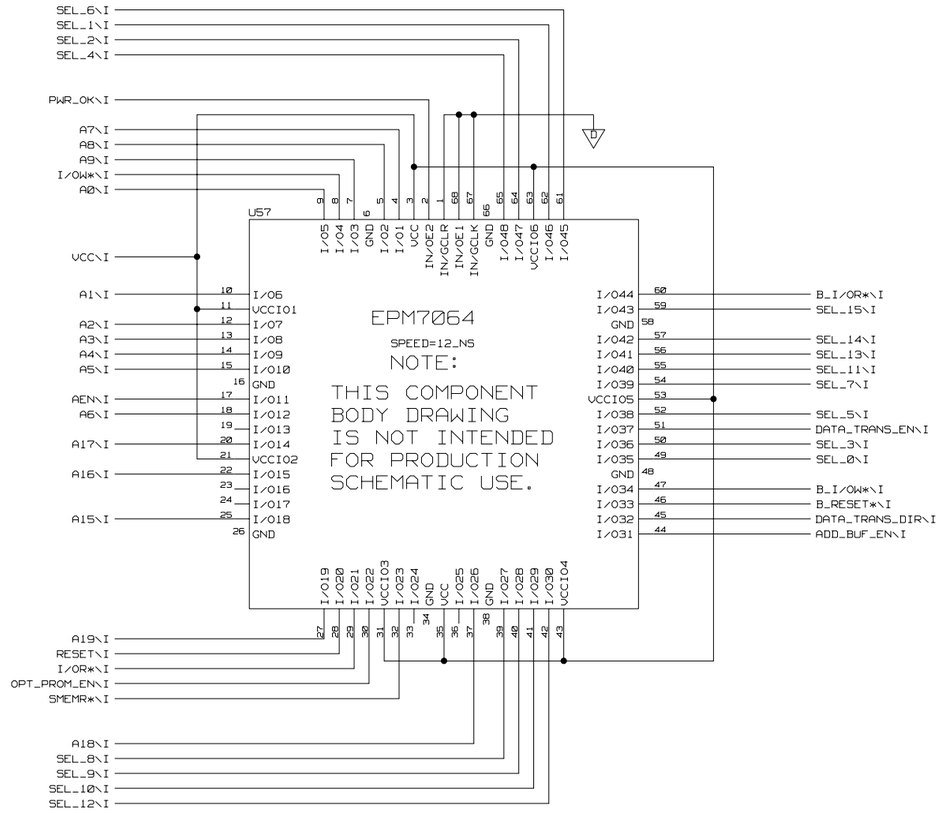

OEC MEDICAL SYSTEMS, INC.

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D	00-879054	B1
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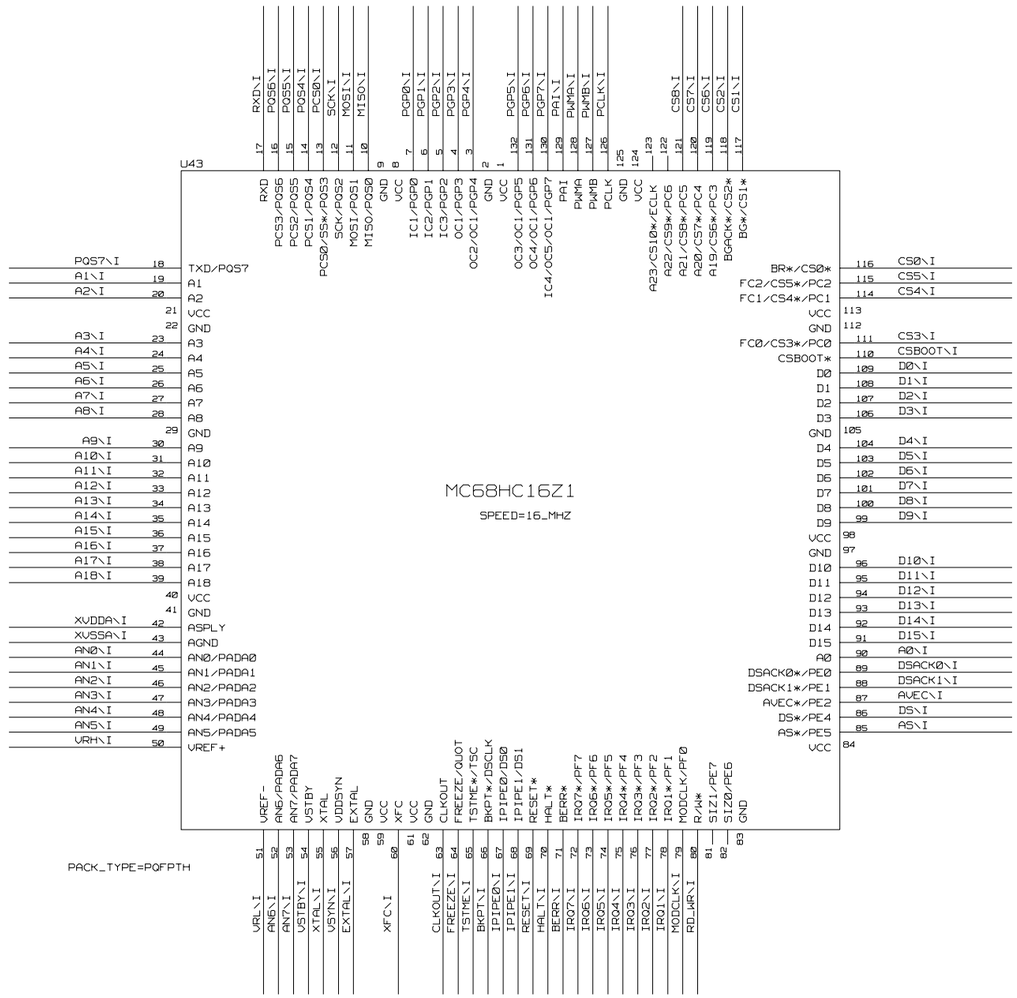

OEC MEDICAL SYSTEMS, INC.	
SIZE D	DWG NO. 00-879054 REV B1
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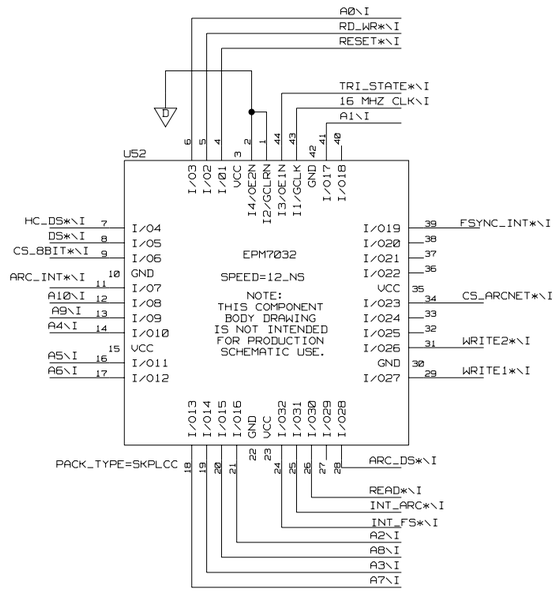

OEC MEDICAL SYSTEMS, INC.			
SIZE D	DWG NO. 00-879054		REV B1
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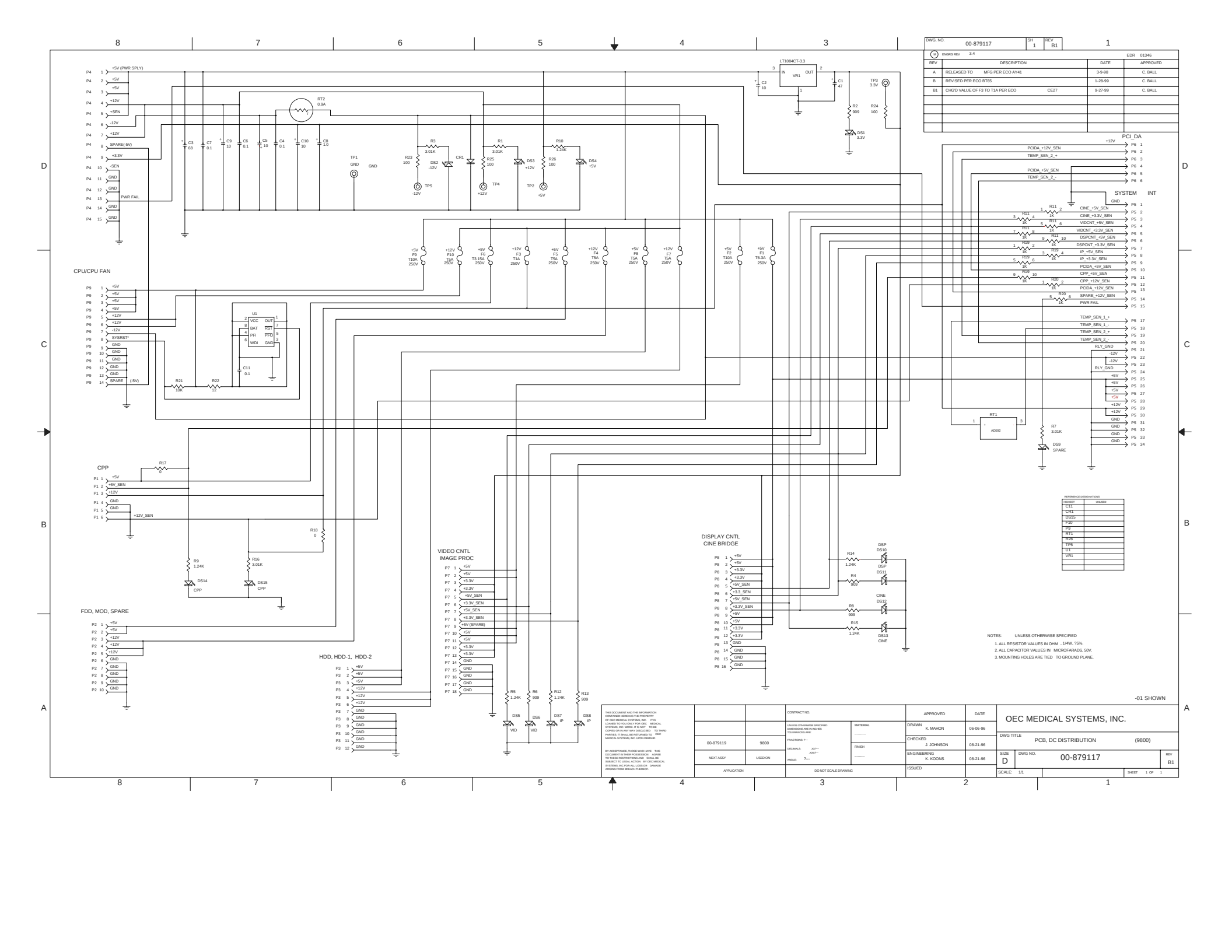
DWG. NO. 00-879117
SH 1
REV B1
ENGRG REV 3.4
EDR 01346
REV DESCRIPTION DATE APPROVED
A RELEASED TO MFG PER ECO AY41 3-9-98 C. BALL
B REVISED PER ECO BT65 1-28-99 C. BALL
B1 CHG'D VALUE OF F3 TO T1A PER ECO CE27 9-27-99 C. BALL
OEC MEDICAL SYSTEMS, INC.
PCB, DC DISTRIBUTION (9800)
DWG NO. 00-879117
REV B1
SIZE D
SCALE: 1/1
SHEET 1 OF 1
-01 SHOWN
CPU/CPU FAN
CPP
FDD, MOD, SPARE
VIDEO CNTL IMAGE PROC
HDD, HDD-1, HDD-2
DISPLAY CNTL CINE BRIDGE
PCI_DA
SYSTEM INT
NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTOR VALUES IN OHM , 1/4W, 75%.
2. ALL CAPACITOR VALUES IN MICROFARADS, 50V.
3. MOUNTING HOLES ARE TIED TO GROUND PLANE.

REVISIONS (M) ENGIN. REV 4			EDR 01346
REV	DESCRIPTION	DATE	APPROVED
A	RELEASED TO MFG PER ECO AV10	02-04-98	C. BALL
A1	REVISED PER ECO BL58	09-21-98	C. BALL
A2	REVISED PER ECO BN90	11-12-98	C. BALL
A3	REVISED PER ECO CE26	09-27-99	C. BALL

P2 - 3 ← ARCNET_SHLD_2
P2 - 6 ← FRAME_SYNC_SHLD_2
P2 - 9 ← FRAME_SYNC_SLV_SHLD
P2 - 10 ← SPARE
P2 - 11 ← SPARE
P2 - 12 ← SPARE
P2 - 8 ← FRAME_SYNC_HI_SLAVE
P2 - 7 ← FRAME_SYNC_LO_SLAVE
P2 - 4 ← FRAME_SYNC_HI_2
P2 - 5 ← FRAME_SYNC_LO_2
P2 - 1 ← ARCNET_HI_2
P2 - 2 ← ARCNET_LO_2
P1 - 22 ← CONFIG_0
P1 - 23 ← CONFIG_1
P1 - 24 ← CONFIG_2
P1 - 25 ← CONFIG_3
P1 - 19 ← DIAG_TXD
P1 - 20 ← DIAG_RXD
P1 - 21 ← DIAG_SHLD
P1 - 26 ← ISOLAT_RLY_CNTL

+5V
0.250A CB1
R2 1K
R3 1K
R4 1K
R5 1K
R6 10K
R7 10K
R8 10K
R9 10K

15 PIN DSUB
+5 (ARCNET_BIAS_PWR) → P4 - 13
FRAME_SYNC_HI_SLAVE → P4 - 15
FRAME_SYNC_LO_SLAVE → P4 - 14
FRAME_SYNC_HI_2 → P4 - 4
FRAME_SYNC_LO_2 → P4 - 5
ARCNET_HI_2 → P4 - 1
ARCNET_LO_2 → P4 - 2 [2]
CONFIG_0 → P4 - 9
CONFIG_1 → P4 - 10
CONFIG_2 → P4 - 11
CONFIG_3 → P4 - 12
DIAG_TXD → P4 - 6
DIAG_RXD → P4 - 7
→ P4 - 8

00-879184-01 SCH, PCB, EXTERNAL INTERFACE
00-879185-01 PCB, EXTERNAL INTERFACE, A/F, 9800
00-879186-60 SPEC, PERF, EXTERNAL INTERFACE 9800

RJ45 JACK — RJ45 JACK
P6 - 1 ↔ P5 - 1
P6 - 2 ↔ P5 - 2
P6 - 3 ↔ P5 - 3
P6 - 4 ↔ P5 - 4 [2]
P6 - 5 ↔ P5 - 5
P6 - 6 ↔ P5 - 6
P6 - 7 ↔ P5 - 7
P6 - 8 ↔ P5 - 8

P1 - 15
P1 - 16
P1 - 17
P1 - 18
+5V
C4 68
C1 0.1
TP1 RED
TP3 BLK
+12V
C3 68
C2 0.1
TP2 RED
TP4 BLK

P1 - 1 ← RELAY_GND
P1 - 2 ← RELAY_+12V
K1
R1 100
12VDC
[1]

P1 - 3 ← PWR_INJCT
K2

P1 - 6 ← XRAY_ON
K3

K4

15 PIN DSUB, HD
PWR_INJECT_1 → P3 - 1
PWR_INJECT_2 → P3 - 6
XRAY_ON_1 → P3 - 2 [2]
XRAY_ON_2 → P3 - 7
RM_IN_USE_1 → P3 - 3
RM_IN_USE_2 → P3 - 8

P1 - 7 ← RM_IN_USE
P1 - 9 ← DR_INT_SW
P1 - 10 ← DR_INT_SW_RTN
P1 - 11 ← CNTL_1
P1 - 12 ← CNTL_1_RTN
P1 - 13 ← CNTL_2
P1 - 14 ← CNTL_2_RTN

R13 1K
R14 1K
R15 1K
R10 10K
R11 10K
R12 10K

DR_INT_SW → P3 - 4
DR_INT_SW_RTN → P3 - 5
CNTL_1 → P3 - 9 [2]
CNTL_1_RTN → P3 - 10
CNTL_2 → P3 - 14
CNTL_2_RTN → P3 - 15

P1 - 4 ← SPARE DRIVER
P1 - 5 ← SPARE DRIVER
P1 - 8 ← SPARE DRIVER

NOTES:
1. DIODE ON SYSTEM INTERFACE PCB
2. EMI FILTERED CONNECTOR

DRAWING
LAST_MODIFIED=Mon Sep 27 13:19:25 1999

-01 SHOWN

REFERENCE DESIGNATIONS

HIGHEST	UNUSED
C4	
CB1	
K4	
P6	
R15	
TP4	

ITEM	QTY.	PART OR IDENT NO.	DESCRIPTION

PART LIST

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		CONTRACT NO.	
		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS: +/- DECIMALS: .XX+/- .XXX+/- ANGLES: +/-	MATERIAL / FINISH
00-879186	9800		
NEXT ASSY	USED ON		
APPLICATION		DO NOT SCALE DRAWING	

APPROVALS	DATE
DRAWN D. DARLEY	8-13-97
CHECKED K. KOONS	8-22-96
ENGINEERING B. WALKER	8-22-96
APPROVED	

OEC MEDICAL SYSTEMS, INC.

DWG TITLE: EXTERNAL INTERFACE PCB

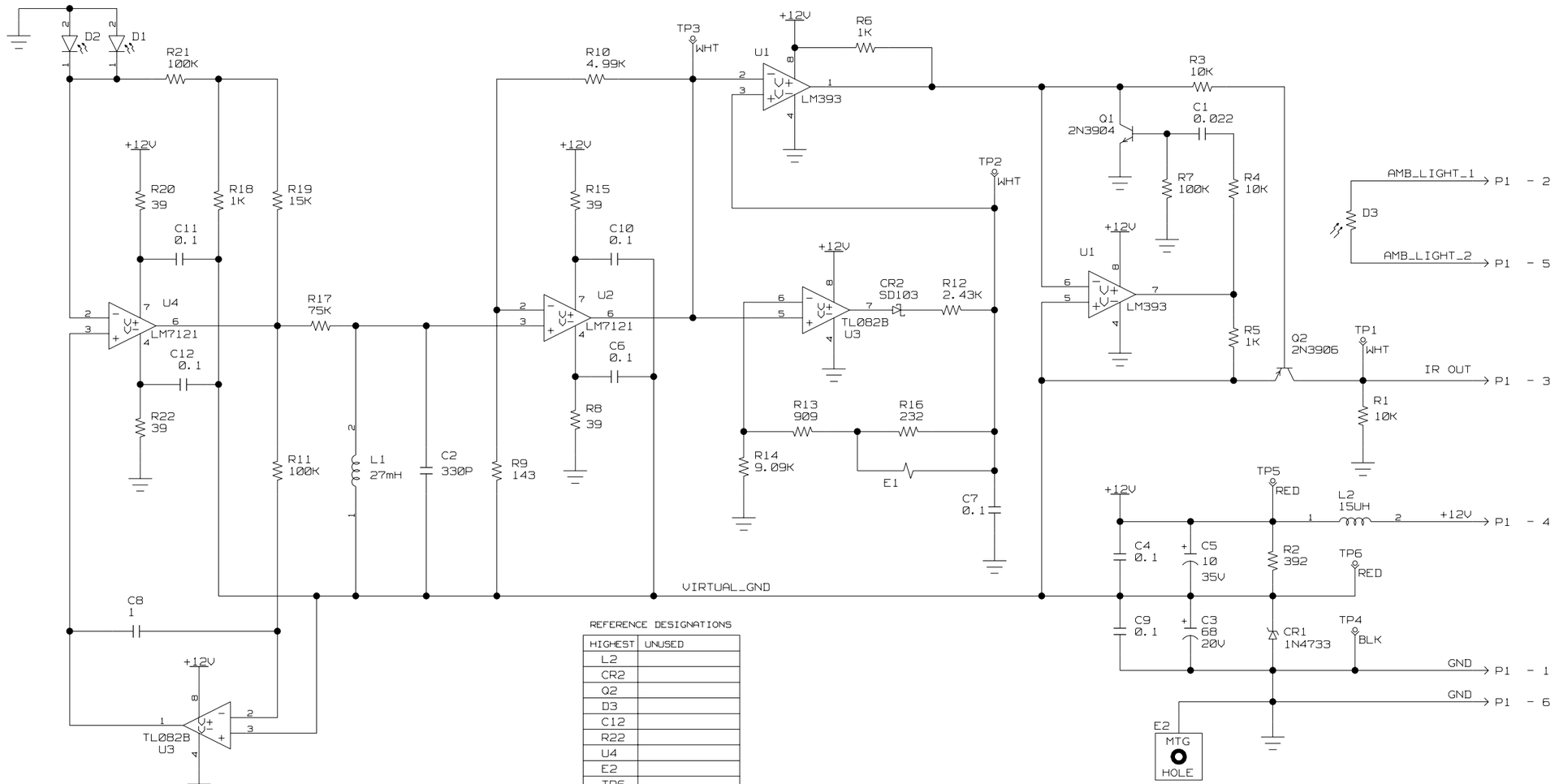
SIZE C | DWG NO. 00-879184 | REV A3

SCALE N/A | SHEET 1 OF 1

00-879184 (C)

05-014-9/93

REV	DESCRIPTION	DATE	APPROVED
	(M) ENGIN. REV 1 REVISIONS		EDR 01346
A	RELEASE TO MANUFACTURING PER ECO AV77		



REFERENCE DESIGNATIONS

HIGHEST	UNUSED
L2	
CR2	
Q2	
D3	
C12	
R22	
U4	
E2	
TP6	
P1	

NOTES: 1. E1 IS A CIRCUIT TRACE AND IS NOT A STUFFED COMPONENT
2. UNLESS OTHERWISE NOTED, ALL RESISTORS ARE 1/4 WATT 1% METAL FILM

-01 SHOWN

ITEM	QTY.	PART OR IDENT NO.	DESCRIPTION

PART LIST

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	9600, 9800
NEXT ASSY	USED ON
APPLICATION	

CONTRACT NO.

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FRACTIONS: +/-
DECIMALS: .XX+/-
.XXX+/-
ANGLES: +/-

MATERIAL

FINISH

DO NOT SCALE DRAWING

APPROVALS	DATE
DRAWN M. HEUER	8/27/96
CHECKED KEN KOONS	9/24/96
ENGINEERING B. WALKER	9/24/96
APPROVED	

OEC MEDICAL SYSTEMS, INC.

DWG TITLE: SCH, PCB, IR RECEIVER, 9800

SIZE C | DWG NO. 00-879378 | REV A

SCALE NONE | SHEET 1 OF 1

00-879378

05-014-9/93

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	RELEASED TO MANUFACTURING PER ECO AW70	2/25/98	C. BALL
A1	REVISED PER ECO BJ38		

ENGIN. REV 5.1 EDR 01346

IMPEDANCE TEST STRIP 1

P7 - 1 → P8 - 1
P7 - 2 → P8 - 2
P7 - 3 → P8 - 3

IMPEDANCE TEST STRIP 2

P9 - 1 → P10 - 1
P9 - 2 → P10 - 2
P9 - 3 → P10 - 3 (VCC)

NOTE:
SEE 00-879499-01 FOR DRIVES 1 AND 2

LOOP IN

P1 - 1 IN_3_HI
P1 - 2 IN_3_LO
P1 - 3

DRIVE 3 (SHT 2)

OUT_3_HI IN_4_HI
OUT_3_LO IN_4_LO
BYPASS_3*
FAIL_3*

DRIVE 4 (SHT 2)

OUT_4_HI IN_5_HI
OUT_4_LO IN_5_LO
BYPASS_4*
FAIL_4*

DRIVE 5 (SHT 3)

OUT_5_HI IN_6_HI
OUT_5_LO IN_6_LO
BYPASS_5*
FAIL_5*

DRIVE 6 (SHT 3)

BYPASS_6*
FAIL_6*

LOOP OUT

OUT_6_HI → P2 - 1
OUT_6_LO → P2 - 2
P2 - 3

BYPASS_<6..3>*
FAIL_<6..3>*

P3 - 6
P3 - 5
P3 - 13
P3 - 14
P3 - 15
P3 - 16
P3 - 7
P3 - 8

TP5 YEL
TP7 TP6 TP4 TP2 TP1
BLK BLK BLK BLK BLK
C34 0.01 50V
+12V
C35 100 20V

P3 - 1
P3 - 2
P3 - 3
P3 - 4
P3 - 12
P3 - 11
P3 - 10
P3 - 9

TP3 RED
VCC
C24 0.01 50V
C26 100 20V

U4
74HC244
1 EN 2
19 EN 1

3 BYPASS_3*	8	A3 2	Y3	12 BYPASS_D3* 3
4 BYPASS_4*	6	A2	Y2	14 BYPASS_D4* 4
5 BYPASS_5*	4	A1	Y1	16 BYPASS_D5* 5
6 BYPASS_6*	2	A0	Y0	18 BYPASS_D6* 6
3 FAIL_3*	11	A3 1	Y3	9 FAIL_D3* 3
4 FAIL_4*	13	A2	Y2	7 FAIL_D4* 4
5 FAIL_5*	15	A1	Y1	5 FAIL_D5* 5
6 FAIL_6*	17	A0	Y0	3 FAIL_D6* 6

BYPASS_D<6..3>*
FAIL_D<6..3>*

VCC
C37 0.1 50V

STATUS

P4 - 1 SPARE
P4 - 2 BYPASS_D1*
P4 - 3 BYPASS_D2*
P4 - 4 3 BYPASS_D3*
P4 - 5 4 BYPASS_D4*
P4 - 6 5 BYPASS_D5*
P4 - 7 6 BYPASS_D6*
P4 - 8 SPARE
P4 - 9 FAIL_D1*
P4 - 10 FAIL_D2*
P4 - 11 3 FAIL_D3*
P4 - 12 4 FAIL_D4*
P4 - 13 5 FAIL_D5*
P4 - 14 6 FAIL_D6*
P4 - 15 SPARE
P4 - 16 4DISK*
P4 - 17
P4 - 18
P4 - 19
P4 - 20

REFERENCE DESIGNATIONS

HIGHEST	UNUSED
BT1	
C53	
J6	J1, J2
P10	P6
R85	
U5	
TP7	

+12V VCC
R21 1K 1% 0.1W
R22 1K 1% 0.1W

P5 - 1 SPARE
P5 - 4 SPARE
P5 - 2 PCIDA_+12_SEN
P5 - 5 PCIDA_+5_SEN
P5 - 3 TEMP_SEN_2+
P5 - 6 TEMP_SEN_2-

BT1 AD592CN TEMPERATURE SENSOR

NOTE:
UNLESS OTHERWISE SPECIFIED, ALL CAPACITORS ARE IN MICROFARADS, RATED AT 50 V AND ALL RESISTORS ARE 0.100 W 1%

REF DESIGNATIONS	DEVICE	GND		+5V	UNUSED
U1, U2, U3, U5	MC10SX1189	13		3, 5, 8, 16	4
U4	74HC244	10		20	

DRAWING
LAST_MODIFIED=Fri Jul 31 13:53:14 1998

-01 SHOWN

ITEM	QTY.	PART OR IDENT NO.	DESCRIPTION

PART LIST

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00-879410	9800
NEXT ASSY	USED ON
APPLICATION	

CONTRACT NO.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS: +/-
DECIMALS: .XX+/-
.XXX+/-
ANGLES: +/-

MATERIAL
FINISH

DO NOT SCALE DRAWING

APPROVALS	DATE
DRAWN J. PERRY	8/20/96
CHECKED B. SPRATT	8/20/96
ENGINEERING J. PERRY	8/20/96
APPROVED	

OEC MEDICAL SYSTEMS, INC.

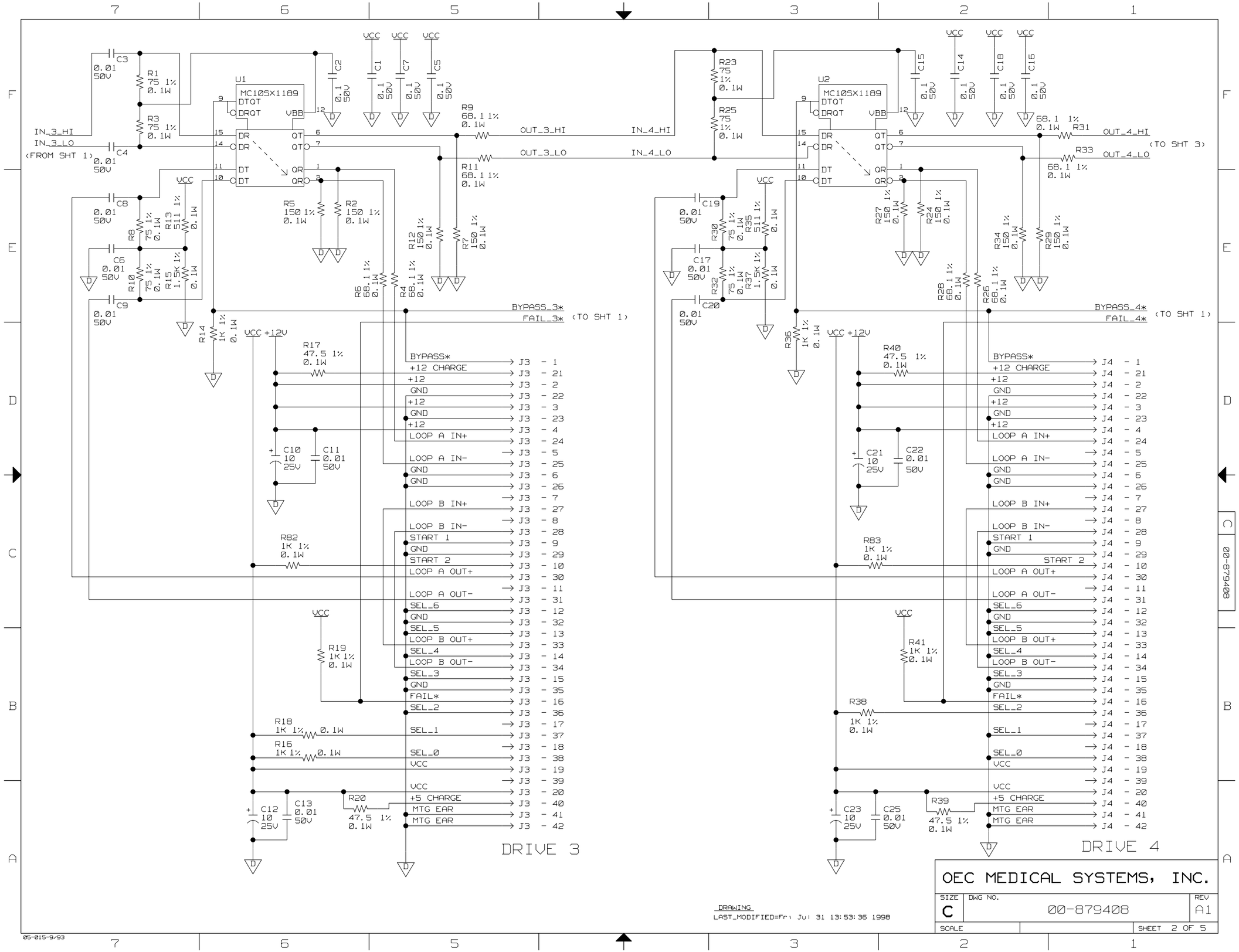
DWG TITLE: SCH, PCB, CINE 4-DISK BACKPLANE

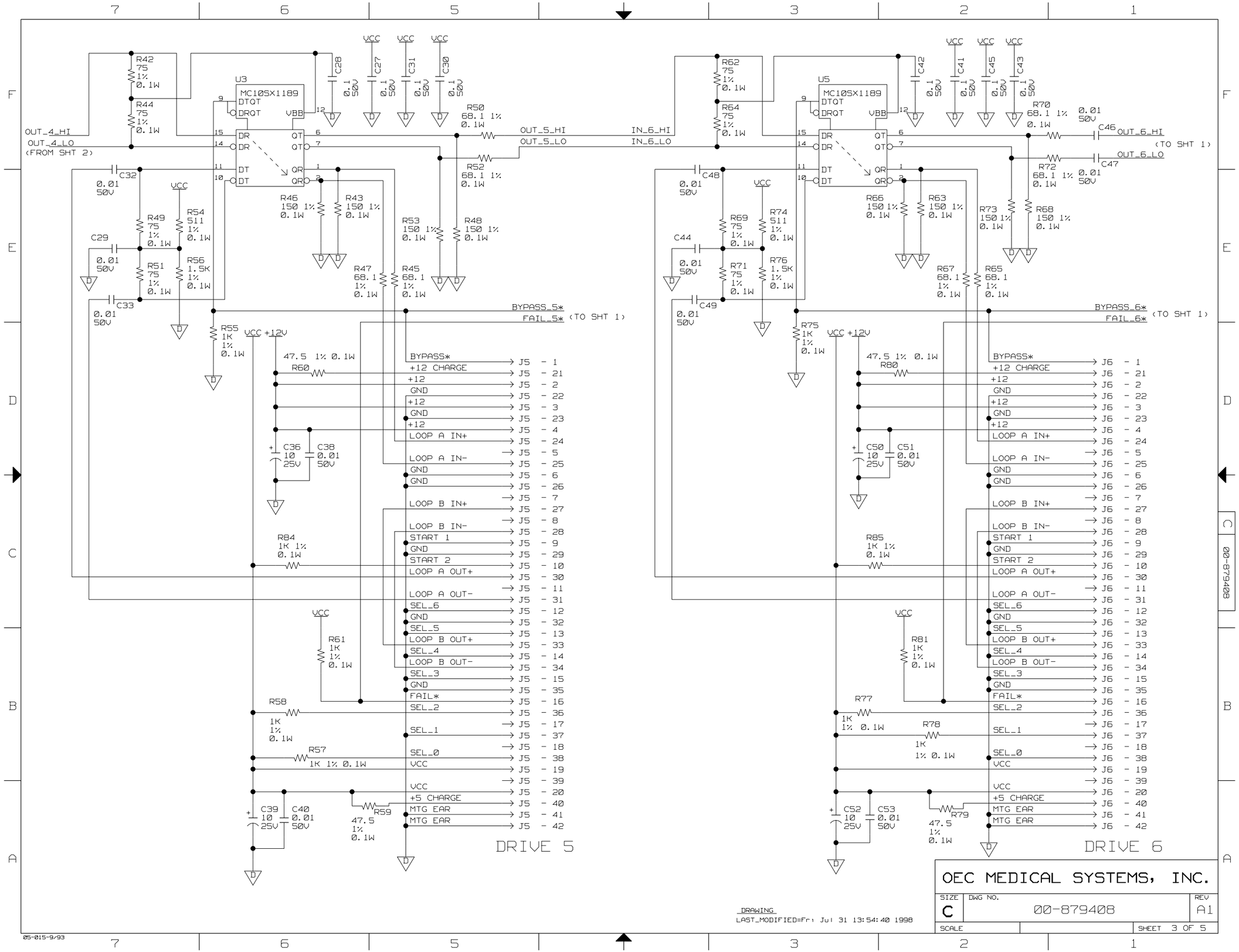
SIZE C | DWG NO. 00-879408 | REV A1

SCALE NONE | SHEET 1 OF 5

00-879408

05-014-9/93


U1
MC10SX1189
DTQT
DRQT
VBB
DR
DR
DT
DT
QT
QT
QR
QR
U2
MC10SX1189
IN_3_HI
IN_3_LO
(FROM SHT 1)
OUT_3_HI
OUT_3_LO
IN_4_HI
IN_4_LO
OUT_4_HI
OUT_4_LO
(TO SHT 3)
BYPASS_3*
FAIL_3*
BYPASS_4*
FAIL_4*
(TO SHT 1)
VCC
VCC +12V
BYPASS*
+12 CHARGE
+12
GND
LOOP A IN+
LOOP A IN-
LOOP B IN+
LOOP B IN-
START 1
START 2
LOOP A OUT+
LOOP A OUT-
SEL_6
SEL_5
SEL_4
SEL_3
SEL_2
SEL_1
SEL_0
FAIL*
+5 CHARGE
MTG EAR
J3 - 1
J3 - 21
J3 - 2
J3 - 22
J3 - 3
J3 - 23
J3 - 4
J3 - 24
J3 - 5
J3 - 25
J3 - 6
J3 - 26
J3 - 7
J3 - 27
J3 - 8
J3 - 28
J3 - 9
J3 - 29
J3 - 10
J3 - 30
J3 - 11
J3 - 31
J3 - 12
J3 - 32
J3 - 13
J3 - 33
J3 - 14
J3 - 34
J3 - 15
J3 - 35
J3 - 16
J3 - 36
J3 - 17
J3 - 37
J3 - 18
J3 - 38
J3 - 19
J3 - 39
J3 - 20
J3 - 40
J3 - 41
J3 - 42
J4 - 1
J4 - 21
J4 - 2
J4 - 22
J4 - 3
J4 - 23
J4 - 4
J4 - 24
J4 - 5
J4 - 25
J4 - 6
J4 - 26
J4 - 7
J4 - 27
J4 - 8
J4 - 28
J4 - 9
J4 - 29
J4 - 10
J4 - 30
J4 - 11
J4 - 31
J4 - 12
J4 - 32
J4 - 13
J4 - 33
J4 - 14
J4 - 34
J4 - 15
J4 - 35
J4 - 16
J4 - 36
J4 - 17
J4 - 37
J4 - 18
J4 - 38
J4 - 19
J4 - 39
J4 - 20
J4 - 40
J4 - 41
J4 - 42
DRIVE 3
DRIVE 4
OEC MEDICAL SYSTEMS, INC.
SIZE C
DWG NO. 00-879408
REV A1
SCALE
SHEET 2 OF 5
DRAWING
LAST_MODIFIED=Fri Jul 31 13:53:36 1998
00-879408
05-015-9/93


U3
MC10SX1189
DTQT
DRQT
VBB
DR
DT
QT
QR
R42 75 1% 0.1W
R44 75 1% 0.1W
R50 68.1 1% 0.1W
R52 68.1 1% 0.1W
R46 150 1% 0.1W
R43 150 1% 0.1W
R53 150 1% 0.1W
R48 150 1% 0.1W
R47 68.1 1% 0.1W
R45 68.1 1% 0.1W
R49 75 1% 0.1W
R54 511 1% 0.1W
R51 75 1% 0.1W
R56 1.5K 1% 0.1W
R55 1K 1% 0.1W
R60 47.5 1% 0.1W
R84 1K 1% 0.1W
R61 1K 1% 0.1W
R58 1K 1% 0.1W
R57 1K 1% 0.1W
R59 47.5 1% 0.1W
C28 0.1 50V
C27 0.1 50V
C31 0.1 50V
C30 0.1 50V
C32 0.01 50V
C29 0.01 50V
C33 0.01 50V
C36 10 25V
C38 0.01 50V
C39 10 25V
C40 0.01 50V
VCC
+12V
OUT_4_HI
OUT_4_LO
(FROM SHT 2)
OUT_5_HI
OUT_5_LO
BYPASS_5*
FAIL_5*
(TO SHT 1)
BYPASS*
+12 CHARGE
+12
GND
LOOP A IN+
LOOP A IN-
LOOP B IN+
LOOP B IN-
START 1
START 2
LOOP A OUT+
LOOP A OUT-
SEL_6
SEL_5
LOOP B OUT+
SEL_4
LOOP B OUT-
SEL_3
FAIL*
SEL_2
SEL_1
SEL_0
+5 CHARGE
MTG EAR
J5 - 1
J5 - 21
J5 - 2
J5 - 22
J5 - 3
J5 - 23
J5 - 4
J5 - 24
J5 - 5
J5 - 25
J5 - 6
J5 - 26
J5 - 7
J5 - 27
J5 - 8
J5 - 28
J5 - 9
J5 - 29
J5 - 10
J5 - 30
J5 - 11
J5 - 31
J5 - 12
J5 - 32
J5 - 13
J5 - 33
J5 - 14
J5 - 34
J5 - 15
J5 - 35
J5 - 16
J5 - 36
J5 - 17
J5 - 37
J5 - 18
J5 - 38
J5 - 19
J5 - 39
J5 - 20
J5 - 40
J5 - 41
J5 - 42
DRIVE 5
U5
MC10SX1189
DTQT
DRQT
VBB
DR
DT
QT
QR
R62 75 1% 0.1W
R64 75 1% 0.1W
R70 68.1 1% 0.1W
R72 68.1 1% 0.1W
R66 150 1% 0.1W
R63 150 1% 0.1W
R73 150 1% 0.1W
R68 150 1% 0.1W
R67 68.1 1% 0.1W
R65 68.1 1% 0.1W
R69 75 1% 0.1W
R74 511 1% 0.1W
R71 75 1% 0.1W
R76 1.5K 1% 0.1W
R75 1K 1% 0.1W
R80 47.5 1% 0.1W
R85 1K 1% 0.1W
R81 1K 1% 0.1W
R77 1K 1% 0.1W
R78 1K 1% 0.1W
R79 47.5 1% 0.1W
C42 0.1 50V
C41 0.1 50V
C45 0.1 50V
C43 0.1 50V
C46 0.01 50V
C47 0.01 50V
C48 0.01 50V
C44 0.01 50V
C49 0.01 50V
C50 10 25V
C51 0.01 50V
C52 10 25V
C53 0.01 50V
VCC
+12V
OUT_6_HI
OUT_6_LO
(TO SHT 1)
BYPASS_6*
FAIL_6*
BYPASS*
+12 CHARGE
+12
GND
LOOP A IN+
LOOP A IN-
LOOP B IN+
LOOP B IN-
START 1
START 2
LOOP A OUT+
LOOP A OUT-
SEL_6
SEL_5
LOOP B OUT+
SEL_4
LOOP B OUT-
SEL_3
FAIL*
SEL_2
SEL_1
SEL_0
+5 CHARGE
MTG EAR
J6 - 1
J6 - 21
J6 - 2
J6 - 22
J6 - 3
J6 - 23
J6 - 4
J6 - 24
J6 - 5
J6 - 25
J6 - 6
J6 - 26
J6 - 7
J6 - 27
J6 - 8
J6 - 28
J6 - 9
J6 - 29
J6 - 10
J6 - 30
J6 - 11
J6 - 31
J6 - 12
J6 - 32
J6 - 13
J6 - 33
J6 - 14
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DRIVE 6
DRAWING
LAST_MODIFIED=Fri Jul 31 13:54:40 1998
OEC MEDICAL SYSTEMS, INC.
SIZE C
DWG NO. 00-879408
REV A1
SCALE
SHEET 3 OF 5
00-879408
05-015-9/93

*** Signal Cross-Reference ***
--- for the entire design --

BYPASS_ <6..3> *	1D3
BYPASS_3 *	1D5 2D4 1D4
BYPASS_4 *	1D5 2D1 1D3
BYPASS_5 *	1D5 3D4 1D3
BYPASS_6 *	1D5 3D1 1D2
BYPASS_D <6..3> *	1D3
BYPASS_D3 *	1D1 1D4
BYPASS_D4 *	1D1 1D4
BYPASS_D5 *	1D1 1D4
BYPASS_D6 *	1C1 1D4
FAIL_ <6..3> *	1D3
FAIL_3 *	1D5 2D4 1D4
FAIL_4 *	1D5 2D1 1D3
FAIL_5 *	1D5 3D4 1D3
FAIL_6 *	1C5 3D1 1D2
FAIL_D <6..3> *	1D3
FAIL_D3 *	1C1 1D4
FAIL_D4 *	1C1 1D4
FAIL_D5 *	1C1 1D4
FAIL_D6 *	1C1 1C4
IN_3_HI	1D5 2D7
IN_3_LO	1D5 2D7
OUT_4_HI	2D1 3D7
OUT_4_LO	2D1 3D7
OUT_6_HI	1D2 3D1
OUT_6_LO	1D2 3D1
PCIDA_+5_SEN	1B7
PCIDA_+12_SEN	1B7
TEMP_SEN_2+	1B7
TEMP_SEN_2-	1B7

00-879408

OEC MEDICAL SYSTEMS, INC.

SIZE	DWG NO.	REV
C	00-879408	A1
SCALE		SHEET 4 OF 5

05-015-9/93

*** Unit Cross-Reference ***
--- for the entire design --

BT1	AD592	1B6
C1	CERSMT_1206	2D5
C2	CERSMT_1206	2D6
C3	CERSMT_0603	2D7
C4	CERSMT_0603	2D7
C5	CERSMT_1206	2D5
C6	CERSMT_0805	2D7
C7	CERSMT_1206	2D5
C8	CERSMT_0603	2D7
C9	CERSMT_0603	2D7
C10	TASMT_7343	2D6
C11	CERSMT_0805	2D6
C12	TASMT_7343	2A6
C13	CERSMT_0805	2A6
C14	CERSMT_1206	2D2
C15	CERSMT_1206	2D2
C16	CERSMT_1206	2D2
C17	CERSMT_0805	2D3
C18	CERSMT_1206	2D2
C19	CERSMT_0603	2D4
C20	CERSMT_0603	2D4
C21	TASMT_7343	2D3
C22	CERSMT_0805	2D2
C23	TASMT_7343	2A3
C24	CERSMT_0805	1D7
C25	CERSMT_0805	2A2
C26	TAR_100U_41547909	1D6
C27	CERSMT_1206	3D5
C28	CERSMT_1206	3D6
C29	CERSMT_0805	3D7
C30	CERSMT_1206	3D5
C31	CERSMT_1206	3D5
C32	CERSMT_0603	3D7
C33	CERSMT_0603	3D7
C34	CERSMT_0805	1D6
C35	TAR_100U_41547909	1D6
C36	TASMT_7343	3D6
C37	CERSMT_1206	1C5
C38	CERSMT_0805	3D6
C39	TASMT_7343	3A6
C40	CERSMT_0805	3A6
C41	CERSMT_1206	3D2
C42	CERSMT_1206	3D2
C43	CERSMT_1206	3D2
C44	CERSMT_0805	3D4
C45	CERSMT_1206	3D2
C46	CERSMT_0603	3D1
C47	CERSMT_0603	3D1
C48	CERSMT_0603	3D4
C49	CERSMT_0603	3D4
C50	TASMT_7343	3D3
C51	CERSMT_0805	3D2
C52	TASMT_7343	3A3
C53	CERSMT_0805	3A3
J3	D50_40SCSIR_51180011	2A5 2A5 2A5 2B5 2B5 2C5 2C5 2D5 2D5 2D5
J4	D50_40SCSIR_51180011	2A1 2A1 2B1 2B1 2B1 2B1 2C1 2C1 2C1 2D1 2D1
J5	D50_40SCSIR_51180011	3A5 3A5 3B5 3B5 3C5 3C5 3D5 3D5
J6	D50_40SCSIR_51180011	3A1 3A1 3B1 3B1 3B1 3B1 3C1 3C1 3C1 3D1 3D1
P1	HDAMPST_1X3_51411076	1D7
P2	HDAMPST_1X3_51411076	1D1
P3	MINJRST_2X8_51411131	1D7
P4	HDRIBSTW_2X10_51106232	1C1 1D1
P5	HDMLXMFLKST_2X3_51411337	1B7
P7	HDMLXST_1X3_51411080	1D7
P8	HDMLXST_1X3_51411080	1D6
P9	HDMLXST_1X3_51411080	1D6
P10	HDMLXST_1X3_51411080	1D5
R1	RESSMT_0805	2D7
R2	RESSMT_0805	2D6
R3	RESSMT_0805	2D7
R4	RESSMT_0805	2D5
R5	RESSMT_0805	2D6
R6	RESSMT_0805	2D6
R7	RESSMT_0805	2D5
R8	RESSMT_0805	2D7
R9	RESSMT_0805	2D5
R10	RESSMT_0805	2D7
R11	RESSMT_0805	2D5
R12	RESSMT_0805	2D5
R13	RESSMT_0805	2D7
R14	RESSMT_0805	2D6
R15	RESSMT_0805	2D7
R16	RESSMT_0805	2B6
R17	RESSMT_0805	2D6
R18	RESSMT_0805	2B6
R19	RESSMT_0805	2B6
R20	RESSMT_0805	2A6
R21	RESSMT_0805	1B6
R22	RESSMT_0805	1B5
R23	RESSMT_0805	2D3
R24	RESSMT_0805	2D2
R25	RESSMT_0805	2D3
R26	RESSMT_0805	2D2
R27	RESSMT_0805	2D2
R28	RESSMT_0805	2D2
R29	RESSMT_0805	2D1
R30	RESSMT_0805	2D3
R31	RESSMT_0805	2D1
R32	RESSMT_0805	2D3
R33	RESSMT_0805	2D1
R34	RESSMT_0805	2D2
R35	RESSMT_0805	2D3
R36	RESSMT_0805	2D3
R37	RESSMT_0805	2D3
R38	RESSMT_0805	2B3
R39	RESSMT_0805	2A2
R40	RESSMT_0805	2D2
R41	RESSMT_0805	2B2
R42	RESSMT_0805	3D7
R43	RESSMT_0805	3D6
R44	RESSMT_0805	3D7
R45	RESSMT_0805	3D5
R46	RESSMT_0805	3D6
R47	RESSMT_0805	3D6
R48	RESSMT_0805	3D5
R49	RESSMT_0805	3D7
R50	RESSMT_0805	3D5
R51	RESSMT_0805	3D7
R52	RESSMT_0805	3D5
R53	RESSMT_0805	3D5
R54	RESSMT_0805	3D7
R55	RESSMT_0805	3D6
R56	RESSMT_0805	3D7
R57	RESSMT_0805	3B6
R58	RESSMT_0805	3B6
R59	RESSMT_0805	3A5
R60	RESSMT_0805	3D6
R61	RESSMT_0805	3B6
R62	RESSMT_0805	3D3
R63	RESSMT_0805	3D2
R64	RESSMT_0805	3D3
R65	RESSMT_0805	3D2
R66	RESSMT_0805	3D3
R67	RESSMT_0805	3D2
R68	RESSMT_0805	3D2
R69	RESSMT_0805	3D3
R70	RESSMT_0805	3D1
R71	RESSMT_0805	3D3
R72	RESSMT_0805	3D1
R73	RESSMT_0805	3D2
R74	RESSMT_0805	3D3
R75	RESSMT_0805	3D3
R76	RESSMT_0805	3D3
R77	RESSMT_0805	3B3
R78	RESSMT_0805	3B2
R79	RESSMT_0805	3A2
R80	RESSMT_0805	3D2
R81	RESSMT_0805	3B2
R82	RESSMT_0805	2C6
R83	RESSMT_0805	2C3
R84	RESSMT_0805	3C6
R85	RESSMT_0805	3C3
TP1	TEST_POINT_COLOR	1D6
TP2	TEST_POINT_COLOR	1D6
TP3	TEST_POINT_COLOR	1D7
TP4	TEST_POINT_COLOR	1D6
TP5	TEST_POINT_COLOR	1D6
TP6	TEST_POINT_COLOR	1D7
TP7	TEST_POINT_COLOR	1D7
U1	MC10SX1189	2D6
U2	MC10SX1189	2D3
U3	MC10SX1189	3D6
U4	74HC244	1D5
U5	MC10SX1189	3D3

C
00-879408
B
A

OEC MEDICAL SYSTEMS, INC.

SIZE	DWG NO.	REV
C	00-879408	A1
SCALE		SHEET 5 OF 5

05-015-9/93

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	RELEASED TO MANUFACTURING PER ECO AW23		

ENGIN. REV 3 EDR 01346

IMPEDANCE TEST STRIP 1

P7 - 1 → P8 - 1
P7 - 2 → P8 - 2
P7 - 3 → P8 - 3

IMPEDANCE TEST STRIP 2

P9 - 1 → P10 - 1
P9 - 2 → P10 - 2
P9 - 3 → P10 - 3
VCC

LOOP IN

P1 - 1 IN_1_HI
P1 - 2 IN_1_LO
P1 - 3

DRIVE 1

SHT 2

OUT_1_HI → IN_2_HI
OUT_1_LO → IN_2_LO
BYPASS_1*
FAIL_1*

DRIVE 2

SHT 2

OUT_2_HI
OUT_2_LO
BYPASS_2*
FAIL_2*

LOOP OUT

OUT_2_HI → P2 - 1
OUT_2_LO → P2 - 2
P2 - 3

BYPASS_<2..1>*
FAIL_<2..1>*

TP2 YEL
3 - P3
4 - P3
TP5 TP4 TP3
C9 0.01 50V
C10 100 20V
+12V
7 - P3
8 - P3
BLK BLK BLK

TP1 RED
VCC
1 - P3
2 - P3
C8 0.01 50V
C7 100 20V
5 - P3
6 - P3

U3
74HC244
EN 2
EN 1
1 BYPASS_1* → A3 2 Y3 → 12 BYPASS_D1* 1
2 BYPASS_2* → A2 Y2 → 14 BYPASS_D2* 2
A1 Y1 → 16
A0 Y0 → 18
1 FAIL_1* → A3 1 Y3 → 9 FAIL_D1* 1
2 FAIL_2* → A2 Y2 → 7 FAIL_D2* 2
A1 Y1 → 5
A0 Y0 → 3

VCC
C20 0.1 50V

BYPASS_D<2..1>*
FAIL_D<2..1>*

STATUS

P4 - 1
P4 - 2
SPARE P4 - 3
1 BYPASS_D1* P4 - 4
2 BYPASS_D2* P4 - 5
BYPASS_D3* P4 - 6
BYPASS_D4* P4 - 7
BYPASS_D5* P4 - 8
BYPASS_D6* P4 - 9
SPARE P4 - 10
1 FAIL_D1* P4 - 11
2 FAIL_D2* P4 - 12
FAIL_D3* P4 - 13
FAIL_D4* P4 - 14
FAIL_D5* P4 - 15
FAIL_D6* P4 - 16
2DISK* P4 - 17
P4 - 18
P4 - 19
P4 - 20

REFERENCE DESIGNATIONS

HIGHEST	UNUSED
U3	
C31	
J2	
P10	P5,6
R41	
TP5	

REF DESIGNATIONS	DEVICE	GND		+5V	UNUSED
U1,U2	MC10SX1189	13		3,5,8,	4
				16	
U3	74HC244	10		20	

NOTE:
UNLESS OTHERWISE SPECIFIED, ALL CAPACITORS ARE IN MICROFARADS, RATED AT 50 V AND ALL RESISTORS ARE 0.100 W 1%

DRAWING

LAST_MODIFIED=Mon Feb 16 12:36:59 1998

-01 SHOWN

ITEM	QTY.	PART OR IDENT NO.	DESCRIPTION

PART LIST

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		CONTRACT NO.	
		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS: +/- DECIMALS: .XX+/- .XXX+/- ANGLES: +/-	MATERIAL / FINISH
00-879410	9800		
NEXT ASSY	USED ON		
APPLICATION		DO NOT SCALE DRAWING	

APPROVALS	DATE
DRAWN J. C. JOHNSON	12-5-96
CHECKED	
ENGINEERING	
APPROVED	

OEC MEDICAL SYSTEMS, INC.

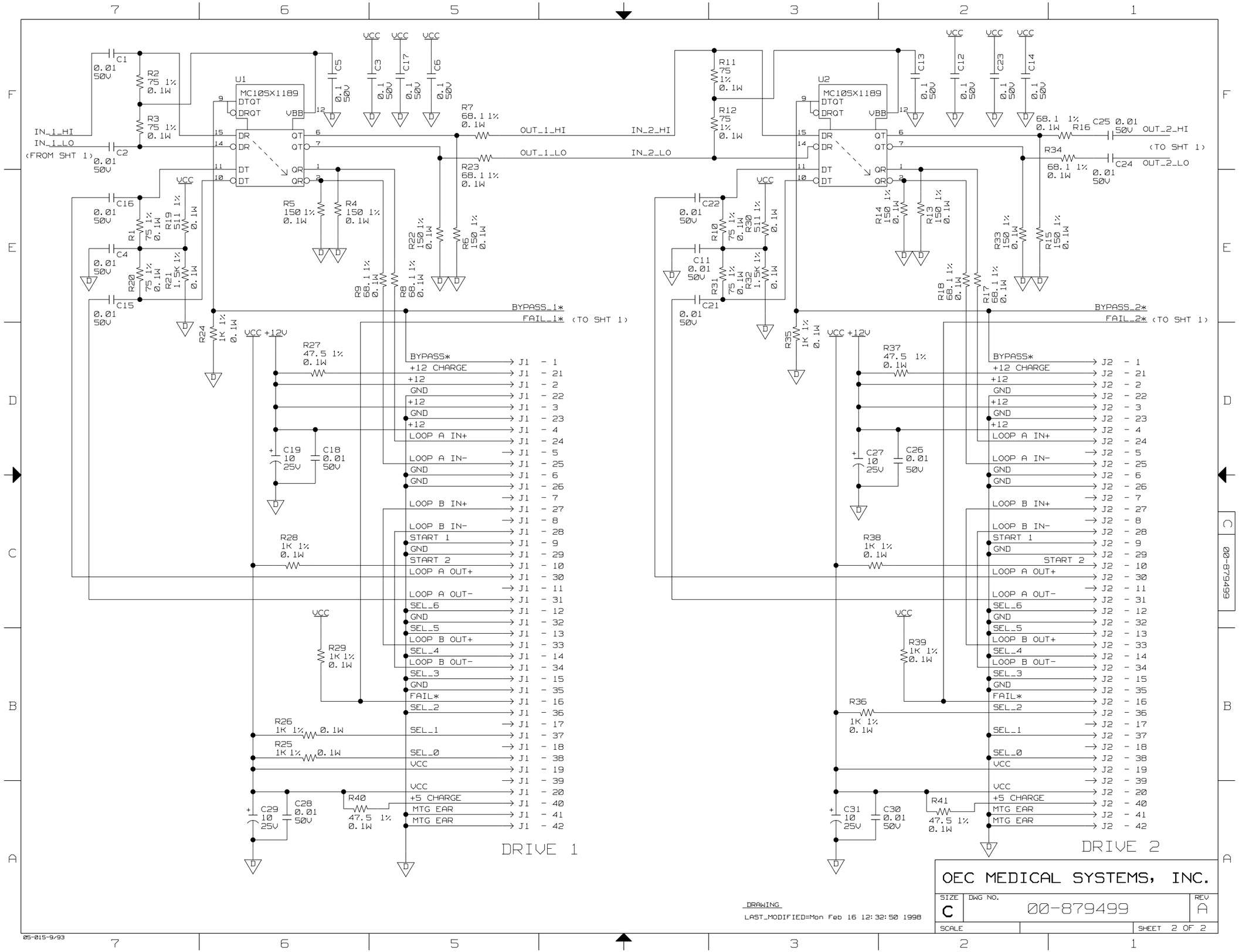
DWG TITLE: SCH, PCB, CINE 2-DISK BACKPLANE

SIZE C | DWG NO. 00-879499 | REV A

SCALE NONE | SHEET 1 OF 2

00-879499

05-014-9/93


IN_1_HI
IN_1_LO
(FROM SHT 1)
C1 0.01 50V
C2 0.01 50V
R2 75 1% 0.1W
R3 75 1% 0.1W
U1
MC10SX1189
DTQT
DRQT
VBB
DR
DR
DT
DT
QT
QT
QR
QR
C5 0.1 50V
C3 0.1 50V
C17 0.1 50V
C6 0.1 50V
VCC
R7 68.1 1% 0.1W
R23 68.1 1% 0.1W
OUT_1_HI
OUT_1_LO
IN_2_HI
IN_2_LO
R11 75 1% 0.1W
R12 75 1% 0.1W
U2
C13 0.1 50V
C12 0.1 50V
C23 0.1 50V
C14 0.1 50V
R16 68.1 1% 0.1W
C25 0.01 50V OUT_2_HI
(TO SHT 1)
R34 68.1 1% 0.1W
C24 0.01 50V OUT_2_LO
C16 0.01 50V
C4 0.01 50V
C15 0.01 50V
R1 75 1% 0.1W
R19 511 1% 0.1W
R20 75 1% 0.1W
R21 1.5K 1% 0.1W
R5 150 1% 0.1W
R4 150 1% 0.1W
R22 150 1% 0.1W
R6 150 1% 0.1W
R9 68.1 1% 0.1W
R8 68.1 1% 0.1W
C22 0.01 50V
C11 0.01 50V
C21 0.01 50V
R10 75 1% 0.1W
R30 511 1% 0.1W
R31 75 1% 0.1W
R32 1.5K 1% 0.1W
R14 150 1% 0.1W
R13 150 1% 0.1W
R33 150 1% 0.1W
R15 150 1% 0.1W
R18 68.1 1% 0.1W
R17 68.1 1% 0.1W
BYPASS_1*
FAIL_1* (TO SHT 1)
BYPASS_2*
FAIL_2* (TO SHT 1)
R24 1K 1% 0.1W
R35 1K 1% 0.1W
VCC +12V
R27 47.5 1% 0.1W
R37 47.5 1% 0.1W
C19 10 25V
C18 0.01 50V
C27 10 25V
C26 0.01 50V
R28 1K 1% 0.1W
R38 1K 1% 0.1W
R29 1K 1% 0.1W
R39 1K 1% 0.1W
R26 1K 1% 0.1W
R25 1K 1% 0.1W
R36 1K 1% 0.1W
R40 47.5 1% 0.1W
R41 47.5 1% 0.1W
C29 10 25V
C28 0.01 50V
C31 10 25V
C30 0.01 50V
BYPASS* J1 - 1
+12 CHARGE J1 - 21
+12 J1 - 2
GND J1 - 22
+12 J1 - 3
GND J1 - 23
+12 J1 - 4
LOOP A IN+ J1 - 24
J1 - 5
LOOP A IN- J1 - 25
GND J1 - 6
GND J1 - 26
J1 - 7
LOOP B IN+ J1 - 27
J1 - 8
LOOP B IN- J1 - 28
START 1 J1 - 9
GND J1 - 29
START 2 J1 - 10
LOOP A OUT+ J1 - 30
J1 - 11
LOOP A OUT- J1 - 31
SEL_6 J1 - 12
GND J1 - 32
SEL_5 J1 - 13
LOOP B OUT+ J1 - 33
SEL_4 J1 - 14
LOOP B OUT- J1 - 34
SEL_3 J1 - 15
GND J1 - 35
FAIL* J1 - 16
SEL_2 J1 - 36
J1 - 17
SEL_1 J1 - 37
J1 - 18
SEL_0 J1 - 38
VCC J1 - 19
J1 - 39
VCC J1 - 20
+5 CHARGE J1 - 40
MTG EAR J1 - 41
MTG EAR J1 - 42
BYPASS* J2 - 1
+12 CHARGE J2 - 21
+12 J2 - 2
GND J2 - 22
+12 J2 - 3
GND J2 - 23
+12 J2 - 4
LOOP A IN+ J2 - 24
J2 - 5
LOOP A IN- J2 - 25
GND J2 - 6
GND J2 - 26
J2 - 7
LOOP B IN+ J2 - 27
J2 - 8
LOOP B IN- J2 - 28
START 1 J2 - 9
GND J2 - 29
START 2 J2 - 10
LOOP A OUT+ J2 - 30
J2 - 11
LOOP A OUT- J2 - 31
SEL_6 J2 - 12
GND J2 - 32
SEL_5 J2 - 13
LOOP B OUT+ J2 - 33
SEL_4 J2 - 14
LOOP B OUT- J2 - 34
SEL_3 J2 - 15
GND J2 - 35
FAIL* J2 - 16
SEL_2 J2 - 36
J2 - 17
SEL_1 J2 - 37
J2 - 18
SEL_0 J2 - 38
VCC J2 - 19
J2 - 39
VCC J2 - 20
+5 CHARGE J2 - 40
MTG EAR J2 - 41
MTG EAR J2 - 42
DRIVE 1
DRIVE 2
00-879499
DRAWING
LAST_MODIFIED=Mon Feb 16 12:32:50 1998
OEC MEDICAL SYSTEMS, INC.
SIZE C
DWG NO. 00-879499
REV A
SCALE
SHEET 2 OF 2
05-015-9/93

REVISIONS (M) ENGIN. REV 4			EDR 01346
REV	DESCRIPTION	DATE	APPROVED
A	RELEASED TO MFG PER ECO AY77	3-18-98	C. BALL
A1	REVISED PER ECO BW23	4-27-99	C. BALL
A2	REVISED PER ECO BW99A	7-1-99	C. BALL
B	REVISED PER ECO CF79	12-2-99	C. BALL

XU1 TO-220 HEAT SINK

14VAC CR1 R31 499 U1 LM2940 IN TAB OUT GND +12V TP5 RED +12V TP6 BLK AGND VR1 AD587 +10.000V OUT TRIM NR IN GND TP4 RED +10V 10Vref 2 E7 C8 1 50V

F2 0.75A 125V T1 115V P1 S1 S2 CB2 1.1A 0.2A CB1 AC125 CR6 1N4747 20V RM04G C1 3300 25V C4 0.1 50V C2 1000 16V R5 4.99K

9V @ 1A R1 1K R4 3.01K RV1 175V RV2 175V

K2 12VDC CR2 1N4001
P6 - 1 MODEM AC 9VAC @ 800MA
P6 - 2 MODEM AC RTN

MC1413 U2 R2 6.04K R3 6.04K C5 0.1 50V C3 1000 16V E7 XE7 VSS

P1 - 4 AC1_T1 5A
P1 - 2 NEUT_FLOAT
P1 - 6 AC2_T1
P1 - 1 AC_T1
P1 - 5 GND_PS
P1 - 3 RTN_T1

LOOP2 P2 - 1
KEY_PWR P2 - 2
LOOP1 P2 - 3
CNCT_ON P2 - 4
INT_GOOD_LO P2 - 5
INT_GOOD_HI P2 - 6

K3 K4 TP2 TP1 TP3 CR4 1N4001 15A

115VAC_PH P5 - 1
P5 - 2
CHASSIS P5 - 3
115VAC_RTN P5 - 4

SEE NOTE 1 R7 3.01K

P3 - 1 12V_KEY
P3 - 2 KEY_PWR
P3 - 3
P3 - 4 GND_PS

K1 12VDC CR3 1N4001

5A AC1_CART P4 - 1
15A NEUT_FLOAT P4 - 2
P4 - 3
5A AC2_CART P4 - 4

K5 12VDC CR5 1N4001 R43 2K R42 2K *Relay_ON 2 F7

R40 49.9K 1N4733 CR12 Q7 MMBT3904 Q8 MMBT3904 LS1 ALARM C11 10 16V R41 499K

NEUT_FLOAT 2 E7
AC2_T1 2 E7
KEY_PWR 2 F7

MTG HOLE E8
MTG HOLE E2
MTG HOLE E3
MTG HOLE E4
MTG HOLE E5
MTG HOLE E6

REFERENCE DESIGNATIONS

HIGHEST	UNUSED
C12	
CB2	
CR12	
DS3	
E8	
F2	
K5	
LS1	
P6	
Q8	Q8
R43	R6, 38, 39
RV2	
T2	
TP12	
U3	
VR1	
XF1	
XU1	

REF DES	DEVICE	DGND	+5V	AGND	-12V	+12V	UNUSED
U1	LM2940-12V			SHOWN		SHOWN	
U2	MC1413			SHOWN		SHOWN	
U3	LM324			SHOWN		SHOWN	
VR1	AD587			SHOWN			1, 3, 5, 7

-02 SHOWN
-01 INACTIVE

ITEM	QTY.	PART OR IDENT NO.	DESCRIPTION

PART LIST

NOTES
1. JUMPER E7 TO BE INSTALLED BETWEEN PINS 1-2 FOR 9800 OR BETWEEN PINS 2 AND 3 FOR UROVIEW 2800 ONLY.

DRAWING
LAST_MODIFIED=Thu Dec 2 13:37:12 1999
ACTIVE_BOMS=-22

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00-880317	9800	CONTRACT NO.	
NEXT ASSY	USED ON	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS: +/- DECIMALS: .XX+/- .XXX+/- ANGLES: +/-	MATERIAL / FINISH
APPLICATION		DO NOT SCALE DRAWING	

APPROVALS	DATE
DRAWN D. DARLEY	8/6/97
CHECKED M. WILLCOCKS	6/13/97
ENGINEERING D. DARLEY	6/13/97
APPROVED	

OEC MEDICAL SYSTEMS, INC.

DWG TITLE: SCH, PCB, POWER CONTROL

SIZE C | DWG NO. 00-880315 | REV B

SCALE NONE | SHEET 1 OF 2

00-880315

05-014-9/93

1 B6 KEY_PWR
DC15P

1 B4 *Relay_ON

1 3F 10Vref

1 B6 NEUT_FLOAT
AC125

1 B6 AC2_T1
AC125X

F1

T2 SECONDARY PRIMARY

CR9 1N4005

CR8 1N4005

R14 39.2K 1%

R16 39.2K 1%

C6 22 200V

C12 1 50V

TP7 WHT

TP8 WHT

R18 4.99K

R19 3.57K

R8 0.5W 10% 10K
UPPER VSENSE ADJUST

R9 0.5W 10% 10K
LOWER VSENSE ADJUST

TP9 WHT

TP10 WHT

R10 3.92K 1%

R20 10K

U3 LM324

R23 39.2
+12V
DC15P

R37 332K

RED LINE HIGH DS3

AMBER LINE LOW DS2

C9 0.1 50V

R17 2.21K

R26 2.21K

1M R36

CR10 1N4001

CR11 1N4001

R25 5.36K

Q4 MMBT3904

C7 10 16V

R24 10K

R32 10K

+12V

DC15P

R15 5.36K

R13 2.21K

R12 4.75K

IN = TO DISABLE SENSE CKT

E1

DS1 GREEN (PWR OK)

CR7 SD103

Q2 MMBT3904

Q1 MMBT2222

R11 475

+12V DC15P R27 10K

+12V DC15P R28 5.49K

R29 10K 1% 0.125W

C10 47 20V

R30 30.1K

TP12 GRN

TP11 GRN

R35 10K

R22 10K

Time Delay 2

Q5 MMBT3904

R34 10K

R21 10K

Time Delay 1

Q3 MMBT2222

Q6 MMBT3904

R33 10K

00-880315-02 SCH, PCB, POWER CONTROL, 9800
00-880316-02 PCB, POWER CONTROL, AF, 9800
00-880317-60 SPEC, PERF, PWR CONT PCB, 9800
12-221104-05 SCR,MACH,PAN,PHL,4-40,5/16,SST
13-311104-00 NUT,HEX-LK-EXT-T,4-40,SST,NA,A-.250

14-111104-00 WSHR,PL,#4,SST,MS15795-804,ID/.120
88-298900-00 CMPD,HS,BTL,20Z,250

DRAWING
LAST_MODIFIED=Thu Dec 2 08:17:28 1999

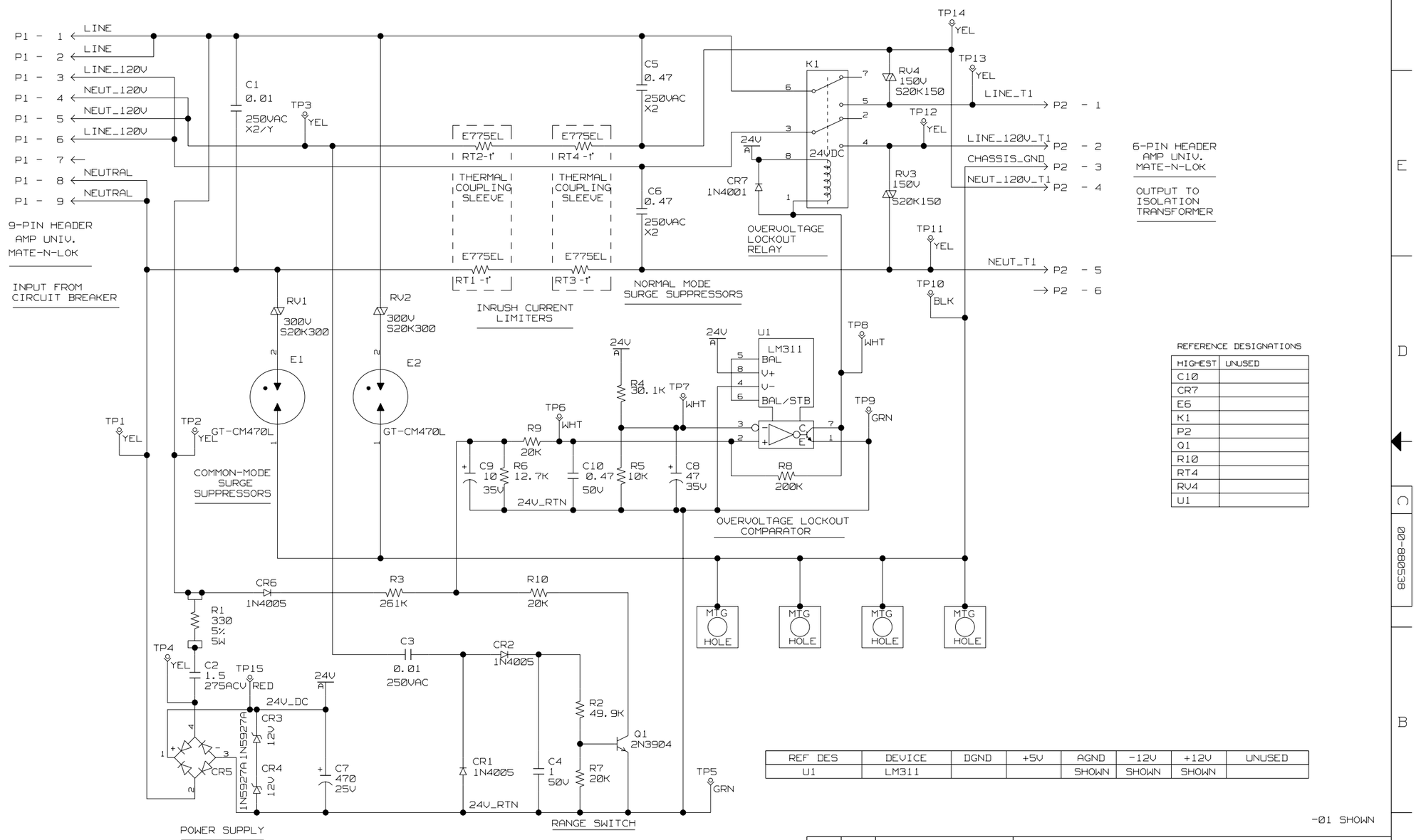
OEC MEDICAL SYSTEMS, INC.

SIZE	DWG NO.	REV
C	00-880315	B
SCALE NONE		SHEET 2 OF 2

00-880315

05-015-9/93

M	ENGIN. REV 4	REVISIONS	EDR 01346
REV	DESCRIPTION	DATE	APPROVED
A	RELEASED TO MFG PER ECO AY91		



REFERENCE DESIGNATIONS

HIGHEST	UNUSED
C10	
CR7	
E6	
K1	
P2	
Q1	
R10	
RT4	
RV4	
U1	

REF DES	DEVICE	DGND	+5V	AGND	-12V	+12V	UNUSED
U1	LM311			SHOWN	SHOWN	SHOWN	

-01 SHOWN

ITEM	QTY.	PART OR IDENT NO.	DESCRIPTION

PART LIST

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		CONTRACT NO.	APPROVALS	DATE
SCH_PKG	9800	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS: +/- DECIMALS: .XX+/- .XXX+/- ANGLES: +/- MATERIAL FINISH	DRAWN D. DARLEY	6/13/97
00-880540	9800		CHECKED B. WALKER	7/30/97
NEXT ASSY	USED ON		ENGINEERING D. DARLEY	7/30/97
APPLICATION		DO NOT SCALE DRAWING	APPROVED	

OEC MEDICAL SYSTEMS, INC.

DWG TITLE: SCH, PCB, SURGE SUPPRESSOR

SIZE C | DWG NO. 00-880538 | REV A

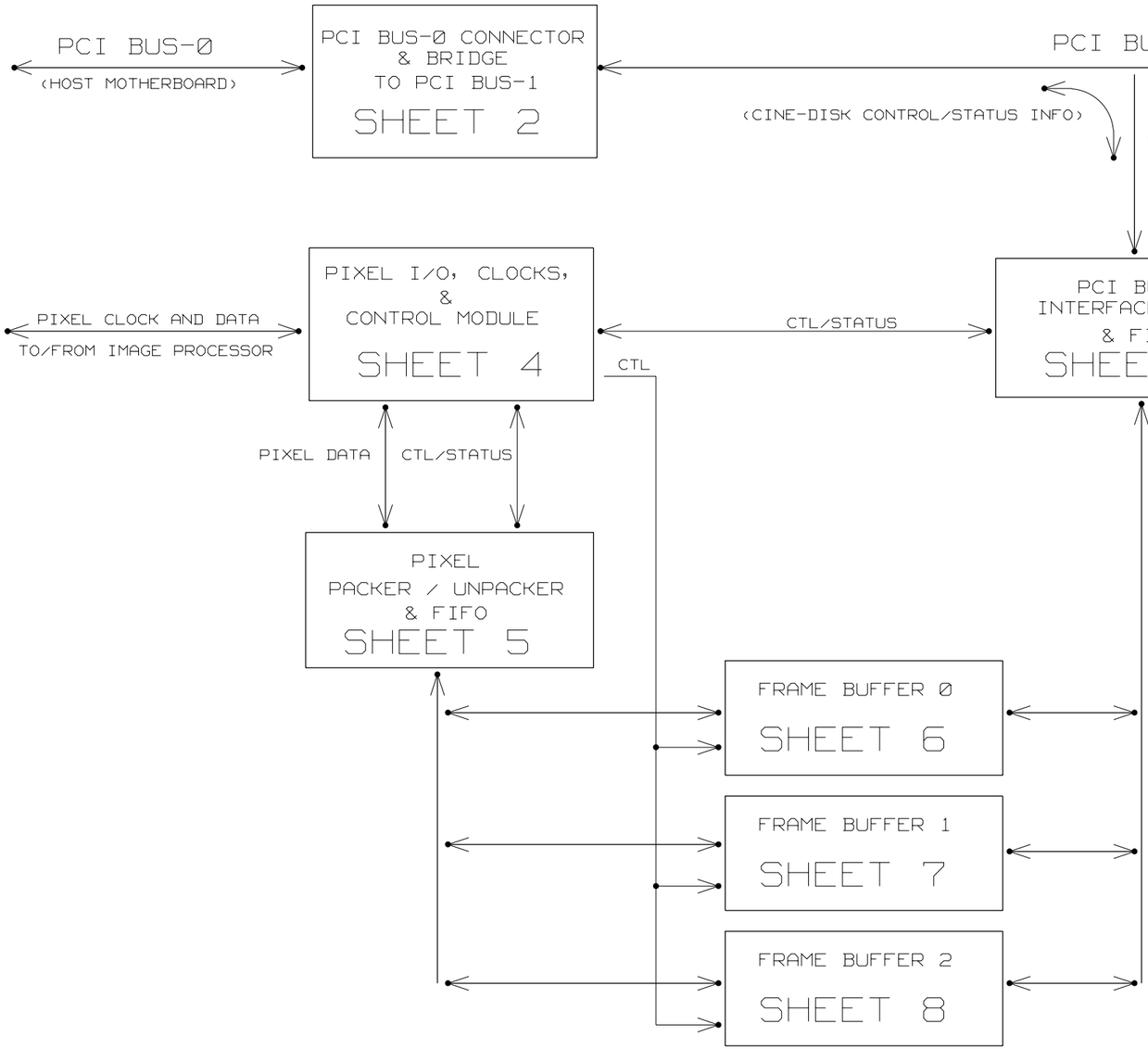
SCALE NONE | SHEET 1 OF 1

00-880538

05-014-9/93

DWG NO. 00-880921	SHT 1	REV A1

M	ENGIN. REV. 1.1 REVISIONS		EDR 01346
REV	DESCRIPTION	DATE	APPROVED
A	RELEASED TO MANUFACTURING PER ECO BN39	11-3-98	C. BALL
A1	REVISED PER ECO CE35	09-27-99	C. BALL



POWER DISTRIBUTION & FPGA PROGRAMMING SHEET 10	TACHLITE FC-AL AND SUPPORT SHEET 11
CTL_MODULE PINOUT SHEET 12	PIXPACK PINOUT SHEET 13
MEMCTL 0 PINOUT SHEET 14	MEMCTL 1 PINOUT SHEET 15
MEMCTL 2 PINOUT SHEET 16	PCI9050 PINOUT SHEET 17
PCI FIFO CTL PINOUT SHEET 18	BYPASS CAPACITORS SHEET 19
BYPASS CAPACITORS SHEET 20	SPARE COMPONENTS AND REFERENCE DESIGNATORS SHEET 21

NOTE:
COMPONENT J7 NOT USED WITH TACHLITE

SHEET LOCATIONS

-01 SHOWN

ITEM	QTY.	PART OR IDENT NO.	DESCRIPTION

PARTS LIST

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		CONTRACT NO.		APPROVED	DATE
		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE:	MATERIAL	DRAWN P. KUHN	4-2-98
00-879155	9800	FRACTIONS: +/- DECIMALS: .XX+/- .XXX+/-	FINISH	CHECKED MAHON	4-3-98
NEXT ASSEMBLY	USED ON	ANGLES: +/-		ENGINEERING P. KUHN	4-2-98
APPLICATION		DO NOT SCALE DRAWING		APPROVED	

OEC MEDICAL SYSTEMS, INC.

DWG TITLE: SCH, PCB, CINE BRIDGE, 9800

SIZE D | DWG NO. 00-880921 | REV A1

SCALE: NONE | SHEET 1 OF 28

05-016-9/93

PCI BUS 0

PCI BUS 1

NOTE: ALL 21152 BYPASS CAPACITORS ARE SHOWN ON SHEET 18

NOTE: CUT TRACE AND CONNECT JUMPER TO ENABLE 21152 POWER MANAGMENT

U45 — 3.3 VOLTS PCI_PCI21152AB

P_PAR, P_CBE<3>, P_CBE<2>, P_CBE<1>, P_CBE<0>, P_FRAME, P_TRDY, P_IRDY, P_STOP, P_LOCK, P_IDSEL, P_DEVSEL, P_REQ, P_GNT, P_VIO, P_PERR, P_SERR, P_CLK, BPCC, GOZ, NAND_OUT, P_RST, P_AD<31..0>

S_PAR, S_CBE<3>, S_CBE<2>, S_CBE<1>, S_CBE<0>, S_FRAME, S_TRDY, S_IRDY, S_STOP, S_LOCK, S_DEVSEL, S_REQ<3>, S_REQ<2>, S_REQ<1>, S_REQ<0>, S_VIO, S_GNT<3>, S_GNT<2>, S_GNT<1>, S_GNT<0>, S_PERR, S_SERR, S_CLK_0<4>, S_CLK_0<3>, S_CLK_0<2>, S_CLK_0<1>, S_CLK_0<0>, S_CLK, S_CFN, S_RST, S_AD<31..0>

AD1_<31..0>

INTAn, INTBn, INTCn, INTDn

JTAG: TRSTn, TCK, TMS, TDI, TDO

NOTES:
UNLESS OTHERWISE SPECIFIED
-ALL RESISTORS ARE IN OHMS, 0.1 W, 1%
-ALL CAPACITORS ARE IN MICROFARADS, 50V

PCI BUS-0 TO PCI BUS-1 BRIDGE

DRAWING

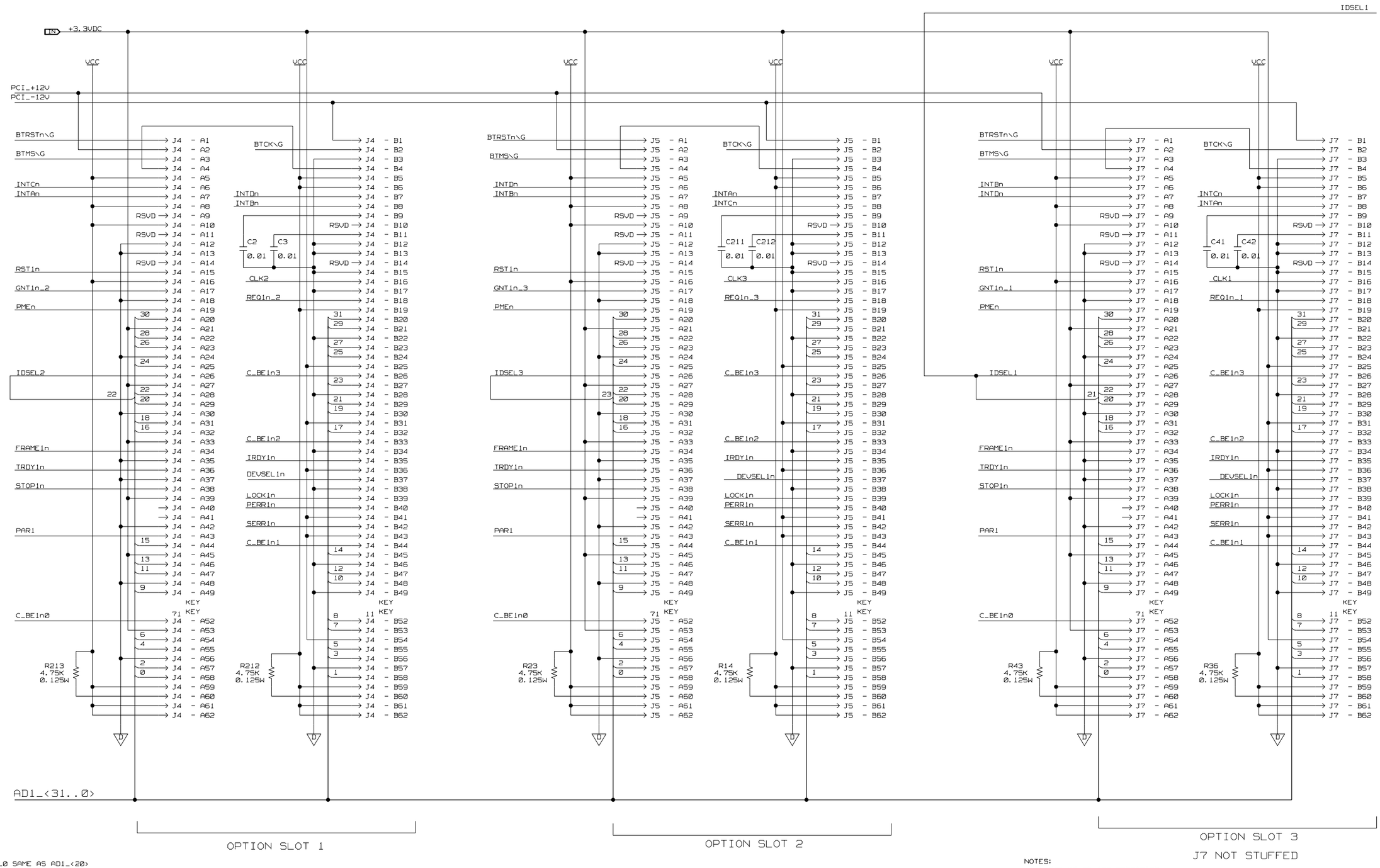
LAST_MODIFIED=Fri Sep 24 14:04:41 1999

OEC MEDICAL SYSTEMS, INC.

SIZE	DWG NO.	REV
D	00-880921	A1

SCALE: | SHEET 2

05-017-9/93



NOTE: IDSEL0 SAME AS AD1_<20>
IDSEL1 SAME AS AD1_<21>
IDSEL2 SAME AS AD1_<22>
IDSEL3 SAME AS AD1_<23>

PCI BUS-1 OPTION SLOTS

NOTES:
UNLESS OTHERWISE SPECIFIED
-ALL RESISTORS ARE IN OHMS, 0.1 W, 1%
-ALL CAPACITORS ARE IN MICROFARADS, 50V

DRAWING

LAST_MODIFIED=Fri Sep 24 14:05:05 1999

OEC MEDICAL SYSTEMS, INC.

SIZE	DWG NO.	REV
D	00-880921	A1

SCALE: | SHEET 3

05-017-9/93

PIXEL I/O, CLOCKS AND CONTROL MODULE

CINE_D<9..0>

PIX_CLK<6..0>

NOTE: PIXCLK15 ROUTED U5-23 >> U6-5 >> U4-48 >> U3-2 >> U3-27 >> R28 (TERMINATION LAST)

NOTE: SEE SHEET 12 FOR CONTROL MODULE PINOUT, POWER, & BYPASSING

IMAGE PROCESSOR PIXEL INTERFACE

P6 - 1 ACQn
P6 - 2 0
P6 - 3 1
P6 - 4 2
P6 - 5 3
P6 - 6 4
P6 - 7 5
P6 - 8 6
P6 - 9 7
P6 - 10 8
P6 - 11 9
P6 - 12 CINE_HDRVn
P6 - 13 CINE_VDRVn
P6 - 14
P6 - 15
P6 - 16
P6 - 17 NC
P6 - 18 NC
P6 - 19 NC
P6 - 20 NC
P6 - 21 CINE_PIXCLK
P6 - 22
P6 - 23
P6 - 24
P6 - 25
P6 - 26
P6 - 27
P6 - 28
P6 - 29
P6 - 30
P6 - 31
P6 - 32
P6 - 33
P6 - 34
P6 - 35
P6 - 36
P6 - 37
P6 - 38
P6 - 39
P6 - 40

PIXCLK15

U6 74FCT88915 100_MHZ FDBK VCC-AN PLLEN LOCK RST LF FREQ-SEL REF-SEL GND-AN

U4 74LCX16374 OE2 CLK2 OE1 CLK1 I7 I6 I5 I4 I3 I2 I1 I0 O7 O6 O5 O4 O3 O2 O1 O0

U5 74LCX16244 OE 4 OE 3 OE 2 OE 1 A3 A2 A1 A0 Y3 Y2 Y1 Y0

NOTE: LOW-SKEW 16244

R37 3.32K
R38 75
C50 330P
R454 3.32K
R455 75
C98 330P
R1 3.32K
R2 75
C12 330P
R4 3.32K
R5 75
C17 330P
R35 3.32K
R225 3.32K
R193 3.32K
R258 3.32K
R221 3.32K
R222 3.32K
R220 3.32K
C25 0.1
R435 75
C704 330P
R363 3.32K

U31 PIXCLK HSYNC VSYNC HIZ RST PPUFIFORST PIXEL TIMING
CS0 CS1 CS2 PCIBCLK LW_Rn WR RD ADS PCIFIFORST PCI TIMING
FFA AFA AEA EFA FFB AFB AEB EFB
BYPASSEDn BYPASSED ENABLE2 ENABLE4 DISKSTAT6 DISKSTAT5 DISKSTAT4 DISKSTAT3 DISKSTAT2 DISKSTAT1 LRCSTAT6 LRCSTAT5 LRCSTAT4 LRCSTAT3 LRCSTAT2 LRCSTAT1
DAT15 DAT14 DAT13 DAT12 DAT11 DAT10 DAT9 DAT8 DAT7 DAT6 DAT5 DAT4 DAT3 DAT2 DAT1 DAT0
ADDCS123 ADDCS122 ADDIN5 ADDIN4 ADDIN3 ADDIN2 CTL_MODULE

STARTACQn STARTRTRVn PIXDVLD PP_LASTn ACQn ACQ RTRVn
LINTI1n LINTI2n
CONFLICTn
DRAMADSn FBADS
CTL_DIAG3n CTL_DIAG2n CTL_DIAG1n CTL_DIAG0n
VSYNC_out HSYNC_out
BANKSEL2 BANKSEL1 BANKSEL0
PCI_PPUn2 PCI_PPUn1 PCI_PPUn0
RD_WRn2 RD_WRn1 RD_WRn0
TXPPOEAB2 TXPPOEAB1 TXPPOEAB0
TXPPOEBA2 TXPPOEBA1 TXPPOEBA0
TXPCOEBA2 TXPCOEBA1 TXPCOEBA0
TXPCOEAB2 TXPCOEAB1 TXPCOEAB0

DS1 PCI FIFO A EMPTY IND; PCI FIFO B EMPTY IND; PCI FIFO FULL IND; ACQUIRE IND

RESETn PPUFIFORSTn CS0n CS1n CS2n BCLK LW_Rn WRn RDn ADSn PCIFIFORSTn PCIFFAn PCIAFAn PCIAEAn PCIEFAn PCIFFBn PCIAFBn PCIAEBn PCIEFBn

DISK DRIVE STATUS
P9 - 1 NC BYPASS_D<1>* 1
P9 - 2 BYPASS_D<2>* 2
P9 - 3 BYPASS_D<3>* 3
P9 - 4 BYPASS_D<4>* 4
P9 - 5 BYPASS_D<5>* 5
P9 - 6 BYPASS_D<6>* 6
P9 - 7 NC FAIL_D<1>* 1
P9 - 8 FAIL_D<2>* 2
P9 - 9 FAIL_D<3>* 3
P9 - 10 FAIL_D<4>* 4
P9 - 11 FAIL_D<5>* 5
P9 - 12 FAIL_D<6>* 6
P9 - 13 ENABLE_2*
P9 - 14 ENABLE_4*
P9 - 15
P9 - 16
P9 - 17
P9 - 18
P9 - 19
P9 - 20

D53 D54 D55 R208 R209 R210 R211 R204 R205 R206 R207 R200 R201 R202 R203 R23 R99 2.21K

U7 74LCX16244 R244 3.32K R311 2.21K

FAIL_D<6..1>*
BYPASS_D<6..1>*
DISK_STAT<14..1>
LAD<31..0>
LA<23..2>

NOTES:
UNLESS OTHERWISE SPECIFIED
-ALL RESISTORS ARE IN OHMS, 0.1 W, 1%
-ALL CAPACITORS ARE IN MICROFARADS, 50V

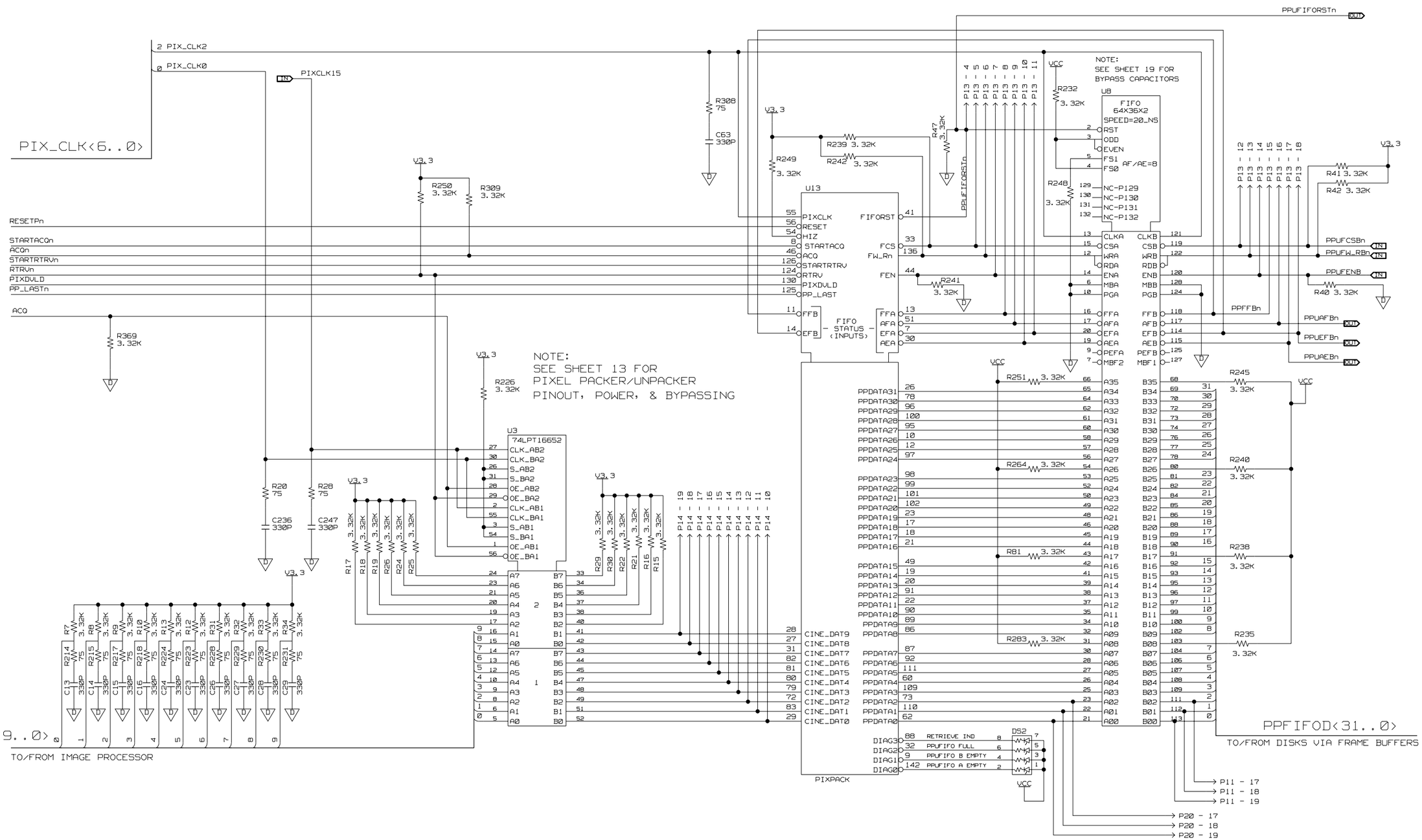
DRAWING LAST_MODIFIED=Fri Sep 24 14:05:42 1999

OEC MEDICAL SYSTEMS, INC.

SIZE D | DWG NO. 00-880921 | REV A1 | SCALE: | SHEET 4

05-017-9/93

PIXEL PACKER/UNPACKER & FIFO



NOTES:
UNLESS OTHERWISE SPECIFIED
-ALL RESISTORS ARE IN OHMS, 0.1 W, 1%
-ALL CAPACITORS ARE IN MICROFARADS, 50V

DRAWING
LAST_MODIFIED=Fri Sep 24 14:06:06 1999

OEC MEDICAL SYSTEMS, INC.

SIZE	DWG NO.	REV
D	00-880921	A1
SCALE:	SHEET 5	

05-017-9/93

NOTE:
SEE SHEET 14 FOR
MEMCTL MODULE 0
PINOUT, POWER, & BYPASSING

V3.3
R276 3.32K
R253 3.32K
R310 3.32K
R85 3.32K

U16
476P
RESETPn
PCIFIFORSTn
PPUFIFORSTn
BANKSEL0n
PCI_PPUn0
RD_WRn0
DRAMADSn
PP_LASTn
PPUAFBn
PPUAEBn
PPUEFBn
PCIAFBn
PCIAEBn
PCIEFBn
CLK
RESET
PCIFIFORST
PPUFIFORST
BANKSEL
PCI_PPUn
RD_WRn
ADS
PP_LAST
HIZ
PPUAFB
PPUAEB
PPUEFB
PCIAFB
PCIAEB
PCIEFB
PPUFEN
PPUFCSn
PPUFW_Rn
PCIFEN
PCIFCSn
PCIFW_Rn
CKE
CSM
RAS
CAS
WE
UDQM
LDQM
ADD21
ADD20
ADD19
ADD18
ADD17
ADD16
ADD15
ADD14
ADD13
ADD12
ADD11
ADD10
ADD9
ADD8
ADD7
ADD6
ADD5
ADD4
ADD3
ADD2
ADDBX11
ADDBX10
ADDBX9
ADDBX8
ADDBX7
ADDBX6
ADDBX5
ADDBX4
ADDBX3
ADDBX2
ADDBX1
ADDBX0
MEMCTL0

P11 - 11
P11 - 12
P11 - 13
P11 - 10
P11 - 9
P11 - 8
P11 - 7
P11 - 6
P11 - 5
P11 - 4
P11 - 3 (HPCLK)

PIXEL PACKER FIFO STATUS
PCI FIFO STATUS

PPUFENB
PPUFCSBn
PPUFW_RBn
PCIFENB
PCIFCSBn
PCIFW_RBn

PIXEL PACKER FIFO CONTROLS
PCI FIFO CONTROLS

R69 3.32K
R65 3.32K
R441 3.32K
R260 3.32K
R412 3.32K
R166 3.32K
R171 3.32K
R100 3.32K
R330 3.32K
R327 3.32K
R314 3.32K
R364 3.32K
R343 3.32K
R374 3.32K
R120 3.32K
R468 3.32K
R467 3.32K
R189 3.32K
R188 3.32K

IBADD<21..2>
R448 75
C97 330P

R319 3.32K
R320 3.32K
R338 3.32K
R396 3.32K

TXPCOEAB0
TXPCOEBA0n
TXPPOEAB0
TXPPOEBA0n

U19
U23
U26
U33
U34
U39
74LCX16652
SDRAM_1MX16
SPEED=10_NS
CLK_AB2
CLK_BA2
S_AB2
S_BA2
OE_AB2
OE_BA2
CLK_AB1
CLK_BA1
S_AB1
S_BA1
OE_AB1
OE_BA1
CLK
CKE
CS
RAS
CAS
WE
UDQM
LDQM
A0 A1 A2 A3 A4 A5 A6 A7
B0 B1 B2 B3 B4 B5 B6 B7
A00 A01 A02 A03 A04 A05 A06 A07 A08 A09 A10 A11
DO00 DO01 DO02 DO03 DO04 DO05 DO06 DO07 DO08 DO09 DO10 DO11 DO12 DO13 DO14 DO15

SEE NOTE 2.

PIX_CLK<6..0>
PIX_CLK3

FRAME0ADDR<11..0>
FRAME0DATA<31..0>

P11 - 16
P11 - 15
P11 - 14

PPFIFOD<31..0>
PCFIFOD<31..0>

PIXEL PACKER FIFO DATA
PCI FIFO DATA

FRAME BUFFER 0

NOTES:
1 - UNLESS OTHERWISE SPECIFIED
ALL RESISTORS ARE IN OHMS, 0.1 W, 1%
ALL CAPACITORS ARE IN MICROFARADS, 50V
2 - NOTE DATA LINE REVERSAL GOING TO RAM.

DRAWING
LAST_MODIFIED=Fri Sep 24 14:06:35 1999

OEC MEDICAL SYSTEMS, INC.

SIZE	DWG NO.	REV
D	00-880921	A1
SCALE:		SHEET 6

05-017-9/93

NOTE:
SEE SHEET 15 FOR
MEMCTL MODULE 1
PINOUT, POWER, & BYPASSING

U17
453P
MEMCTL1

PIXEL PACKER FIFO STATUS
PCI FIFO STATUS

PIXEL PACKER FIFO CONTROLS
PCI FIFO CONTROLS

IBADD<21..2>

FRAME1ADDR<11..0>

FRAME1DATA<31..0>

PIX_CLK<5..0>

PPFIFOD<31..0>

PCFIFOD<31..0>

PIXEL PACKER FIFO DATA

PCI FIFO DATA

SEE NOTE 2.

FRAME BUFFER 1

NOTES:
1 - UNLESS OTHERWISE SPECIFIED
ALL RESISTORS ARE IN OHMS, 0.1 W, 1%
ALL CAPACITORS ARE IN MICROFARADS, 50V
2 - NOTE DATA LINE REVERSAL GOING TO RAM.

DRAWING
LAST_MODIFIED=Fri Sep 24 14:07:00 1999

OEC MEDICAL SYSTEMS, INC.

SIZE	DWG NO.	REV
D	00-880921	A1
SCALE:		SHEET 7

05-017-9/93

NOTE:
SEE SHEET 16 FOR
MEMCTL MODULE 2
PINOUT, POWER, & BYPASSING

V3.3
R71 3.32K
R77 3.32K
R70 3.32K
R281 3.32K

U18
455P
RESETPn
PCIFIFORSTn
PPUFIFORSTn
BANKSEL2n
PCI_PPUn2
RD_WRn2
DRAMADSn
PP_LASTn
CLK
RESET
PCIFIFORST
PPUFIFORST
BANKSEL
PCI_PPUn
RD_WRn
ADS
PP_LAST
HIZ

PIXEL PACKER FIFO STATUS
PCI FIFO STATUS
PPUAFBn
PPUAEBn
PPUEFBn
PCIAFBn
PCIAEBn
PCIEFBn
PPUAFB
PPUAEB
PPUEFB
PCIAFB
PCIAEB
PCIEFB

PPUFEN
PPUFCSn
PPUFW_Rn
PCIFEN
PCIFCSn
PCIFW_Rn
CKE
CSM
RAS
CAS
WE
UDQM
LDQM

P18 - 11
P18 - 12
P18 - 13
P18 - 10
P18 - 9
P18 - 8
P18 - 7
P18 - 6
P18 - 5
P18 - 4

R331 3.32K
R64 3.32K
R351 3.32K
R54 3.32K

PPUFENB
PPUFCSBn
PPUFW_RBn
PCIFENB
PCIFCSBn
PCIFW_RBn
PIXEL PACKER FIFO CONTROLS
PCI FIFO CONTROLS

IBADD<21..2>
P18 - 3(HPCLK)
R182 75
C705 330P

ADD21
ADD20
ADD19
ADD18
ADD17
ADD16
ADD15
ADD14
ADD13
ADD12
ADD11
ADD10
ADD9
ADD8
ADD7
ADD6
ADD5
ADD4
ADD3
ADD2
MEMCTL2

ADDBX11
ADDBX10
ADDBX9
ADDBX8
ADDBX7
ADDBX6
ADDBX5
ADDBX4
ADDBX3
ADDBX2
ADDBX1
ADDBX0

R354 3.32K 11
R342 3.32K 10
R391 3.32K 9
R134 3.32K 8
R392 3.32K 7
R135 3.32K 6
R390 3.32K 5
R133 3.32K 4
R147 3.32K 3
R405 3.32K 2
R148 3.32K 1
R149 3.32K 0

R312 3.32K
R321 3.32K
R315 3.32K

V3.3
R52 3.32K
R50 3.32K

V3.3
R76 3.32K
R68 3.32K

TXPC0EAB2
TXPC0EBA2n
TXPP0EAB2
TXPP0EBA2n

U21 74LCX16652
U25 74LCX16652
U32 74LCX16652
U38 74LCX16652
CLK_AB2
CLK_BA2
S_AB2
S_BA2
OE_AB2
OE_BA2
CLK_AB1
CLK_BA1
S_AB1
S_BA1
OE_AB1
OE_BA1
A7 A6 A5 A4 A3 A2 A1 A0
B7 B6 B5 B4 B3 B2 B1 B0

PIX_CLK<5..0>
PIX_CLK5

U28 SDRAM_1MX16
SPEED=10_NS
CLK
CKE
CS
RAS
CAS
WE
UDQM
LDQM
A11 A10 A09 A08 A07 A06 A05 A04 A03 A02 A01 A00
DQ15 DQ14 DQ13 DQ12 DQ11 DQ10 DQ09 DQ08 DQ07 DQ06 DQ05 DQ04 DQ03 DQ02 DQ01 DQ00
PACK_TYPE=TSOPII
SEE NOTE 2.

U37 SDRAM_1MX16
SPEED=10_NS
PACK_TYPE=TSOPII
SEE NOTE 2.

FRAME2ADDR<11..0>
FRAME2DATA<31..0>
P18 - 16
P18 - 15
P18 - 14

PIXEL PACKER FIFO DATA
PPFIFOD<31..0>
PCI FIFO DATA
PCFIFOD<31..0>

FRAME BUFFER 2

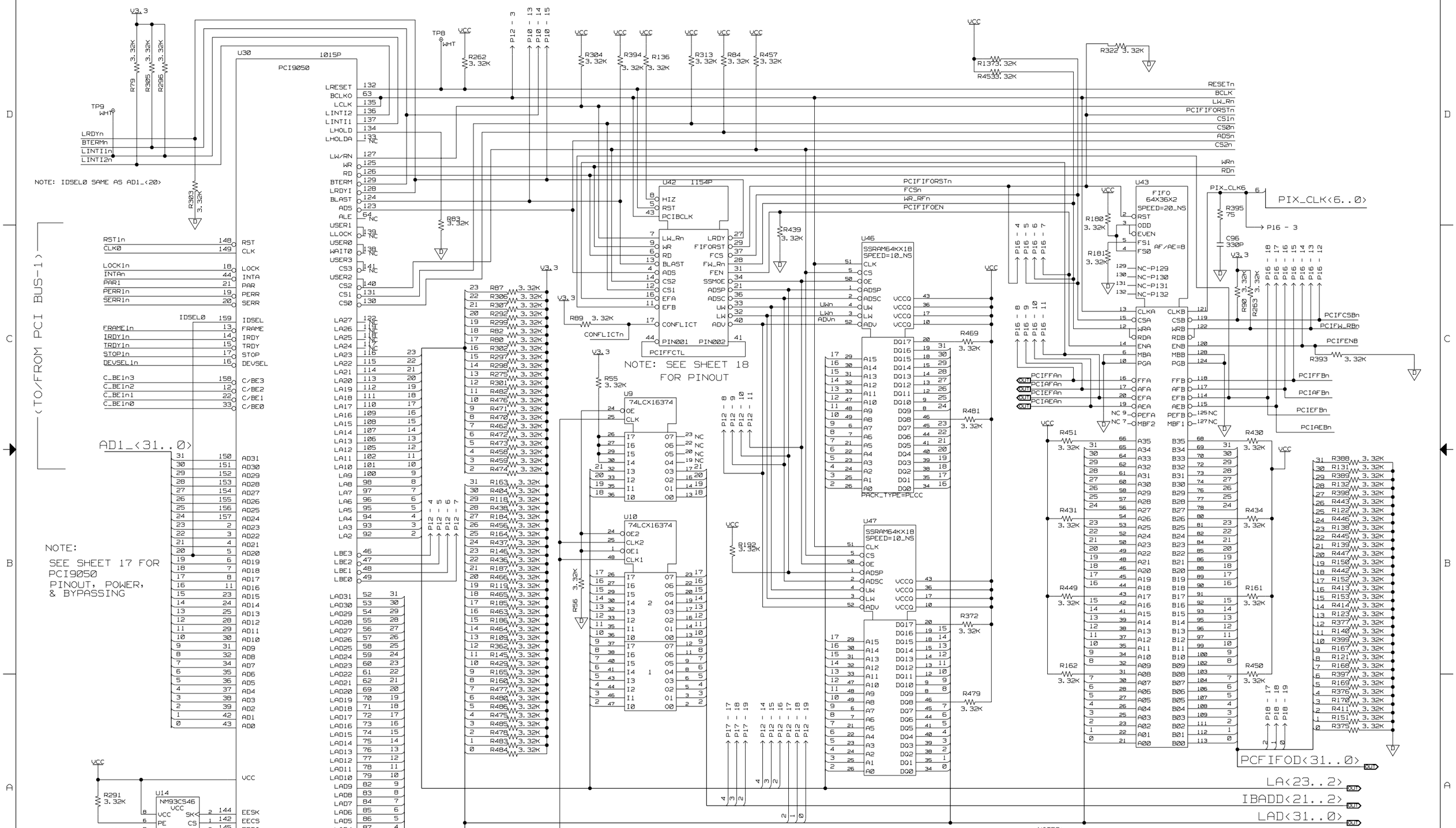
NOTES:
1 - UNLESS OTHERWISE SPECIFIED
ALL RESISTORS ARE IN OHMS, 0.1 W, 1%
ALL CAPACITORS ARE IN MICROFARADS, 50V
2 - NOTE DATA LINE REVERSAL GOING TO RAM.

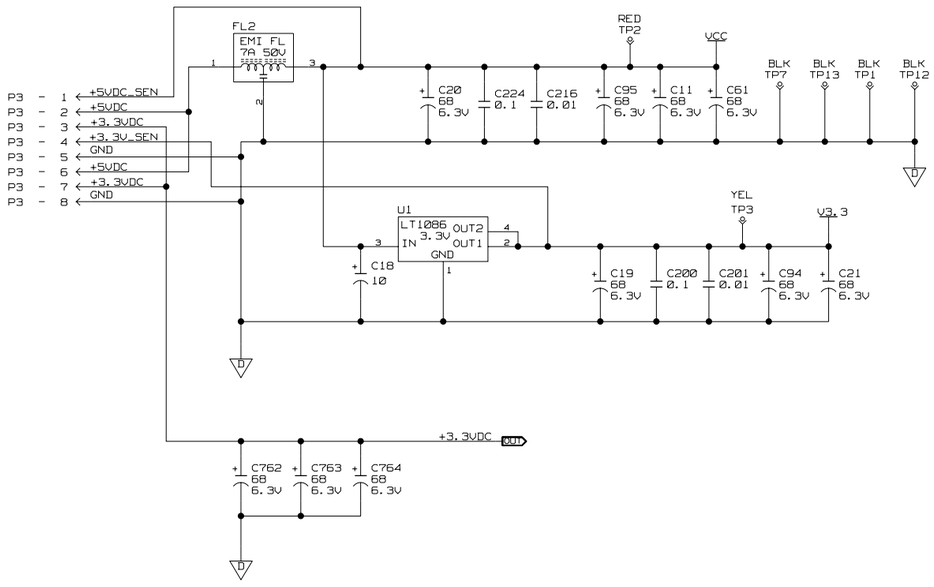
DRAWING
LAST_MODIFIED=Fri Sep 24 14:07:39 1999

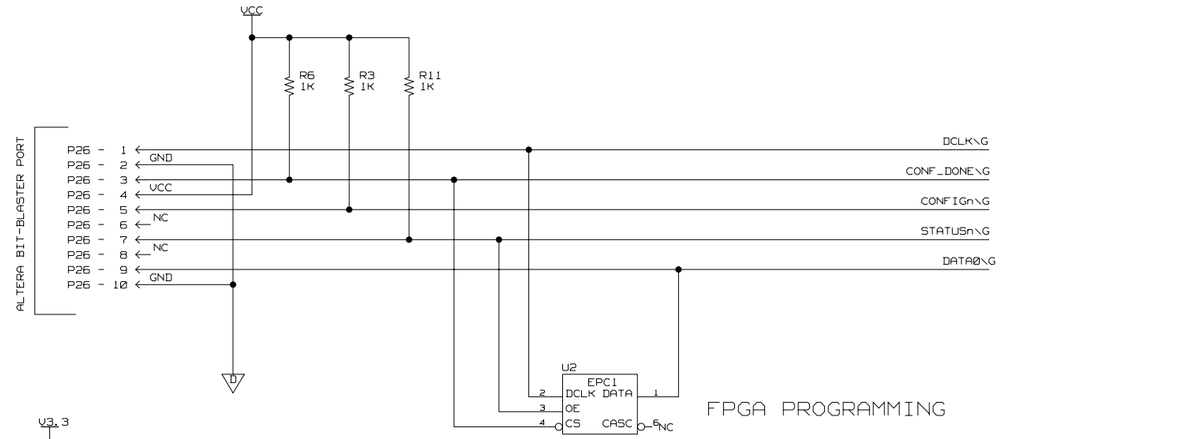
OEC MEDICAL SYSTEMS, INC.

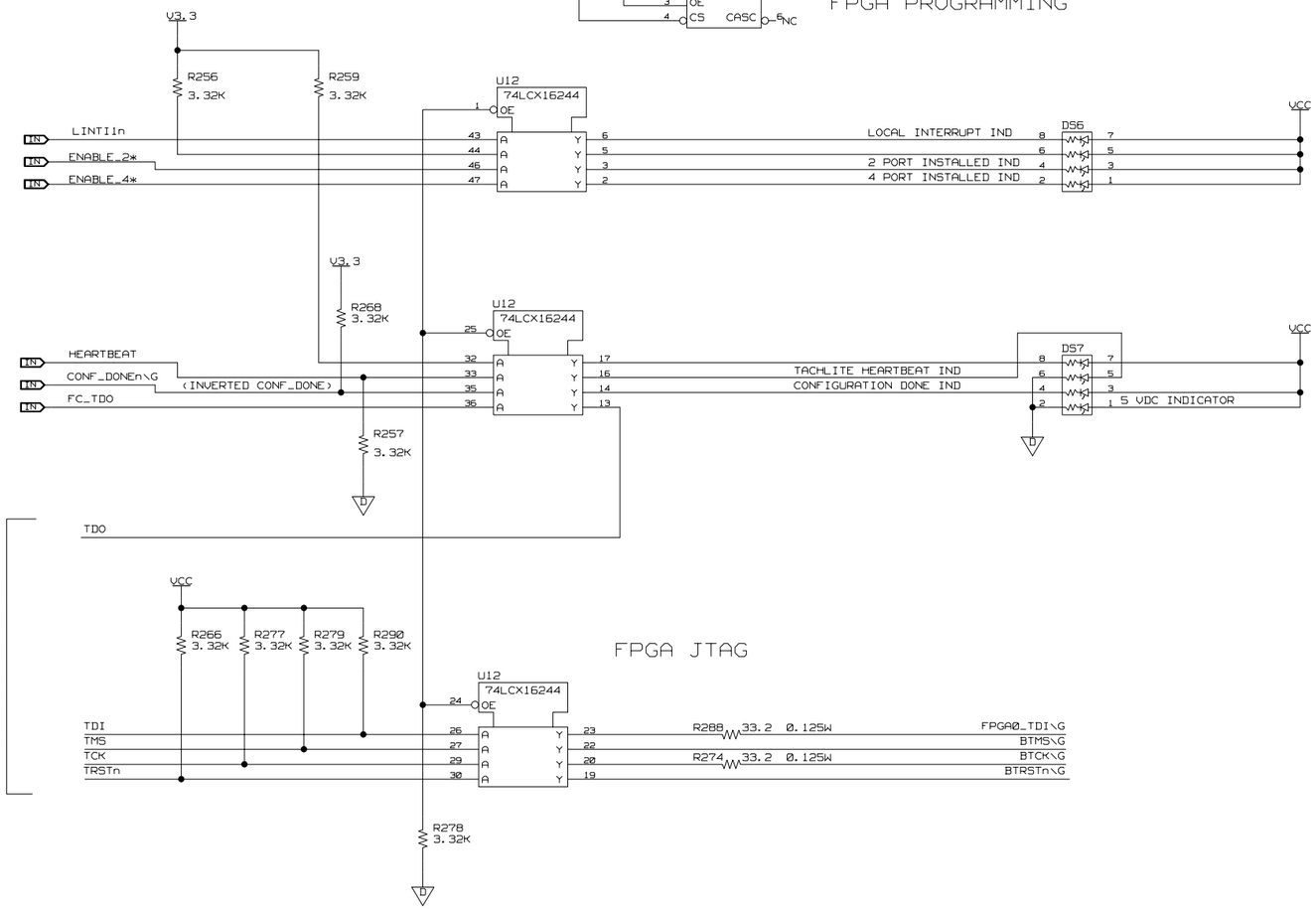
SIZE	DWG NO.	REV
D	00-880921	A1
SCALE:		SHEET 8

05-017-9/93


U30 1015P PCI9050
U42 1154P
U43 FIFO 64X36X2 SPEED=20_NS
U46 SSRAM64KX18 SPEED=10_NS
U47 SSRAM64KX18 SPEED=10_NS
U9 74LCX16374
U10 74LCX16374
U14 NM93CS46
(TO/FROM PCI BUS-1)
AD1_<31..0>
NOTE: IDSEL0 SAME AS AD1_<20>
NOTE: SEE SHEET 18 FOR PINOUT
NOTE: SEE SHEET 17 FOR PCI9050 PINOUT, POWER, & BYPASSING
PACK_TYPE=PLCC
PIX_CLK<6..0>
PCFIFOD<31..0>
LA<23..2>
IBADD<21..2>
LAD<31..0>
NOTES: UNLESS OTHERWISE SPECIFIED -ALL RESISTORS ARE IN OHMS, 0.1 W, 1% -ALL CAPACITORS ARE IN MICROFARADS, 50V
PCI BUS-1 INTERFACE, MEM, & FIFO
OEC MEDICAL SYSTEMS, INC.
DRAWING
LAST_MODIFIED=Fri Sep 24 14:08:05 1999







NOTES:
UNLESS OTHERWISE SPECIFIED
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-ALL CAPACITORS ARE IN MICROFARADS, 50V

POWER DISTRIBUTION & FPGA PROGRAMMING

DRAWING LAST_MODIFIED=Fri Sep 24 14:08:50 1999

OEC MEDICAL SYSTEMS, INC.

SIZE	DWG NO.	REV
D	00-880921	A1

SCALE: | SHEET 10

05-017-9/93

HP_TACHLITE

HPFC-5100B

PCI BUS INTERFACE

3.3 VOLT POWER SUPPLY PINS

I/O SUPPLY PINS

FIBRE CHANNEL INTERFACE

TEST INTERFACE

EXTERNAL MEMORY INTERFACE

NOTE: IDSEL1 SAME AS AD1_<21>

NOTE: COMPONENTS SHOULD BE EQUIDISTANT FROM 32.2 OHM RESISTORS

CLOCK TERMINATION SEQUENCE
CLK > 32.2 OHM > COMPONENT > NETWORK

106.25 MHZ CLOCK 75 Network Termination

106.25 MHz Clock Network Termination

TACHLITE 5.0 V and 3.3 V SUPPLY

TRANSCEIVER 3.3 V SUPPLY

2 W RESISTOR TO BE INSTALLED FOR HEAT DISSIPATION IF NEEDED

P8 IS A 9 PIN DSUB CONNECTOR PINS 10 & 11 ARE SHIELD

TO FC-AL

NOTE: SEE PAGE 20 FOR BYPASSING

NOTE: CUT TRACE WIRE JUMPER TO ENABLE FLOW THRU MEM

DIGITAL GROUND

A1	J3	L10	T1
D4	J9	L11	U4
D7	J10	L12	U8
D8	J11	M9	U13
D12	J12	M10	U17
D13	K9	M11	W5
D17	K10	M12	Y12
F19	K11	N4	
H4	K12	N17	
H17	L9	P18	

U29 — PCI BUS INTERFACE

C_BE7	Y11
C_BE6	W11
C_BE5	V11
C_BE4	U11
C_BE3	C_BEIn3 M4
C_BE2	C_BEIn2 U1
C_BE1	C_BEIn1 Y1
C_BE0	C_BEIn0 Y5
PAR64	V12
PAR	PAR1 W2
ACK64	V10
REQ64	Y10
REQ	REQIn_1 K2
GNT	GNTIn_1 J1
CLK	CLK1 Y6
DEVSEL	DEVSELIn U3
IDSEL	IDSEL1 N1
FRAME	FRAMEIn T3
INTA	INTBn J2
IRDY	IRDYIN U2
PERR	PERRIn W1
SERR	SERRIn V3
STOP	STOPIn V2
TRDY	TRDYIn T4
RST	RSTIn Y7

U22 — LTI086 OUT2 3.3V OUT1 (IN / GND)

U11 — LTI086 OUT2 3.3V OUT1 (IN / GND)

FL3, FL1 — EMI FL 7A 50V

U15 — 3.3 VOLTS VSC7125

EN_CDET	24
COM_DET	47
EWRAP	19
LCK_REF	27
RCLK	31
RCLKn	30
REFCLK	22
V33_TXA	18
V33_RXA	50
V33_PECL	57

TACHRX<9..0>

RX9	34
RX8	35
RX7	36
RX6	38
RX5	39
RX4	40
RX3	41
RX2	43
RX1	44
RX0	45
RX+	54
RX-	52
RYCAP1	49
RXCAP0	48

TACHTX<9..0>

TX9	13
TX8	12
TX7	11
TX6	9
TX5	8
TX4	7
TX3	6
TX2	4
TX1	3
TX0	2
TX+	62
TX-	61
TXCAP1	16
TXCAP0	17

U41 — SSRAM64KX36P, SPEED=10_NS

CLK	89
CE	98
CE2	92
CE2	97
OE	86
ADSC	85
ADSP	84
ADV	83
BWE	87
BW4	96
BW3	95
BW2	94
BW1	93
GW	88
ZZ	64
MODE	31
FT	14
A16_NC	50
A15	49
A14	48
A13	47
A12	46
A11	45
A10	44
A9	81
A8	82
A7	99
A6	100
A5	33
A4	32
A3	35
A2	34
A1	36
A0	37
DQP4	30
DQP3	1
DQP2	80
DQP1	51
DQ32	29
DQ31	28
DQ30	25
DQ29	24
DQ28	23
DQ27	22
DQ26	19
DQ25	18
DQ24	13
DQ23	12
DQ22	9
DQ21	8
DQ20	7
DQ19	6
VCCQ	91
VCCQ	77
VCCQ	70
VCCQ	66
VCCQ	65
VCCQ	61
VCCQ	54
VCCQ	41
VCCQ	27
VCCQ	20
VCCQ	16
VCCQ	15
VCCQ	11
VCCQ	4

PACK_TYPE=PBGA

PACK_TYPE=TQFP

HEARTBEAT

FC_TDO

BTMS\G

BTCK\G

BTRST\G

FPGA4_TDO\G

TACHADDR<17..1>

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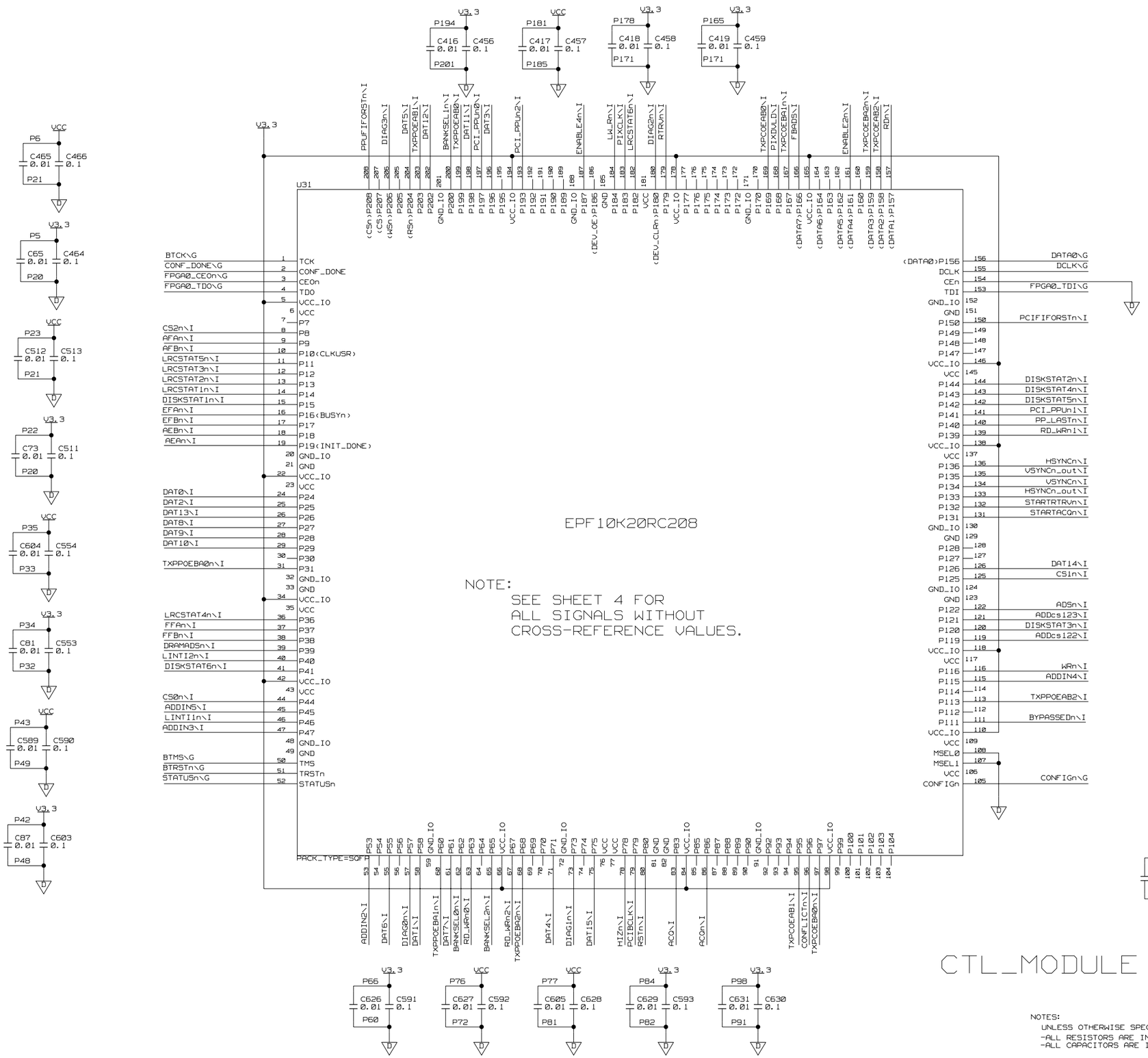
MPAR<3..0>

05-017-9/93



NOTE:
SEE SHEET 4 FOR
ALL SIGNALS WITHOUT
CROSS-REFERENCE VALUES.

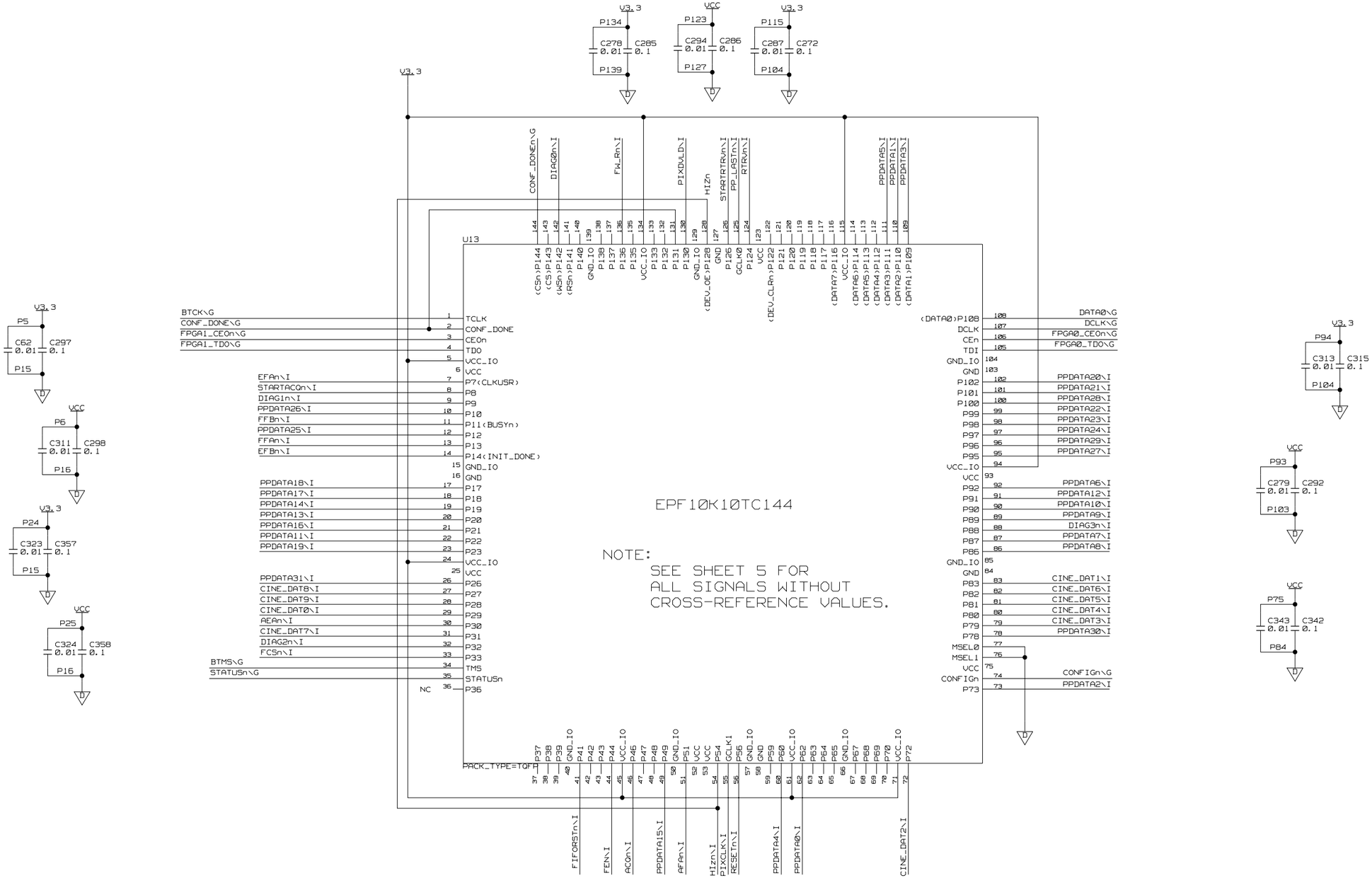
CTL_MODULE ALTERA PINOUT

NOTES:
UNLESS OTHERWISE SPECIFIED
-ALL RESISTORS ARE IN OHMS, 0.1 W, 1%
-ALL CAPACITORS ARE IN MICROFARADS, 50V

OEC MEDICAL SYSTEMS, INC.

SIZE	DWG NO.	REV
D	00-880921	A1
SCALE:	SHEET 12	

05-017-9/93



PIXPACK ALTERA PINOUT

NOTES:
UNLESS OTHERWISE SPECIFIED
-ALL RESISTORS ARE IN OHMS, 0.1 W, 1%
-ALL CAPACITORS ARE IN MICROFARADS, 50V

DRAWING

LAST_MODIFIED=Fri Sep 24 14:17:55 1999

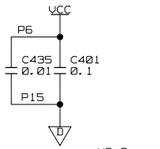
OEC MEDICAL SYSTEMS, INC.

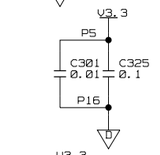
SIZE	DWG NO.	REV
D	00-880921	A1
SCALE:		SHEET 13

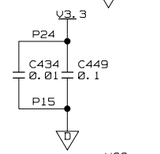
05-017-9/93

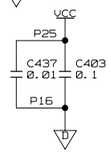
HP LOGIC ANALYZER
(TEMPORARY)

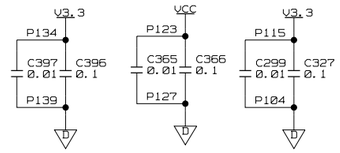
P21 - 4 ⟵ wakeup
P21 - 5 ⟵ pcird
P21 - 6 ⟵ data_valid
P21 - 7 ⟵ pciwr
P21 - 8 ⟵ refr
P21 - 9 ⟵ mrs
P21 - 10 ⟵ dcab
P21 - 11 ⟵ actv
P21 - 12 ⟵ read
P21 - 13 ⟵ ppuwr
P21 - 14 ⟵ ppurd
P21 - 15 ⟵ writ
P21 - 16 ⟵ idle
P21 - 17 ⟵ INIT
P21 - 18 ⟵ slfref
P21 - 19 ⟵ slfr

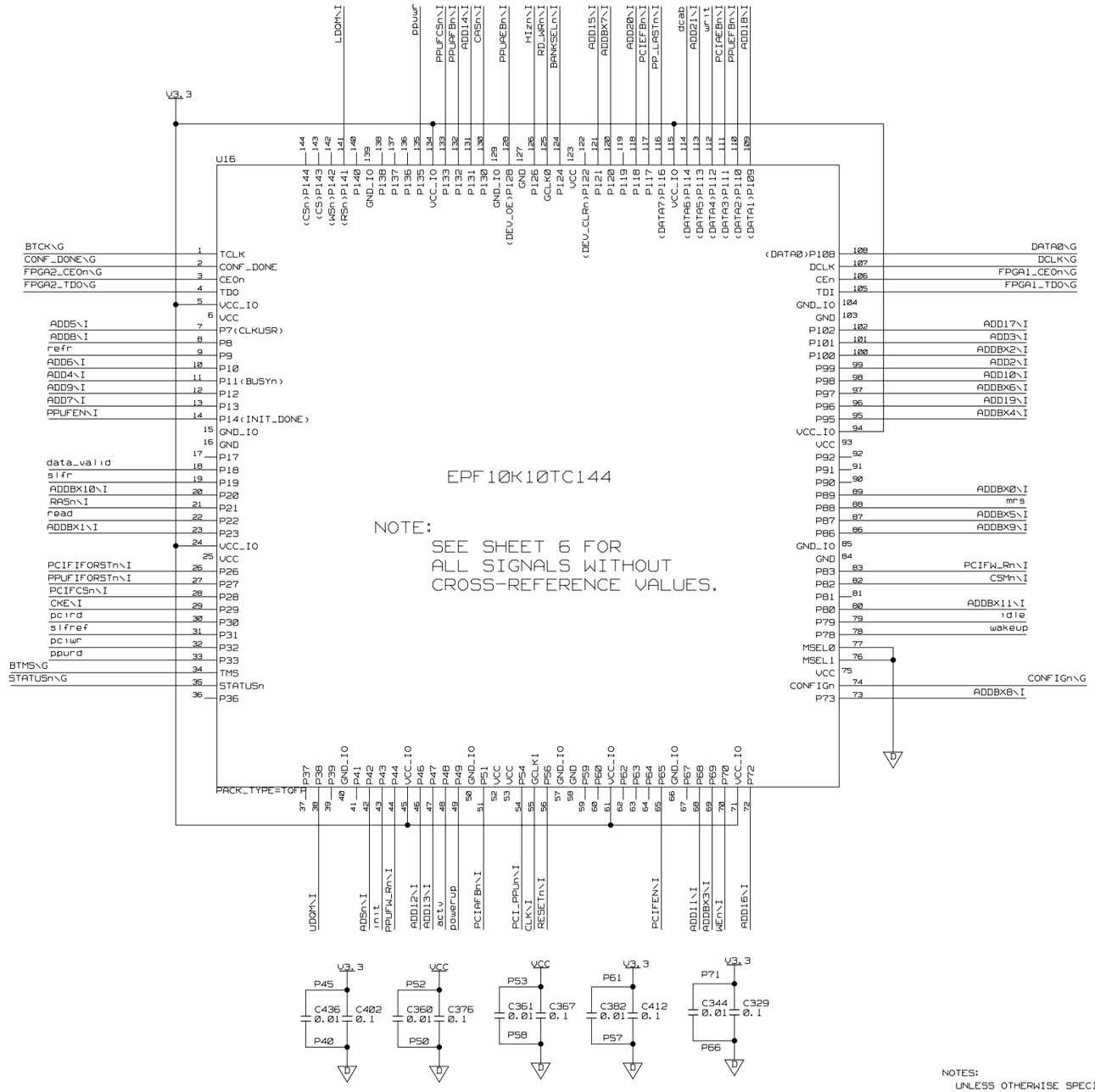




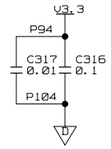


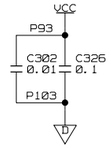


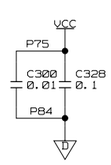




NOTE:
SEE SHEET 6 FOR
ALL SIGNALS WITHOUT
CROSS-REFERENCE VALUES.







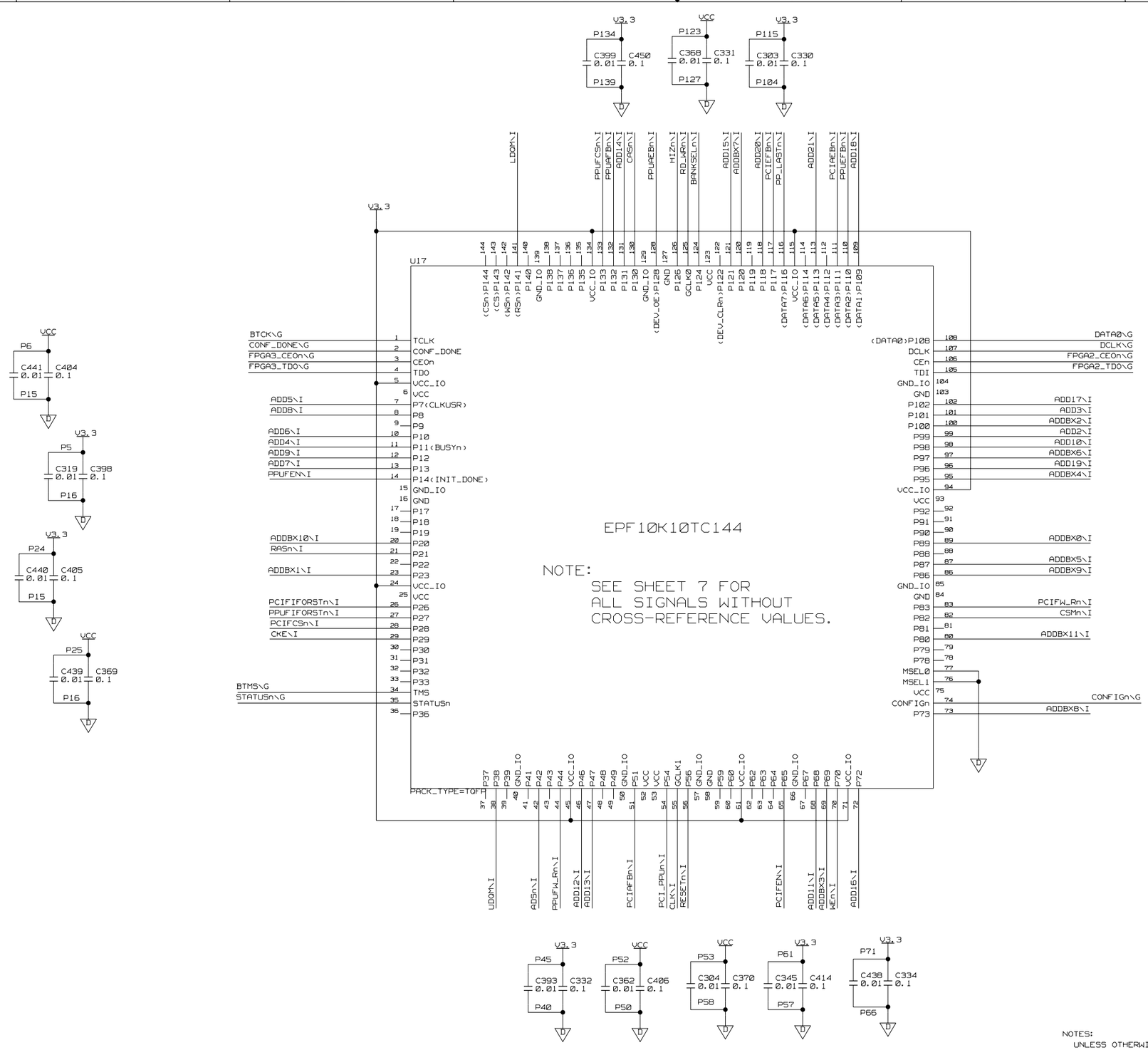
NOTES:
UNLESS OTHERWISE SPECIFIED
-ALL RESISTORS ARE IN OHMS, 0.1 W, 1%
-ALL CAPACITORS ARE IN MICROFARADS, 50V

MEMCTL0 ALTERA PINOUT

OEC MEDICAL SYSTEMS, INC.

SIZE D | DWG NO. 00-880921 | REV A1 | SCALE: | SHEET 14

05-017-9/93



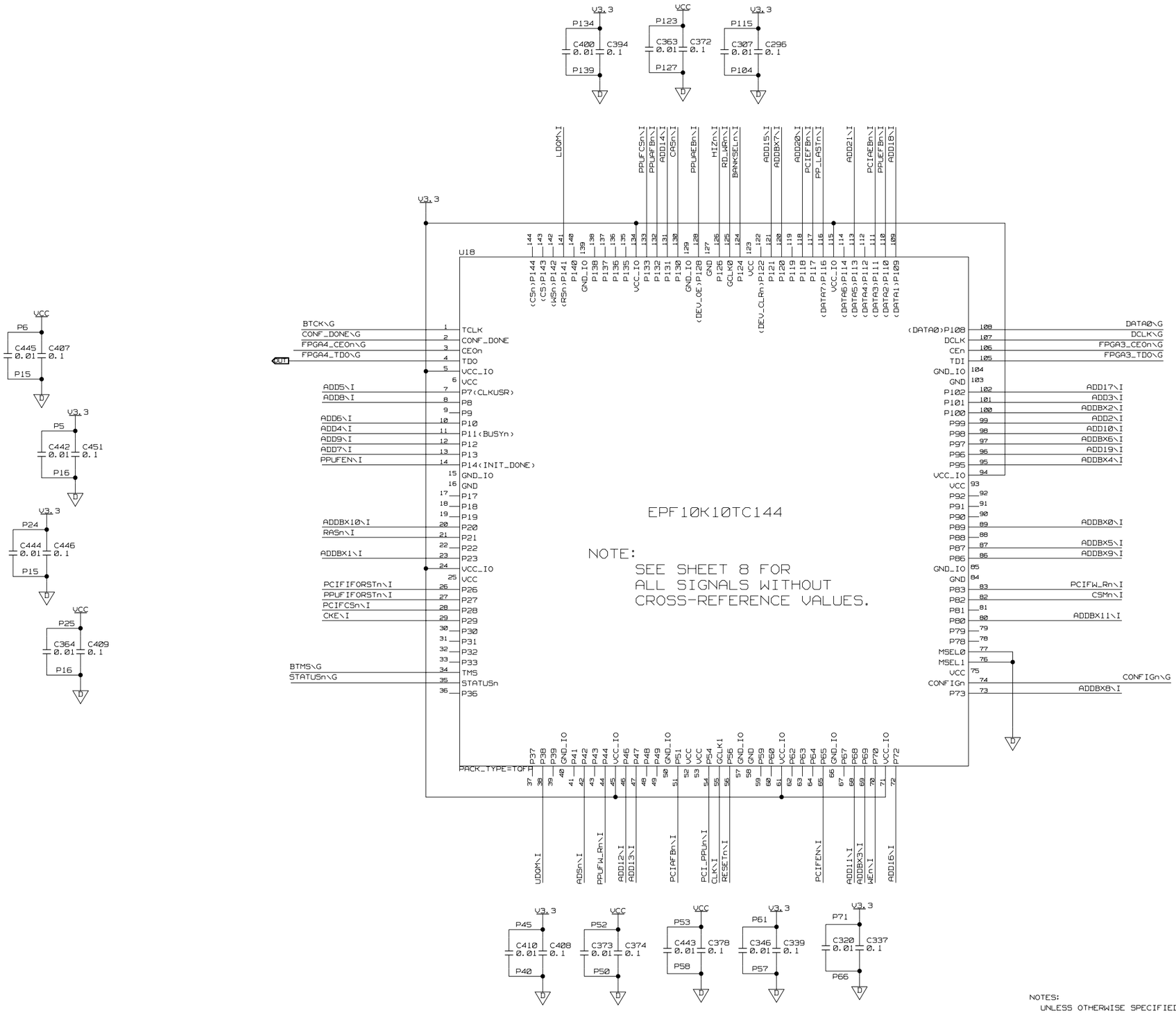
MEMCTL1 ALTERA PINOUT

NOTES:
UNLESS OTHERWISE SPECIFIED
-ALL RESISTORS ARE IN OHMS, 0.1 W, 1%
-ALL CAPACITORS ARE IN MICROFARADS, 50V

OEC MEDICAL SYSTEMS, INC.

SIZE	DWG NO.	REV
D	00-880921	A1
SCALE:		SHEET 15

05-017-9/93



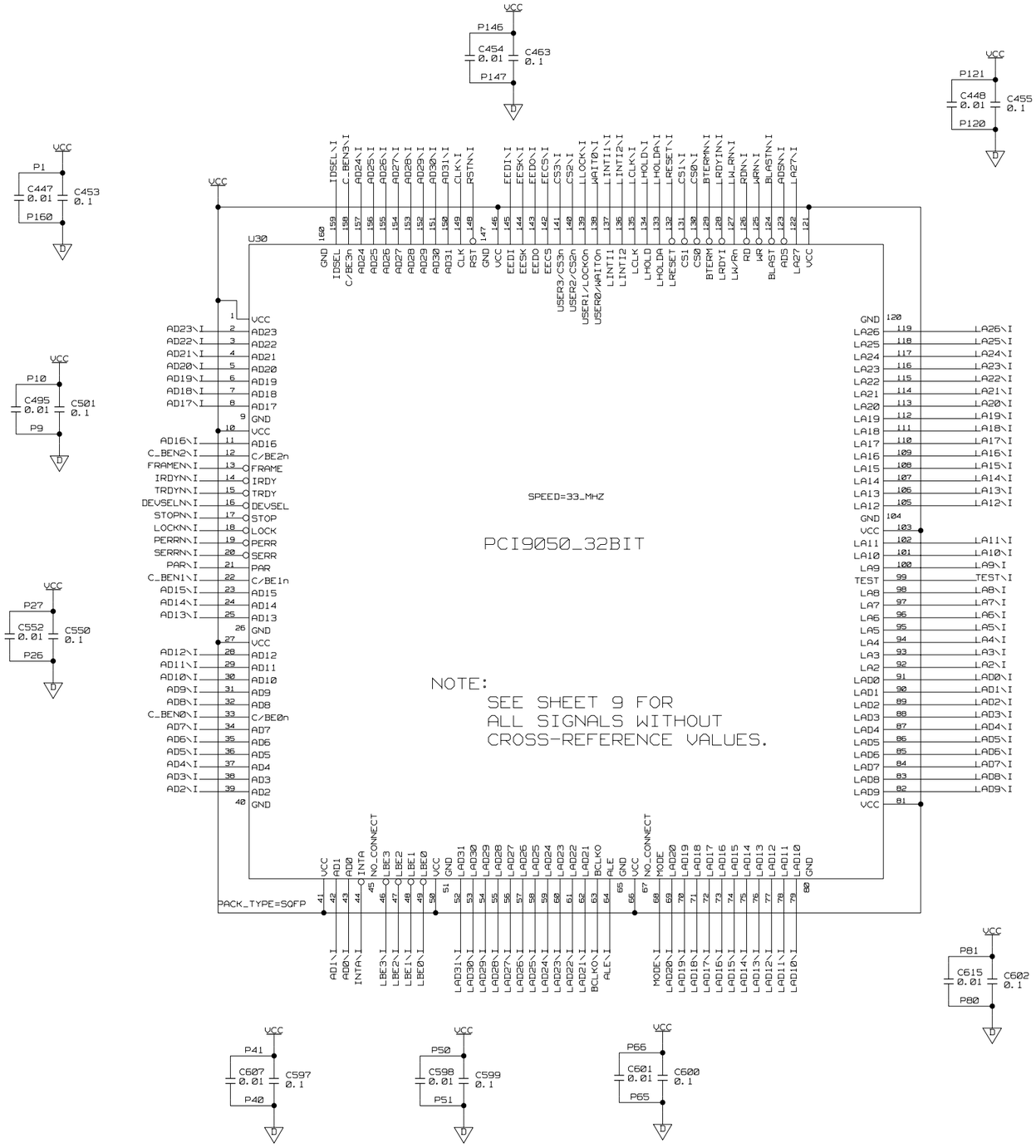
MEMCTL2 ALTERA PINOUT

NOTES:
UNLESS OTHERWISE SPECIFIED
-ALL RESISTORS ARE IN OHMS, 0.1 W, 1%
-ALL CAPACITORS ARE IN MICROFARADS, 50V

OEC MEDICAL SYSTEMS, INC.

SIZE	DWG NO.	REV
D	00-880921	A
SCALE:	SHEET 16	

05-017-9/93



NOTE:
SEE SHEET 9 FOR
ALL SIGNALS WITHOUT
CROSS-REFERENCE VALUES.

PLX TECHNOLOGIES PCI9050 PINOUT

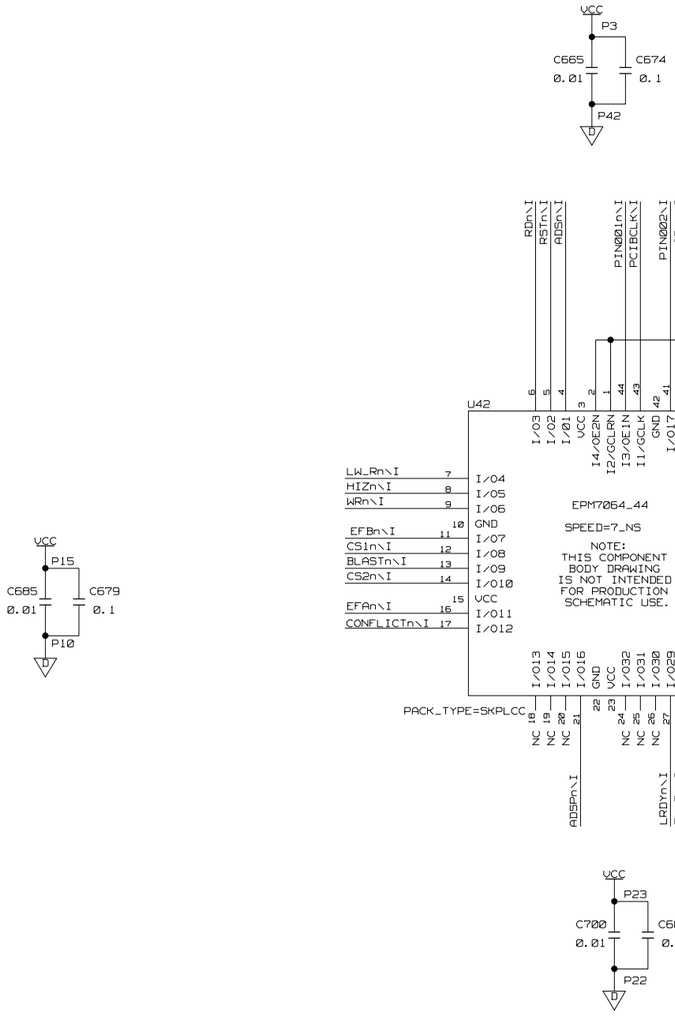
NOTES:
UNLESS OTHERWISE SPECIFIED
-ALL RESISTORS ARE IN OHMS, 0.1 W, 1%
-ALL CAPACITORS ARE IN MICROFARADS, 50V

DRAWING LAST_MODIFIED=Fri Sep 24 14:16:31 1999

OEC MEDICAL SYSTEMS, INC.

SIZE	DWG NO.	REV
D	00-880921	A1
SCALE:	SHEET 17	

05-017-9/93



NOTE:

SEE SHEET 9 FOR ALL SIGNALS
WITHOUT CROSS REFERENCE DESIGNATORS.

PCI FIFO CONTROL ALTERA PINOUT

NOTES:
UNLESS OTHERWISE SPECIFIED
-ALL RESISTORS ARE IN OHMS, 0.1 W, 1%
-ALL CAPACITORS ARE IN MICROFARADS, 50V

OEC MEDICAL SYSTEMS, INC.

SIZE	DWG NO.	REV
D	00-880921	A1
SCALE:	SHEET 18	

BYPASS CAPACITORS INTENDED FOR DEC 21152 (SHT 2)

3.3 V

C673 0.01, C690 0.1, C672 0.01, C689 0.1, C671 0.01, C688 0.1, C670 0.01, C687 0.1, C682 0.01, C678 0.1, C697 0.01, C698 0.1, C709 0.01, C717 0.1
C728 0.01, C723 0.1, C734 0.01, C733 0.1, C751 0.01, C756 0.1, C740 0.01, C741 0.1, C742 0.01, C743 0.1, C744 0.01, C738 0.1, C752 0.01, C745 0.1
C757 0.01, C746 0.1, C753 0.01, C747 0.1, C731 0.01, C732 0.1, C730 0.01, C729 0.1, C718 0.01, C710 0.1, C699 0.01, C692 0.1, C683 0.01, C684 0.1

BYPASS CAPACITORS INTENDED FOR 74FCT88915 (SHT 4)

VCC

C235 0.01, C225 0.1, C214 0.01, C215 0.1, C22 0.01, C230 0.1, C30 0.01, C244 0.1, C248 0.01, C249 0.1

BYPASS CAPACITORS INTENDED FOR 74LCX16244 & 74LCX16374's (SHEETS 4 & 9)

3.3

C226 0.01, C227 0.1, C237 0.1, C238 0.01
C228 0.01, C229 0.1, C239 0.1, C240 0.01
C231 0.01, C232 0.1, C241 0.1, C242 0.01
C283 0.01, C284 0.1, C312 0.1, C314 0.01
C260 0.01, C269 0.1, C275 0.1, C277 0.01
C270 0.01, C271 0.1, C281 0.1, C282 0.01

BYPASS CAPACITORS INTENDED FOR 1M X 16 SDRAMS (SHT 6, 7, & 8)

3.3

C533 0.01, C505 0.1, C534 0.01, C524 0.1, C535 0.01, C525 0.1, C536 0.01, C470 0.1, C473 0.01, C472 0.1, C460 0.01, C471 0.1
C476 0.01, C477 0.1, C537 0.01, C526 0.1, C538 0.01, C527 0.1, C539 0.01, C482 0.1, C480 0.01, C481 0.1, C479 0.01, C478 0.1
C485 0.01, C486 0.1, C540 0.01, C529 0.1, C541 0.01, C530 0.1, C542 0.01, C491 0.1, C489 0.01, C490 0.1, C488 0.01, C487 0.1
C636 0.01, C570 0.1, C568 0.01, C569 0.1, C566 0.01, C567 0.1, C632 0.01, C595 0.1, C635 0.01, C634 0.1, C633 0.01, C616 0.1
C621 0.01, C574 0.1, C562 0.01, C573 0.1, C561 0.01, C572 0.1, C618 0.01, C585 0.1, C611 0.01, C619 0.1, C612 0.01, C620 0.1
C639 0.01, C578 0.1, C588 0.01, C577 0.1, C586 0.01, C587 0.1, C638 0.01, C596 0.1, C613 0.01, C624 0.1, C614 0.01, C625 0.1

BYPASS CAPACITORS INTENDED FOR SSRAMS (SHT 9)

VCC

C712 0.01, C725 0.1, C711 0.01, C724 0.1, C748 0.01, C735 0.1, C758 0.01, C754 0.1, C759 0.01, C755 0.1
C714 0.01, C727 0.1, C713 0.01, C726 0.1, C736 0.01, C737 0.1, C760 0.01, C749 0.1, C761 0.01, C750 0.1

BYPASS CAPACITORS INTENDED FOR PCI OPTION SLOTS (J4, J5, J7)

3.3

C202 0.01, C203 0.01, C204 0.01, C205 0.01, C206 0.01, C207 0.01, C4 0.01, C5 0.01, C6 0.01, C7 0.01, C8 0.01, C9 0.01
C33 0.01, C34 0.01, C35 0.01, C36 0.01, C37 0.01, C38 0.01, C217 0.01, C218 0.01, C219 0.01, C220 0.01, C221 0.01, C222 0.01
C262 0.01, C263 0.01, C264 0.01, C265 0.01, C266 0.01, C267 0.01, C43 0.01, C44 0.01, C45 0.01, C46 0.01, C47 0.01, C48 0.01

VCC

C209 0.01, C1 0.01, C208 0.01, C10 0.01
C32 0.01, C210 0.01, C39 0.01, C223 0.01
C261 0.01, C40 0.01, C268 0.01, C49 0.01

BYPASS CAPACITORS

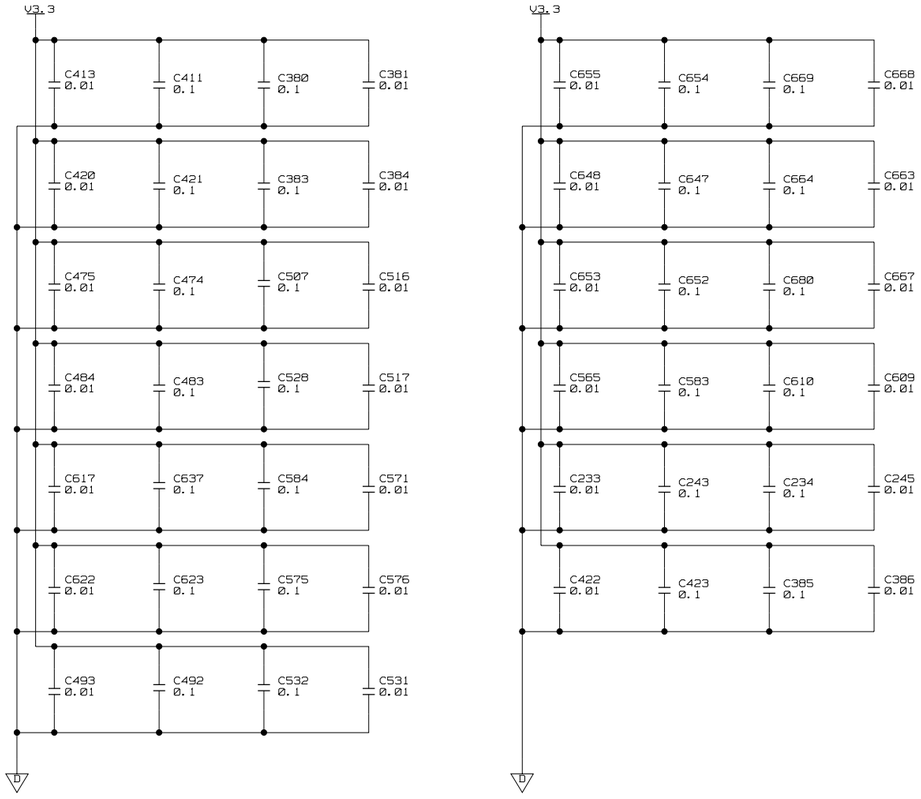
NOTES:
UNLESS OTHERWISE SPECIFIED
-ALL RESISTORS ARE IN OHMS, 0.1 W, 1%
-ALL CAPACITORS ARE IN MICROFARADS, 50V

DRAWING
LAST_MODIFIED=Fri Sep 24 14:10:03 1999

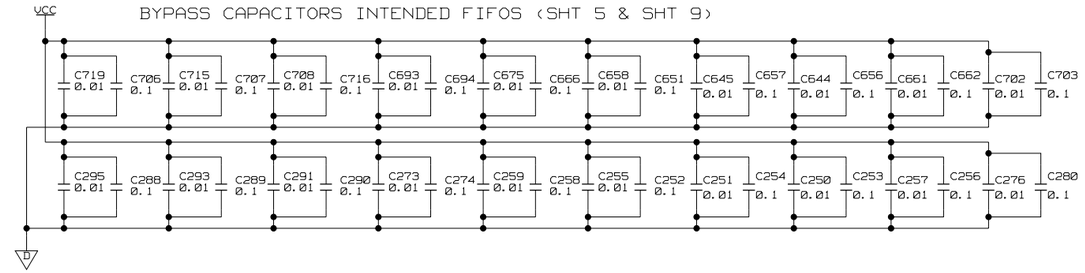
OEC MEDICAL SYSTEMS, INC.

SIZE	DWG NO.	REV
D	00-880921	A1
SCALE:	SHEET 19	

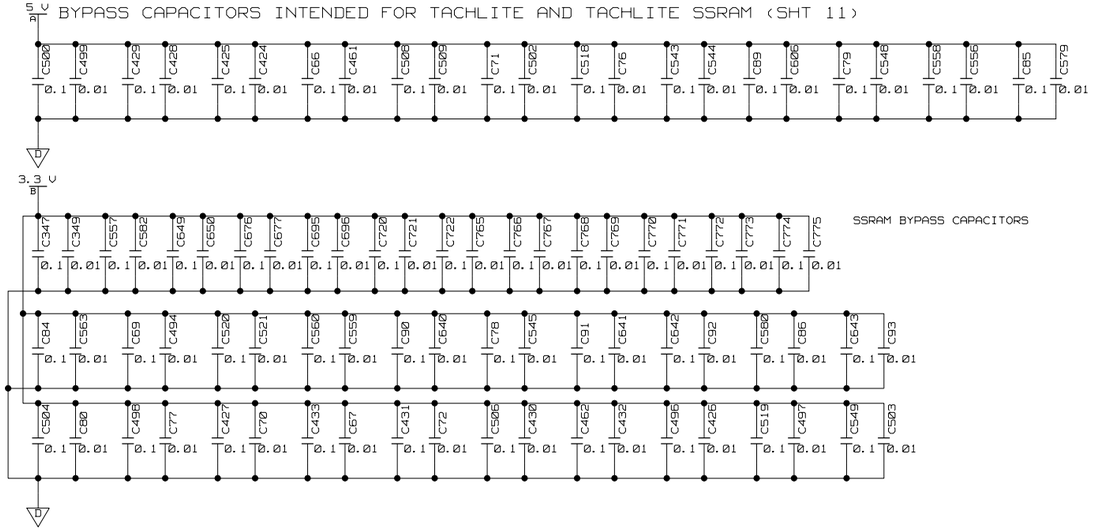
BYPASS CAPACITORS INTENDED FOR 74LCX16652's (SHEETS 5, 6, 7, & 8)



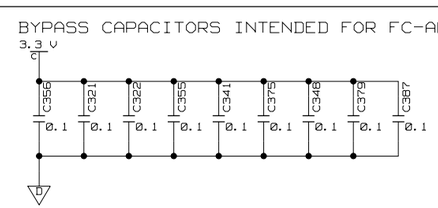
BYPASS CAPACITORS INTENDED FIFOS (SHT 5 & SHT 9)



BYPASS CAPACITORS INTENDED FOR TACHLITE AND TACHLITE SSRAM (SHT 11)



BYPASS CAPACITORS INTENDED FOR FC-AL TRANSCEIVER (SHT 11)



BYPASS CAPACITORS (CONTINUED)

NOTES:
UNLESS OTHERWISE SPECIFIED
-ALL RESISTORS ARE IN OHMS, 0.1 W, 1%
-ALL CAPACITORS ARE IN MICROFARADS, 50V

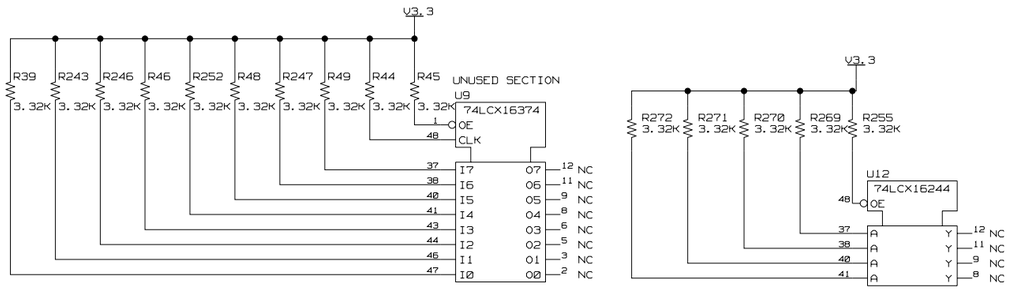
DRAWING
LAST_MODIFIED=Fri Sep 24 14:10:29 1999

OEC MEDICAL SYSTEMS, INC.

SIZE	DWG NO.	REV
D	00-880921	A1
SCALE:	SHEET 20	

05-017-9/93

SPARE COMPONENTS/SECTIONS



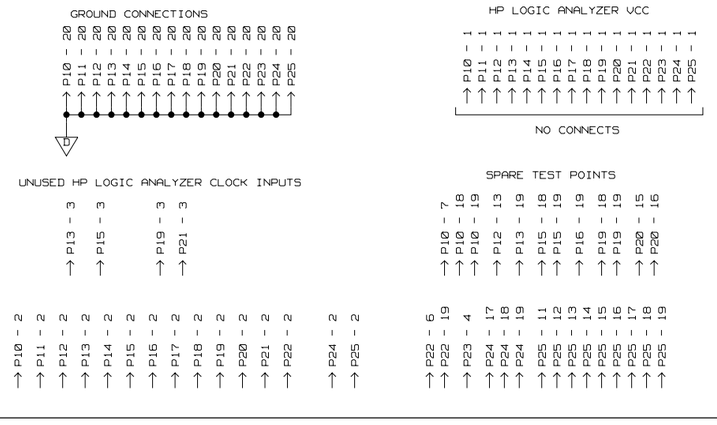
REFERENCE DESIGNATIONS	
HIGHEST	UNUSED
C775	C31, 105-199, 213, 246
DS7	
E7	
FL3	
R486	R267, 280, 285, 300, 373, 416, 417, 419, R421, 423, 425, 427, 428, 432, 433, 444
TP18	
U47	U44
L6	
Y1	

REF DESIGNATION	DEVICE	GND	V33	+5V
U2	EPC1	5		7, 8
U3	74LPT16652	4, 11, 18, 25, 32, 39, 46, 53	7, 22, 35, 50	
U19-21, 23-25, 32, 33, 35, 38-40	74LCX16652	4, 11, 18, 25, 32, 39, 46 53	7, 22, 35, 50	
U4, 9, 10	74LCX16374	4, 10, 15, 21, 28, 34, 39, 45	7, 18, 31, 42	
U5, 7, 12	74LCX16244	4, 10, 15, 21, 28, 34, 39, 45	7, 18, 31, 42	
U6	74FCT88915	1, 10, 13, 17, 20, 24		3, 8, 15, 22, 27
U42	EPM7064	10, 22, 30, 42		3, 15, 23, 35
U8, 43	FIFO_64X36X2	1, 8, 18, 24, 33, 40, 47, 55, 63, 67, 71, 79, 87, 94, 101, 110, 116, 126		11, 29, 36, 51, 59, 75, 83, 98, 105, 123
U13, 16-18	EPF10KTCI44	15, 16, 40, 50, 57, 58, 66, 84, 85, 103, 104, 127, 129, 139	5, 24, 45, 61, 71, 94, 115, 134	6, 25, 52, 53, 75, 93, 123
U14	NM96CS46	5		8
U26-28, 34, 36, 37	SDRAM_1MX16	4, 10, 26, 41, 47, 50	1, 7, 13, 25, 38, 44	
U30	PCI9050	9, 26, 40, 51, 65, 80, 104, 120, 147, 160		1, 10, 27, 41, 50, 66, 81, 103, 121, 146
U31	EPF10K20RC208	20, 21, 32, 33, 48, 49, 59, 72, 81, 82, 91, 123, 124, 129, 130, 151, 152, 171, 185, 188, 201	5, 22, 34, 42, 66, 84, 98, 110, 118, 138, 146, 165, 178, 194	6, 23, 35, 43, 76, 77, 106, 109, 117, 137, 145, 181
U46, 47	SSRAM64KX18	11, 16, 27, 37, 42		10, 17, 28, 36, 43
U45	DEC21152AB	1, 12, 19, 27, 34, 41, 50, 54, 58, 65, 71, 81, 86, 94, 103, 112, 119, 121, 128, 135, 143, 151, 157	8, 15, 23, 30, 40, 46, 56, 60, 75, 80, 90, 98, 108, 116, 120, 125, 131, 139, 147, 154, 160	
U1, 11, 22, 48	LT1086	1	2, 4	3
U15	VSC7125	1, 14, 15, 21, 25, 32, 33, 46, 51, 56, 58	5, 10, 18, 20, 23, 28, 29, 37, 42, 50, 53, 55, 57, 59, 60, 63	
U41	SSRAM_64KX36P	5, 10, 17, 21, 26, 40, 55, 60, 67, 71, 76, 90	4, 11, 15, 16, 20, 27, 41, 54, 61, 65, 66, 70, 77, 91	
U29	HPFC-5100B	A1, D4, D7, D8, D12, D13, D17, F19, H4, H17, J3, J9, J10, J11, J12, K9, K10, K11, K12, L9, L10, L11, L12, M9, M10, M11, M12, N4, N17, P18, T1, U4, U8, U13, U17, W6, Y12	B5, C12, D6, D11, D15, F4, F17, F20, J4, K4, L17, P4, R4, R17, R20, U6, U10, U15, V7, W12	L4, P2, R19, U7, U14, U18, V1, W7, W10, W18, Y2, Y13

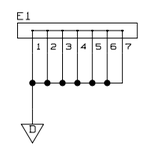
SPARE

TEST POINT INPUTS, CLOCKS AND GROUND

COMPATIBLE WITH HP LOGIC ANALYZER



PCB STIFFENER



NOTES:
UNLESS OTHERWISE SPECIFIED
-ALL RESISTORS ARE IN OHMS, Ø.1 W, 1%
-ALL CAPACITORS ARE IN MICROFARADS, 50V

DRAWING

LAST_MODIFIED=Fri Sep 24 14:10:58 1999

SPARE COMPONENTS AND REFERENCE DESIGNATORS

OEC MEDICAL SYSTEMS, INC.

SIZE	DWG NO.	REV
D	00-880921	A1
SCALE:		SHEET 21

05-017-9/93

*** Signal Cross-Reference ***
--- for the entire design --

+3.3VDC	10B7 10C8 3D8
+3.3V_SEN	10C8
+5VDC	10C8
+5VDC_SEN	10C8
ACQ	4C1 5C8 12A5
ACQN	4C1 5C8 12A4 13A5
ACTV	14A5 14D8
AD <31..0>	2A6 2B6 2A5
AD0	17A6
AD1	17A6
AD1_ <31..0>	2A1 3A8 9C8 11D8
AD2	17B7
AD3	17B7
AD4	17B7
AD5	17B7
AD6	17B7
AD7	17B7
AD8	17B7
AD9	17B7
AD10	17B7
AD11	17B7
AD12	17B7
AD13	17B7
AD14	17B7
AD15	17B7
AD16	17C7
AD17	17C7
AD18	17C7
AD19	17C7
AD20	17C7
AD21	17C7
AD22	17C7
AD23	17C7
AD24	17D6
AD25	17D6
AD26	17D6
AD27	17D6
AD28	17D6
AD29	17D6
AD30	17D6
AD31	17D6
ADD2	14C2 15C3 16C2
ADD3	14C2 15C3 16C2
ADD4	14C6 15C6 16C6
ADD5	14C6 15C6 16C6
ADD6	14C6 15C6 16C6
ADD7	14C6 15C6 16C6
ADD8	14C6 15C6 16C6
ADD9	14C6 15C6 16C6
ADD10	14C2 15C3 16C2
ADD11	14A4 15A4 16A4
ADD12	14A5 15A5 16A5
ADD13	14A5 15A5 16A5
ADD14	14D5 15D5 16D4
ADD15	14D4 15D4 16D4
ADD16	14A4 15A4 16A3
ADD17	14C2 15C3 16C2
ADD18	14D4 15D4 16D3
ADD19	14C2 15C3 16C2
ADD20	14D4 15D4 16D4
ADD21	14D4 15D4 16D4
ADDBX0	14C2 15C3 16C2
ADDBX1	14B6 15B6 16B6
ADDBX2	14C2 15C3 16C2
ADDBX3	14A4 15A4 16A4
ADDBX4	14C2 15C3 16C2
ADDBX5	14B2 15C3 16B2
ADDBX6	14C2 15C3 16C2
ADDBX7	14D4 15D4 16D4
ADDBX8	14B2 15B3 16B2
ADDBX9	14B2 15B3 16B2
ADDBX10	14C6 15C6 16C6
ADDBX11	14B2 15B3 16B2
ADDCS122	12B3
ADDCS123	12B3
ADDIN2	12A6
ADDIN3	12B7
ADDIN4	12B3
ADDIN5	12B7
ADSCN	18C4
ADSN	4B8 9D2 12B3 17D4 18C5
ADSPN	18B5
ADVN	9C4 18C4
AEBN	12C7
AFBN	12C7
ALE	17A5
BANKSEL0N	4B1 6D8 12A6
BANKSEL1N	4B1 7D8 12D6
BANKSEL2N	4B1 8D7 12A5
BCLK	4B8 9D2
BCLKO	17A5
BLASTN	17D4 18B5
BTCK	3D2 3D4 3D7 10A2 11A8 12D7 13C7 14C6 15C6 16C6
BTERMN	9D8 17D5
BTMS	3D3 3D6 3D8 10B2 11A8 12B7 13B7 14B6 15B6 16B6
BTRSTN	3D3 3D6 3D8 10A2 11A8 12B7
BYPASSEDN	11C4 12B3 4B4
BYPASS_D <6..1>	* 4B8 4A4
CINE_D <9..0>	4D1 5B8
CINE_DAT0	13B7
CINE_DAT1	13B3
CINE_DAT2	13A4
CINE_DAT3	13B3
CINE_DAT4	13B3
CINE_DAT5	13B3
CINE_DAT6	13B3
CINE_DAT7	13B7
CINE_DAT8	13B7
CINE_DAT9	13B7
CINE_HDRVN	4D8
CINE_PIXCLK	4D8
CINE_VDRVN	4D8
CLK0	2C1 9C8
CLK1	2C1 3C2 11C8
CLK2	2C1 3C7
CLK3	2C1 3C4
CLK4	2C1
CONFIGN	10D2 12B3 13B3 14B2 15B2 16B2
CONFLICTN	4C1 9C5 12A4 18B5
CONF_DONE	10D2 12C7 13C7 14C6 15C6 16C6
CONF_DONEN	13D5 10B5
CS0	17D5
CS0N	4C8 9D2 12B7
CS1	17D5
CS1N	4C8 9D2 12B3 18B5
CS2	17D5
CS2N	4B8 9D2 12C7 18B5
CS3	17D5
CTL_DIAG0N	4B2
CTL_DIAG1N	4B2
CTL_DIAG2N	4B2
CTL_DIAG3N	4C2
C_BE1N0	2D1 3B3 3B6 3B8 11C8 9C8
C_BE1N1	2D1 3B2 3B4 3B7 11C8 9C8
C_BE1N2	2D1 3C2 3C4 3C7 11C8 9C8
C_BE1N3	2D1 3C2 3C4 3C7 11C8 9C8
C_BEN <3..0>	2D6
C_BEN0	17B7
C_BEN1	17B7
C_BEN2	17C7
C_BEN3	17D6
DAT0	12C7
DAT1	12A6
DAT2	12C7
DAT3	12D5
DAT4	12A5
DAT5	12D6
DAT6	12A6
DAT7	12A6
DAT8	12C7
DAT9	12B7
DAT10	12B7
DAT11	12D6
DAT12	12D6
DAT13	12C7
DAT14	12B3
DAT15	12A5
DATA0	10D2 12D3 13C3 14C2 15C2 16C2
DATA_VALID	14C6 14D8
DCAB	14D4 14D8
DCLK	10D2 12C3 13C3 14C2 15C2 16C2
DEVSEL1N	2D1 3B2 3B4 3B7 11B8 9C8
DISKSTAT1N	12C7
DISKSTAT2N	12C3
DISKSTAT3N	12B3
DISKSTAT4N	12C3
DISKSTAT5N	12C3
DISKSTAT6N	12B7
DISK_STAT <14..1>	4B4
DRAMADSN	4C1 12B7 6D8 7D8 8D8
EECS	17D5
EEDI	17D5
EEDO	17D5
EESK	17D5
ENABLE2N	12D4
ENABLE4N	12D5
ENABLE_2 *	4A5 10C5
ENABLE_4 *	4A5 10C5
FAIL_D <6..1> *	4A8 4A5
FBADS	4C1 12D4 9A8
FC_TDO	11A8 10B5
FPGA0_CEON	12C7 13C3
FPGA0_TDI	10B2 12C3
FPGA0_TDO	12C7 13C3
FPGA1_CEON	13C7 14C2
FPGA1_TDO	13C7 14C2
FPGA2_CEON	14C6 15C2
FPGA2_TDO	14C6 15C2
FPGA3_CEON	15C6 16C2
FPGA3_TDO	15C6 16C2
FPGA4_CEON	16C6
FPGA4_TDO	16C6 11A8
FRAME0ADDR <11..0>	6B4
FRAME0DATA <31..0>	6A4
FRAME1ADDR <11..0>	7B4
FRAME1DATA <31..0>	7A4
FRAME1N	2D1 3B3 3B6 3B8 11B8 9C8
FRAME2ADDR <11..0>	8B4
FRAME2DATA <31..0>	8A4
GNT1N_0	2C1
GNT1N_1	2C1 3C3 11C8
GNT1N_2	2C1 3C8
GNT1N_3	2C1 3C6
GNTN	2C6
HEARTBEAT	11A8 10C5
HSYNCN	12C3
HSYNCN_OUT	12C3
IBADD <21..2>	9A1 6C8 7C8 8C8
IDLE	14B2 14D8
IDSEL0	9C7
IDSEL1	3C3 3D1 11B8
IDSEL2	3C8
IDSEL3	3C5
INIT	14A5 14D8
INTA	17A6
INTAN	2A1 3C2 3D4 3D8 9C8
INTBN	2A1 3C7 3D3 3D6 11B8
INTCN	2A1 3C4 3D2 3D8
INTDN	2A1 3D3 3D6 3D7
IRDY1N	2D1 3B2 3B4 3B7 11B8 9C8
LA <23..2>	9A1 4A8
LA2	17B4
LA3	17B4
LA4	17B4
LA5	17B4
LA6	17B4
LA7	17B4
LA8	17B4
LA9	17C4
LA10	17C4
LA11	17C4
LA12	17C4
LA13	17C4
LA14	17C4
LA15	17C4
LA16	17C4
LA17	17C4
LA18	17C4
LA19	17C4
LA20	17C4
LA21	17C4
LA22	17C4
LA23	17C4
LA24	17C4
LA25	17C4
LA26	17C4
LA27	17D4
LAD <31..0>	9A1 4A8
LAD0	17B4
LAD1	17B4
LAD2	17B4
LAD3	17B4
LAD4	17B4
LAD5	17B4
LAD6	17B4
LAD7	17B4
LAD8	17B4
LAD9	17B4
LAD10	17A4
LAD11	17A4
LAD12	17A4
LAD13	17A4

LAD14	17A4
LAD15	17A4
LAD16	17A5
LAD17	17A5
LAD18	17A5
LAD19	17A5
LAD20	17A5
LAD21	17A5
LAD22	17A5
LAD23	17A5
LAD24	17A5
LAD25	17A5
LAD26	17A5
LAD27	17A5
LAD28	17A5
LAD29	17A5
LAD30	17A5
LAD31	17A6
LBE0	17A6
LBE1	17A6
LBE2	17A6
LBE3	17A6
LCLK	17D5
LHOLD	17D5
LHOLDA	17D5
LINTI1	17D5
LINTI1N	4C1 9D8 12B7 10C5
LINTI2	17D5
LINTI2N	4C1 9D8 12B7
LLOCK	17D5
LOCK1N	2D1 3B2 3B4 3B7 9C8
LRCSTAT1N	12C7
LRCSTAT2N	12C7
LRCSTAT3N	12C7
LRCSTAT4N	12B7
LRCSTAT5N	12C7
LRCSTAT6N	12D5
LRDYIN	17D5
LRDYN	9D8 18B4
LRESET	17D5
LWN	18B4 9C4
LW_RN	4B8 9D2 17D4 18C5 12D5
MODE	17A5
MPAR <3..0>	11A4
MRS	14C2 14D8
PAR1	2D1 3B3 3B6 3B8 11C8 9C8
PCFIFOD <31..0>	9A1 6A8 7A8 8A8
PCIAEAN	9C3 4B8
PCIAEBN	9C1 14D4 15D4 16D3 4B8 6D8 7D8 8D7
PCIAFAN	9C3 4B8
PCIAFBN	9C1 14A5 15A5 16A4 4B8 6D8 7D8 8D7
PCIBCLK	12A5 18C5
PCIEFAN	9C3 4B8
PCIEFBN	9C1 14D4 15D4 16D4 4B8 6D8 7D8 8D7
PCIFCSBN	6D1 7D1 8D1 9C1
PCIFCSN	14B6 15B6 16B6
PCIFEN	14A4 15A4 16A4
PCIFENB	6D1 7D1 8D1 9C1
PCIFFAN	9C3 4B8
PCIFFBN	9C1 4B8
PCIFIFOEN	9D3
PCIFIFORSTN	9D2 9D3 12C3 14B6 15B6 16B6 4B8 6D8 7D8 8D8
PCIFW_RBN	6D1 7D1 8D1 9C1
PCIFW_RN	14B2 15B3 16B2
PCIRD	14B6 14D8
PCIWR	14B6 14D8
PCI_+3.3V	2C7 2C8
PCI_+5V	2B8 2C5 2D6 2D7 2D8
PCI_+5V_IO	2B7 2C8 2D7

PCI_+12V	2D7 3D8
PCI_-12V	2D7 3D8
PCI_PPUN0	4B1 6D8 12D5
PCI_PPUN1	4B1 7D8 12C3
PCI_PPUN2	4B1 8D7 12D5
PERR1N	2C1 3B2 3B4 3B7 11B8 9C8
PIN001N	18C5
PIN002	18C4
PIXCLK13	4C4
PIXCLK15	4D7 5D7
PIXDVLD	4C1 12D4 13D5 5C8
PIX_CLK <6..0>	4D1 9D1 5D8 6B8 7B8 8B8
PIX_CLK0	5D7
PIX_CLK2	5D7
PIX_CLK3	6B7
PIX_CLK4	7B7
PIX_CLK5	8B7
PIX_CLK6	9D2
PMEN	2C6 3C3 3C6 3C8
POWERUP	14A5
PPDATA0	13A4
PPDATA1	13D4
PPDATA2	13B3
PPDATA3	13D4
PPDATA4	13A4
PPDATA5	13D4
PPDATA6	13C3
PPDATA7	13B3
PPDATA8	13B3
PPDATA9	13B3
PPDATA10	13B3
PPDATA11	13B7
PPDATA12	13C3
PPDATA13	13B7
PPDATA14	13B7
PPDATA15	13A5
PPDATA16	13B7
PPDATA17	13C7
PPDATA18	13C7
PPDATA19	13B7
PPDATA20	13C3
PPDATA21	13C3
PPDATA22	13C3
PPDATA23	13C3
PPDATA24	13C3
PPDATA25	13C7
PPDATA26	13C7
PPDATA27	13C3
PPDATA28	13C3
PPDATA29	13C3
PPDATA30	13B3
PPDATA31	13B7
PPFFBN	5C2
PPFIFOD <31..0>	5B1 6A8 7A8 8A8
PPUAEBN	5C1 14D4 15D5 16D4 6D8 7D8 8D7
PPUAFBN	5C1 14D5 15D5 16D4 6D8 7D8 8D7
PPUEFBN	5C1 14D4 15D4 16D3 6D8 7D8 8D7
PPUFCSBN	6D1 7D1 8D1 5D1
PPUFCSN	14D5 15D5 16D5
PPUFEN	14C6 15C6 16C6
PPUFENB	6D1 7D1 8D1 5C1
PPUFIFORSTN	5D1 12D6 14B6 15B6 16B6 4C8 6D8 7D8 8D8
PPUFW_RBN	6D1 7D1 8D1 5C1
PPUFW_RN	14A5 15A5 16A5
PPURD	14B6 14D8
PPUWR	14D5 14D8
PP_LASTN	4C1 12C3 14D4 15D4 16D4 5C8 6D8 7D8 8D7 13D4

RDN	4B8 9D2 12D4 17D4 18C5
RD_WRN0	4A1 6D8 12A6
RD_WRN1	4A1 7D8 12C3
RD_WRN2	4B1 8D7 12A5
READ	14B6 14D8
REFR	14C6 14D8
REQ1N_0	2C1
REQ1N_1	2C1 3C2 11C8
REQ1N_2	2C1 3C7
REQ1N_3	2C1 3C4
REQN	2C6
RESETN	4C8 9D2
RESETPN	4C6 5D8 6D8 7D8 8D7
RST1N	2C1 3C3 3C6 3C8 9C8 11B8
RTRVN	4C1 5C8 12D5 13D4
SERR1N	2C1 3B2 3B4 3B7 11B8 9C8
SLFR	14C6 14D8
SLFREF	14B6 14D8
SSMOEN	18B4
STARTACQN	4C1 12C3 13C7 5D8
STARTRTRVN	4C1 12C3 5C8 13D5
STATUSN	10D2 12B7 13B7 14B6 15B6 16B6
STOP1N	2D1 3B3 3B6 3B8 11B8 9C8
TACHADDR <17..1>	11A5
TACHDATA <31..0>	11A5
TACHRX <9..0>	11C3
TACHTX <9..0>	11C3
TCK	2A5 10A5
TDI	2A5 10B5
TDO	2A5 10B5
TEST	17B4
TMS	2A5 10B5
TRDY1N	2D1 3B3 3B6 3B8 11B8 9C8
TRSTN	2A5 10A5
TXPCOEAB0	4A1 6C8 12D4
TXPCOEAB1	4A1 7C8 12A4
TXPCOEAB2	4A1 8C8 12D4
TXPCOEBA0N	4A1 6C8 12A4
TXPCOEBA1N	4A1 7C8 12D4
TXPCOEBA2N	4A1 8C8 12D4
TXPPOEAB0	4A1 6B8 12D6
TXPPOEAB1	4A1 7B8 12D6
TXPPOEAB2	4A1 8B8 12B3
TXPPOEBA0N	4A1 6B8 12B7
TXPPOEBA1N	4A1 7B8 12A6
TXPPOEBA2N	4A1 8B8 12A5
UWN	18B4 9C4
VSYNCN	12C3
VSYNCN_OUT	12C3
WAIT0	17D5
WAKEUP	14B2 14D8
WRIT	14D4 14D8
WRN	4B8 9D2 12B3 17D4 18C5
WR_RFN	9D3

*** Unit Cross-Reference ***
--- for the entire design --

C1	CERSMT_0805	19A6
C2	CERSMT_0805	3C7
C3	CERSMT_0805	3C7
C4	CERSMT_0805	19A7
C5	CERSMT_0805	19A7
C6	CERSMT_0805	19A7
C7	CERSMT_0805	19A7
C8	CERSMT_0805	19A6
C9	CERSMT_0805	19A6
C10	CERSMT_0805	19A5
C11	TASMT_7343	10C6
C12	CERSMT_0805	4C7
C13	CERSMT_0805	5B8
C14	CERSMT_0805	5B8
C15	CERSMT_0805	5B7
C16	CERSMT_0805	5B7
C17	CERSMT_0805	4C7
C18	TASMT_6032	10C7
C19	TASMT_7343	10B6
C20	TASMT_7343	10C7
C21	TASMT_7343	10B6
C22	CERSMT_0805	19D5
C23	CERSMT_0805	5B7
C24	CERSMT_0805	5B7
C25	CERSMT_1206	4D5
C26	CERSMT_0805	5B7
C27	CERSMT_0805	5B7
C28	CERSMT_0805	5B7
C29	CERSMT_0805	5B7
C30	CERSMT_0805	19D4
C32	CERSMT_0805	19A6
C33	CERSMT_0805	19A8
C34	CERSMT_0805	19A8
C35	CERSMT_0805	19A8
C36	CERSMT_0805	19A8
C37	CERSMT_0805	19A7
C38	CERSMT_0805	19A7
C39	CERSMT_0805	19A6
C40	CERSMT_0805	19A6
C41	CERSMT_0805	3C2
C42	CERSMT_0805	3C2
C43	CERSMT_0805	19A7
C44	CERSMT_0805	19A7
C45	CERSMT_0805	19A7
C46	CERSMT_0805	19A7
C47	CERSMT_0805	19A6
C48	CERSMT_0805	19A6
C49	CERSMT_0805	19A5
C50	CERSMT_0805	4D7
C51	TASMT_7343	11D1
C52	TASMT_6032	11D1
C53	CERSMT_0603	11C1
C54	CERSMT_0603	11C1
C55	CERSMT_0603	11C1
C56	CERSMT_0603	11C1
C57	CERSMT_0805	11C1
C58	CERSMT_0603	11C1
C59	CERSMT_0805	11C2
C60	CERSMT_0805	11C2
C61	TASMT_7343	10C6
C62	CERSMT_0805	13C8
C63	CERSMT_0805	5D4
C64	CERSMT_0805	11C2
C65	CERSMT_0805	12D8
C66	CERSMT_0805	20C3
C67	CERSMT_0805	20B3
C68	CERSMT_1206	12D1
C69	CERSMT_0805	20B4
C70	CERSMT_0805	20B4
C71	CERSMT_0805	20C3
C72	CERSMT_0805	20B3
C73	CERSMT_0805	12C8
C74	CERSMT_0805	12C1
C75	TASMT_6032	11D1
C76	CERSMT_0805	20C2
C77	CERSMT_0805	20B4
C78	CERSMT_0805	20B3
C79	CERSMT_0805	20C2
C80	CERSMT_0805	20B4
C81	CERSMT_0805	12B8
C82	CERSMT_1206	12B1
C83	TASMT_7343	11D1
C84	CERSMT_0805	20B4
C85	CERSMT_0805	20C1
C86	CERSMT_0805	20B2
C87	CERSMT_0805	12A8
C88	CERSMT_0805	12B1
C89	CERSMT_0805	20C2
C90	CERSMT_0805	20B3
C91	CERSMT_0805	20B3
C92	CERSMT_0805	20B2
C93	CERSMT_0805	20B2
C94	TASMT_7343	10B6
C95	TASMT_7343	10C6
C96	CERSMT_0805	9C2
C97	CERSMT_0805	6C7
C98	CERSMT_0805	4C7
C99	TASMT_7343	2B8
C100	CERSMT_1206	2B7
C101	CERSMT_1206	2D8
C102	TASMT_6032	2B8
C103	TASMT_7343	2B7
C104	CERSMT_1206	2D7
C105	CERSMT_0805	11D3
C200	CERSMT_1206	10B6
C201	CERSMT_0805	10B6
C202	CERSMT_0805	19A8
C203	CERSMT_0805	19A8
C204	CERSMT_0805	19A8
C205	CERSMT_0805	19A8
C206	CERSMT_0805	19A7
C207	CERSMT_0805	19A7
C208	CERSMT_0805	19A6
C209	CERSMT_0805	19A6
C210	CERSMT_0805	19A6
C211	CERSMT_0805	3C4
C212	CERSMT_0805	3C4
C214	CERSMT_0805	19D5
C215	CERSMT_1206	19D5
C216	CERSMT_0805	10C6
C217	CERSMT_0805	19A7
C218	CERSMT_0805	19A7
C219	CERSMT_0805	19A7
C220	CERSMT_0805	19A7
C221	CERSMT_0805	19A6
C222	CERSMT_0805	19A6
C223	CERSMT_0805	19A5
C224	CERSMT_1206	10C7
C225	CERSMT_1206	19D5
C226	CERSMT_0805	19D3
C227	CERSMT_1206	19D3
C228	CERSMT_0805	19D3
C229	CERSMT_1206	19D3
C230	CERSMT_1206	19D5
C231	CERSMT_0805	19D3
C232	CERSMT_1206	19D3
C233	CERSMT_0805	20C6
C234	CERSMT_1206	20C5
C235	CERSMT_0805	19D5
C236	CERSMT_0805	5B7
C237	CERSMT_1206	19D2
C238	CERSMT_0805	19D2
C239	CERSMT_1206	19D2
C240	CERSMT_0805	19D2
C241	CERSMT_1206	19D2
C242	CERSMT_0805	19D2
C243	CERSMT_1206	20C6
C244	CERSMT_1206	19D4
C245	CERSMT_0805	20C5
C247	CERSMT_0805	5B6
C248	CERSMT_0805	19D4
C249	CERSMT_1206	19D4
C250	CERSMT_0805	20D2
C251	CERSMT_0805	20D2
C252	CERSMT_1206	20D2
C253	CERSMT_1206	20D2
C254	CERSMT_1206	20D2
C255	CERSMT_0805	20D2
C256	CERSMT_1206	20D1
C257	CERSMT_0805	20D2
C258	CERSMT_1206	20D3
C259	CERSMT_0805	20D3
C260	CERSMT_0805	19C3
C261	CERSMT_0805	19A6
C262	CERSMT_0805	19A8
C263	CERSMT_0805	19A8
C264	CERSMT_0805	19A8
C265	CERSMT_0805	19A8
C266	CERSMT_0805	19A7
C267	CERSMT_0805	19A7
C268	CERSMT_0805	19A6
C269	CERSMT_1206	19C3
C270	CERSMT_0805	19C3
C271	CERSMT_1206	19C3
C272	CERSMT_1206	13D4
C273	CERSMT_0805	20D3
C274	CERSMT_1206	20D3
C275	CERSMT_1206	19C2
C276	CERSMT_0805	20D1
C277	CERSMT_0805	19C2
C278	CERSMT_0805	13D5
C279	CERSMT_0805	13C2
C280	CERSMT_1206	20D1
C281	CERSMT_1206	19C2
C282	CERSMT_0805	19C2
C283	CERSMT_0805	19C3
C284	CERSMT_1206	19C3
C285	CERSMT_1206	13D5
C286	CERSMT_1206	13D5
C287	CERSMT_0805	13D4
C288	CERSMT_1206	20D4
C289	CERSMT_1206	20D4
C290	CERSMT_1206	20D3
C291	CERSMT_0805	20D3
C292	CERSMT_1206	13C2
C293	CERSMT_0805	20D4
C294	CERSMT_0805	13D5
C295	CERSMT_0805	20D4
C296	CERSMT_1206	16D4
C297	CERSMT_1206	13C8
C298	CERSMT_1206	13C7
C299	CERSMT_0805	14D4
C300	CERSMT_0805	14B2
C301	CERSMT_0805	14C7
C302	CERSMT_0805	14C2
C303	CERSMT_0805	15D4
C304	CERSMT_0805	15A4
C305	CERSMT_0805	15C2
C306	CERSMT_0805	15B2
C307	CERSMT_0805	16D4
C308	CERSMT_0805	16C2
C309	CERSMT_0805	16C2
C310	CERSMT_0805	16B2
C311	CERSMT_0805	13C8
C312	CERSMT_1206	19C2
C313	CERSMT_0805	13C2
C314	CERSMT_0805	19C2
C315	CERSMT_1206	13C2
C316	CERSMT_1206	14C1
C317	CERSMT_0805	14C2
C318	CERSMT_1206	15C1
C319	CERSMT_0805	15C7
C320	CERSMT_0805	16A4
C321	CERSMT_0805	20A4
C322	CERSMT_0805	20A4
C323	CERSMT_0805	13B8
C324	CERSMT_0805	13B8
C325	CERSMT_1206	14C7
C326	CERSMT_1206	14C1
C327	CERSMT_1206	14D4
C328	CERSMT_1206	14B1
C329	CERSMT_1206	14A4
C330	CERSMT_1206	15D4
C331	CERSMT_1206	15D4
C332	CERSMT_1206	15A5
C333	CERSMT_1206	15B1
C334	CERSMT_1206	15A4
C335	CERSMT_1206	16C1
C336	CERSMT_1206	16C1
C337	CERSMT_1206	16A4
C338	CERSMT_1206	16B1
C339	CERSMT_1206	16A4
C340	CERSMT_0805	11C3
C341	CERSMT_0805	20A4
C342	CERSMT_1206	13B2
C343	CERSMT_0805	13B2
C344	CERSMT_0805	14A4
C345	CERSMT_0805	15A4
C346	CERSMT_0805	16A4
C347	CERSMT_0805	20C4
C348	CERSMT_0805	20A3
C349	CERSMT_0603	20C4
C350	CERSMT_1206	11D3
C351	CERSMT_1206	13A5
C352	CERSMT_1206	13A5
C353	CERSMT_1206	13A4
C354	CERSMT_1206	13A4
C355	CERSMT_0805	20A4
C356	CERSMT_0805	20A4
C357	CERSMT_1206	13B8
C358	CERSMT_1206	13B7
C359	CERSMT_0805	13A5
C360	CERSMT_0805	14A5
C361	CERSMT_0805	14A4
C362	CERSMT_0805	15A5
C363	CERSMT_0805	16D4
C364	CERSMT_0805	16B7
C365	CERSMT_0805	14D4
C366	CERSMT_1206	14D4
C367	CERSMT_1206	14A4
C368	CERSMT_0805	15D4
C369	CERSMT_1206	15B7
C370	CERSMT_1206	15A4
C371	CERSMT_0805	15C2
C372	CERSMT_1206	16D4
C373	CERSMT_0805	16A5
C374	CERSMT_1206	16A5
C375	CERSMT_0805	20A4
C376	CERSMT_1206	14A5
C377	CERSMT_1206	15C1
C378	CERSMT_1206	16A4
C379	CERSMT_0805	20A3
C380	CERSMT_1206	20D7
C381	CERSMT_0805	20D7
C382	CERSMT_0805	14A4
C383	CERSMT_1206	20D7
C384	CERSMT_0805	20D7
C385	CERSMT_1206	20B5
C386	CERSMT_0805	20B5

OEC MEDICAL SYSTEMS, INC.

SIZE	DWG NO.	REV
D	00-880921	A1
SCALE:		SHEET 24

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C387	CERSMT_0805	20A3
C388	CERSMT_0805	13A5
C389	CERSMT_0805	13A5
C390	CERSMT_1206	13A4
C391	CERSMT_0805	13A4
C392	CERSMT_0805	13A4
C393	CERSMT_0805	15A5
C394	CERSMT_1206	16D5
C395	CERSMT_0805	11C3
C396	CERSMT_1206	14D5
C397	CERSMT_0805	14D5
C398	CERSMT_1206	15C7
C399	CERSMT_0805	15D5
C400	CERSMT_0805	16D5
C401	CERSMT_1206	14C7
C402	CERSMT_1206	14A5
C403	CERSMT_1206	14B7
C404	CERSMT_1206	15C7
C405	CERSMT_1206	15B7
C406	CERSMT_1206	15A5
C407	CERSMT_1206	16C7
C408	CERSMT_1206	16A5
C409	CERSMT_1206	16B7
C410	CERSMT_0805	16A5
C411	CERSMT_1206	20D7
C412	CERSMT_1206	14A4
C413	CERSMT_0805	20D8
C414	CERSMT_1206	15A4
C415	CERSMT_0603	11D2
C416	CERSMT_0805	12D6
C417	CERSMT_0805	12D5
C418	CERSMT_0805	12D5
C419	CERSMT_0805	12D4
C420	CERSMT_0805	20D8
C421	CERSMT_1206	20D7
C422	CERSMT_0805	20B6
C423	CERSMT_1206	20B6
C424	CERSMT_0805	20C4
C425	CERSMT_0805	20C4
C426	CERSMT_0805	20B2
C427	CERSMT_0805	20B4
C428	CERSMT_0805	20C4
C429	CERSMT_0805	20C4
C430	CERSMT_0805	20B3
C431	CERSMT_0805	20B3
C432	CERSMT_0805	20B2
C433	CERSMT_0805	20B3
C434	CERSMT_0805	14B7
C435	CERSMT_0805	14C7
C436	CERSMT_0805	14A5
C437	CERSMT_0805	14B7
C438	CERSMT_0805	15A4
C439	CERSMT_0805	15B7
C440	CERSMT_0805	15B7
C441	CERSMT_0805	15C7
C442	CERSMT_0805	16C7
C443	CERSMT_0805	16A4
C444	CERSMT_0805	16B7
C445	CERSMT_0805	16C7
C446	CERSMT_1206	16B7
C447	CERSMT_0805	17D7
C448	CERSMT_0805	17D4
C449	CERSMT_1206	14B7
C450	CERSMT_1206	15D5
C451	CERSMT_1206	16C7
C452	CERSMT_0603	11D4
C453	CERSMT_1206	17D7
C454	CERSMT_0805	17D5
C455	CERSMT_1206	17D3
C456	CERSMT_1206	12D5
C457	CERSMT_1206	12D5
C458	CERSMT_1206	12D5
C459	CERSMT_1206	12D4
C460	CERSMT_0805	19C6
C461	CERSMT_0805	20C3
C462	CERSMT_0805	20B3
C463	CERSMT_1206	17D5
C464	CERSMT_1206	12D7
C465	CERSMT_0805	12D8
C466	CERSMT_1206	12D7
C467	CERSMT_1206	12A2
C468	CERSMT_0805	12A2
C469	CERSMT_0805	12D1
C470	CERSMT_1206	19C7
C471	CERSMT_1206	19C6
C472	CERSMT_1206	19C7
C473	CERSMT_0805	19C7
C474	CERSMT_1206	20C7
C475	CERSMT_0805	20C8
C476	CERSMT_0805	19C8
C477	CERSMT_1206	19C8
C478	CERSMT_1206	19C6
C479	CERSMT_0805	19C6
C480	CERSMT_0805	19C7
C481	CERSMT_1206	19C7
C482	CERSMT_1206	19C7
C483	CERSMT_1206	20C7
C484	CERSMT_0805	20C8
C485	CERSMT_0805	19C8
C486	CERSMT_1206	19C8
C487	CERSMT_1206	19C6
C488	CERSMT_0805	19C6
C489	CERSMT_0805	19C7
C490	CERSMT_1206	19C7
C491	CERSMT_1206	19C7
C492	CERSMT_1206	20B7
C493	CERSMT_0805	20B8
C494	CERSMT_0805	20B4
C495	CERSMT_0805	17C7
C496	CERSMT_0805	20B2
C497	CERSMT_0805	20B2
C498	CERSMT_0805	20B4
C499	CERSMT_0805	20C4
C500	CERSMT_0805	20C4
C501	CERSMT_1206	17C7
C502	CERSMT_0805	20C3
C503	CERSMT_0805	20B2
C504	CERSMT_0805	20B4
C505	CERSMT_1206	19C8
C506	CERSMT_0805	20B3
C507	CERSMT_1206	20C7
C508	CERSMT_0805	20C3
C509	CERSMT_0805	20C3
C510	CERSMT_0805	17C3
C511	CERSMT_1206	12C7
C512	CERSMT_0805	12C8
C513	CERSMT_1206	12C7
C514	CERSMT_1206	12C1
C515	CERSMT_1206	12C1
C516	CERSMT_0805	20C7
C517	CERSMT_0805	20C7
C518	CERSMT_0805	20C3
C519	CERSMT_0805	20B2
C520	CERSMT_0805	20B4
C521	CERSMT_0805	20B4
C522	CERSMT_1206	17C3
C523	CERSMT_0805	12C1
C524	CERSMT_1206	19C8
C525	CERSMT_1206	19C7
C526	CERSMT_1206	19C8
C527	CERSMT_1206	19C7
C528	CERSMT_1206	20C7
C529	CERSMT_1206	19C8
C530	CERSMT_1206	19C7
C531	CERSMT_0805	20B7
C532	CERSMT_1206	20B7
C533	CERSMT_0805	19C8
C534	CERSMT_0805	19C8
C535	CERSMT_0805	19C7
C536	CERSMT_0805	19C7
C537	CERSMT_0805	19C8
C538	CERSMT_0805	19C7
C539	CERSMT_0805	19C7
C540	CERSMT_0805	19C8
C541	CERSMT_0805	19C7
C542	CERSMT_0805	19C7
C543	CERSMT_0805	20C2
C544	CERSMT_0805	20C2
C545	CERSMT_0805	20B3
C546	CERSMT_1206	12C1
C547	CERSMT_0805	12C1
C548	CERSMT_0805	20C2
C549	CERSMT_0805	20B2
C550	CERSMT_1206	17B7
C551	CERSMT_0805	12B1
C552	CERSMT_0805	17B7
C553	CERSMT_1206	12B7
C554	CERSMT_1206	12B7
C555	CERSMT_0805	12B1
C556	CERSMT_0805	20C1
C557	CERSMT_0805	20C4
C558	CERSMT_0805	20C1
C559	CERSMT_0805	20B3
C560	CERSMT_0805	20B3
C561	CERSMT_0805	19B7
C562	CERSMT_0805	19B8
C563	CERSMT_0805	20B4
C564	CERSMT_1206	12B1
C565	CERSMT_0805	20C6
C566	CERSMT_0805	19B7
C567	CERSMT_1206	19B7
C568	CERSMT_0805	19B8
C569	CERSMT_1206	19B8
C570	CERSMT_1206	19B8
C571	CERSMT_0805	20C7
C572	CERSMT_1206	19B7
C573	CERSMT_1206	19B8
C574	CERSMT_1206	19B8
C575	CERSMT_1206	20B7
C576	CERSMT_0805	20B7
C577	CERSMT_1206	19B8
C578	CERSMT_1206	19B8
C579	CERSMT_0805	20C1
C580	CERSMT_0805	20B2
C581	CERSMT_1206	12B1
C582	CERSMT_0603	20C4
C583	CERSMT_1206	20C6
C584	CERSMT_1206	20C7
C585	CERSMT_1206	19B7
C586	CERSMT_0805	19B7
C587	CERSMT_1206	19B7
C588	CERSMT_0805	19B8
C589	CERSMT_0805	12B8
C590	CERSMT_1206	12B7
C591	CERSMT_1206	12A6
C592	CERSMT_1206	12A5
C593	CERSMT_1206	12A5
C594	CERSMT_0805	12A2
C595	CERSMT_1206	19B7
C596	CERSMT_1206	19B7
C597	CERSMT_1206	17A6
C598	CERSMT_0805	17A6
C599	CERSMT_1206	17A5
C600	CERSMT_1206	17A5
C601	CERSMT_0805	17A5
C602	CERSMT_1206	17A3
C603	CERSMT_1206	12A8
C604	CERSMT_0805	12B8
C605	CERSMT_0805	12A5
C606	CERSMT_0805	20C2
C607	CERSMT_0805	17A6
C608	CERSMT_1206	12A2
C609	CERSMT_0805	20C5
C610	CERSMT_1206	20C5
C611	CERSMT_0805	19B7
C612	CERSMT_0805	19B6
C613	CERSMT_0805	19B7
C614	CERSMT_0805	19B6
C615	CERSMT_0805	17A4
C616	CERSMT_1206	19B6
C617	CERSMT_0805	20C8
C618	CERSMT_0805	19B7
C619	CERSMT_1206	19B7
C620	CERSMT_1206	19B6
C621	CERSMT_0805	19B8
C622	CERSMT_0805	20B8
C623	CERSMT_1206	20B7
C624	CERSMT_1206	19B7
C625	CERSMT_1206	19B6
C626	CERSMT_0805	12A6
C627	CERSMT_0805	12A6
C628	CERSMT_1206	12A5
C629	CERSMT_0805	12A5
C630	CERSMT_1206	12A4
C631	CERSMT_0805	12A4
C632	CERSMT_0805	19B7
C633	CERSMT_0805	19B6
C634	CERSMT_1206	19B7
C635	CERSMT_0805	19B7
C636	CERSMT_0805	19B8
C637	CERSMT_1206	20C7
C638	CERSMT_0805	19B7
C639	CERSMT_0805	19B8
C640	CERSMT_0805	20B3
C641	CERSMT_0805	20B2
C642	CERSMT_0805	20B2
C643	CERSMT_0805	20B2
C644	CERSMT_0805	20D2
C645	CERSMT_0805	20D2
C646	CERSMT_0805	18B3
C647	CERSMT_1206	20D6
C648	CERSMT_0805	20D6
C649	CERSMT_0805	20C4
C650	CERSMT_0603	20C4
C651	CERSMT_1206	20D2
C652	CERSMT_1206	20C6
C653	CERSMT_0805	20C6
C654	CERSMT_1206	20D6
C655	CERSMT_0805	20D6
C656	CERSMT_1206	20D2
C657	CERSMT_1206	20D2
C658	CERSMT_0805	20D2
C659	CERSMT_1206	18B3
C660	CERSMT_0805	2B8
C661	CERSMT_0805	20D2
C662	CERSMT_1206	20D1
C663	CERSMT_0805	20D5
C664	CERSMT_1206	20D5
C665	CERSMT_0805	18D5
C666	CERSMT_1206	20D3
C667	CERSMT_0805	20C5
C668	CERSMT_0805	20D5
C669	CERSMT_1206	20D5
C670	CERSMT_0805	19D7
C671	CERSMT_0805	19D7
C672	CERSMT_0805	19D8
C673	CERSMT_0805	19D8
C674	CERSMT_1206	18D5
C675	CERSMT_0805	20D3
C676	CERSMT_0805	20C4
C677	CERSMT_0603	20C3
C678	CERSMT_1206	19D7

OEC MEDICAL SYSTEMS, INC.

SIZE	DWG NO.	REV
D	00-880921	A1
SCALE:		SHEET 25

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C679  CERSMT_1206 18B6
C680  CERSMT_1206 20C5
C681  CERSMT_1210 2C5
C682  CERSMT_0805 19D7
C683  CERSMT_0805 19D6
C684  CERSMT_1206 19D6
C685  CERSMT_0805 18B7
C686  CERSMT_1206 18B4
C687  CERSMT_1206 19D7
C688  CERSMT_1206 19D7
C689  CERSMT_1206 19D8
C690  CERSMT_1206 19D8
C691  CERSMT_1206 2B8
C692  CERSMT_1206 19D6
C693  CERSMT_0805 20D3
C694  CERSMT_1206 20D3
C695  CERSMT_0805 20C3
C696  CERSMT_0603 20C3
C697  CERSMT_0805 19D6
C698  CERSMT_1206 19D6
C699  CERSMT_0805 19D6
C700  CERSMT_0805 18B5
C701  CERSMT_0805 7C7
C702  CERSMT_0805 20D1
C703  CERSMT_1206 20D1
C704  CERSMT_0805 4D4
C705  CERSMT_0805 8C7
C706  CERSMT_1206 20D4
C707  CERSMT_1206 20D4
C708  CERSMT_0805 20D3
C709  CERSMT_0805 19D6
C710  CERSMT_1206 19D7
C711  CERSMT_0805 19C5
C712  CERSMT_0805 19C5
C713  CERSMT_0805 19C5
C714  CERSMT_0805 19C5
C715  CERSMT_0805 20D4
C716  CERSMT_1206 20D3
C717  CERSMT_1206 19D6
C718  CERSMT_0805 19D7
C719  CERSMT_0805 20D4
C720  CERSMT_0805 20C3
C721  CERSMT_0603 20C3
C722  CERSMT_0805 20C3
C723  CERSMT_1206 19D8
C724  CERSMT_1206 19C5
C725  CERSMT_1206 19C5
C726  CERSMT_1206 19C5
C727  CERSMT_1206 19C5
C728  CERSMT_0805 19D8
C729  CERSMT_1206 19D7
C730  CERSMT_0805 19D7
C731  CERSMT_0805 19D7
C732  CERSMT_1206 19D7
C733  CERSMT_1206 19D8
C734  CERSMT_0805 19D8
C735  CERSMT_1206 19C5
C736  CERSMT_0805 19C5
C737  CERSMT_1206 19C5
C738  CERSMT_1206 19D6
C739  CERSMT_1206 2C7
C740  CERSMT_0805 19D7
C741  CERSMT_1206 19D7
C742  CERSMT_0805 19D7
C743  CERSMT_1206 19D7
C744  CERSMT_0805 19D6
C745  CERSMT_1206 19D6
C746  CERSMT_1206 19D8
C747  CERSMT_1206 19D8
C748  CERSMT_0805 19C5
C749  CERSMT_1206 19C4
C750  CERSMT_1206 19C4
C751  CERSMT_0805 19D7
C752  CERSMT_0805 19D6
C753  CERSMT_0805 19D8
C754  CERSMT_1206 19C4
C755  CERSMT_1206 19C4
C756  CERSMT_1206 19D7
C757  CERSMT_0805 19D8
C758  CERSMT_0805 19C4
C759  CERSMT_0805 19C4
C760  CERSMT_0805 19C4
C761  CERSMT_0805 19C4
C762  TASMT_7343 10B7
C763  TASMT_7343 10B7
C764  TASMT_7343 10B7
C765  CERSMT_0603 20C3
C766  CERSMT_0805 20C3
C767  CERSMT_0603 20C3
C768  CERSMT_0805 20C3
C769  CERSMT_0603 20C2
C770  CERSMT_0805 20C2
C771  CERSMT_0603 20C2
C772  CERSMT_0805 20C2
C773  CERSMT_0603 20C2
C774  CERSMT_0805 20C2
C775  CERSMT_0603 20C2
DS1   LED4_67480200 4C2
DS2   LED4_67480200 5B3
DS3   LED4_67480200 4B7
DS4   LED4_67480200 4B6
DS5   LED4_67480200 4B6
DS6   LED4_67480200 10C2
DS7   LED4_67480200 10C2
E1    PCB_STIF_7 21B5
E2    JMPST_1X2_90012601 11D4
E3    JMPST_1X2 11A6
E5    JMPST_1X2 11A3
E7    JMPST_1X2 2C6
FL1   EMI_FLTR_43600000 11D2
FL2   EMI_FLTR_43600000 10C7
FL3   EMI_FLTR_43600000 11D2
J4    PCI32_5VR_124 3A6 3A7 3B6 3B7 3B7 3B7 3B7 3C6
            3C6 3C6 3C7 3D6 3D6 3D6 3D7 3D7
J5    PCI32_5VR_124 3A4 3A5 3B4 3B4 3B5 3B5 3C4 3C4
            3C4 3C5 3C5 3D4 3D5
J7    PCI32_5VR_124 3A1 3A1 3A2 3B1 3B1 3B1 3B2 3B2
            3B2 3C1 3C1 3C2 3C2 3C2 3D1 3D2
J8    DSUB_9_MTG_51109739 11B1 11C1 11C1
L1    FR_BD_SMT_43200000 11C1
L2    FR_BD_SMT_43200000 11C2
L3    FR_BD_SMT_43200000 11C2
L4    FR_BD_SMT_43200000 11D2
L5    FR_BD_SMT_43200000 11C2
L6    FR_BD_SMT_43200000 11D3
P1    CONN_EDGE_PCI_124_5V 2A6 2A6 2A6 2A6 2A6 2A6
            2B6 2B6 2C6 2C6 2C6 2C6 2C8 2C8
            2C8 2C8 2C8 2C8 2D6 2D6 2D8 2D8 2D8
            2D8 2D8 2D8
P3    MINJRRA_2X4_51411109 10C8
P6    D50RA_40P_51180007 4C8 4C8 4C8 4D8 4D8 4D8
P9    HDRIBSTW_2X10_51106232 4A8 4A8 4B8 4B8
P10   HDRIBST_2X10 4C5 4D2 9D5 9D6 21A7 21A7 21A8
            21B7 21B8
P11   HDRIBST_2X10 5A2 6A5 6C7 6D5 6D5 21A8 21B6
            21B8
P12   HDRIBST_2X10 4D2 9A4 9B6 9C4 9D6 21A6 21A8
            21B6 21B8
P13   HDRIBST_2X10 5D2 5D2 5D3 5D3 21A6 21A8 21B6
            21B8
P14   HDRIBST_2X10 4C4 4C7 4D5 4D7 5B4 5B4 5B5 21A8
            21B6 21B8
P15   HDRIBST_2X10 4B5 21A6 21A8 21A8 21B6 21B8
P16   HDRIBST_2X10 9C1 9C3 9D1 21A6 21A8 21B6 21B8
P17   HDRIBST_2X10 7A5 7C7 7D5 9A4 21A7 21B6 21B8
P18   HDRIBST_2X10 8A5 8C7 8D5 9A1 21A7 21B6 21B7
P19   HDRIBST_2X10 4B2 21A6 21A7 21A8 21B6 21B7
P20   HDRIBST_2X10 4B1 4D2 4D4 5A2 21A6 21A7 21B6
            21B7
P21   HDRIBST_2X10 14D8 21A7 21B6 21B7
P22   HDRIBST_2X10 11A1 11A2 11A3 11A4 21A7 21B6
            21B7
P23   HDRIBST_2X10 11B4 11B4 11B4 11C4 11C4 11D3
            11D4 11D4 21A7 21B6 21B7
P24   HDRIBST_2X10 11A8 11B8 11B8 21A6 21A6 21A7
            21B6 21B7
P25   HDRIBST_2X10 4B1 4B2 21A6 21A7 21B6 21B7
P26   HDBKST_2X5_90012602 10D5
R1    RESSMT_0805 4C7
R2    RESSMT_0805 4C7
R3    RESSMT_0805 10D4
R4    RESSMT_0805 4C7
R5    RESSMT_0805 4C7
R6    RESSMT_0805 10D4
R7    RESSMT_0805 5B8
R8    RESSMT_0805 5B8
R9    RESSMT_0805 5B7
R10   RESSMT_0805 5B7
R11   RESSMT_0805 10D3
R12   RESSMT_0805 5B7
R13   RESSMT_0805 5B7
R14   RESSMT_1206 3B4
R15   RESSMT_0805 5B5
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R17   RESSMT_0805 5B6
R18   RESSMT_0805 5B6
R19   RESSMT_0805 5B6
R20   RESSMT_0805 5C7
R21   RESSMT_0805 5B5
R22   RESSMT_0805 5B5
R23   RESSMT_1206 3B5
R24   RESSMT_0805 5B6
R25   RESSMT_0805 5B6
R26   RESSMT_0805 5B6
R27   RESWW_2W  11D1
R28   RESSMT_0805 5C6
R29   RESSMT_0805 5B5
R30   RESSMT_0805 5B5
R31   RESSMT_0805 5B7
R32   RESSMT_0805 5B7
R33   RESSMT_0805 5B7
R34   RESSMT_0805 5B7
R35   RESSMT_0805 4D7
R36   RESSMT_1206 3B2
R37   RESSMT_0805 4D7
R38   RESSMT_0805 4D7
R39   RESSMT_0805 21D8
R40   RESSMT_0805 5C1
R41   RESSMT_0805 5D1
R42   RESSMT_0805 5D1
R43   RESSMT_1206 3B3
R44   RESSMT_0805 21D7
R45   RESSMT_0805 21D7
R46   RESSMT_0805 21D8
R47   RESSMT_0805 5D3
R48   RESSMT_0805 21D7
R49   RESSMT_0805 21D7
R50   RESSMT_0805 8B3
R51   RESSMT_0805 7C4
R52   RESSMT_0805 8C3
R53   RESSMT_0805 7D4
R54   RESSMT_0805 8D4
R55   RESSMT_0805 9C5
R56   RESSMT_0805 9B5
R57   RESSMT_0603 11C1
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R59   RESSMT_0603 11C2
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R62   RESSMT_0805 7C3
R63   RESSMT_0603 11C2
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R65   RESSMT_0805 6D4
R66   RESSMT_0805 7C3
R67   RESSMT_0805 7D7
R68   RESSMT_0805 8B7
R69   RESSMT_0805 6D4
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R71   RESSMT_0805 8D7
R72   RESSMT_0805 7D4
R73   RESSMT_0805 7D4
R74   RESSMT_0805 7D7
R75   RESSMT_0805 7D7
R76   RESSMT_0805 8C7
R77   RESSMT_0805 8D7
R78   RESSMT_0805 11D3
R79   RESSMT_0805 9D8
R80   RESSMT_0805 9C6
R81   RESSMT_0805 5B3
R82   RESSMT_0805 9C6
R83   RESSMT_0805 9D6
R84   RESSMT_0805 9D4
R85   RESSMT_0805 6D7
R86   RESSMT_0603 11D3
R87   RESSMT_0805 9C6
R88   RESSMT_0603 11D4
R89   RESSMT_0805 9C5
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R97   RESSMT_0805 11D4
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R109  RESSMT_0805 9B6
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R118  RESSMT_0805 9B6
R119  RESSMT_0805 9B6
R120  RESSMT_0805 6C4
R121  RESSMT_0805 9B1
R122  RESSMT_0805 9B1
R123  RESSMT_0805 9B1
R124  RESSMT_0805 11A7
R125  RESSMT_0805 11A7
R126  RESSMT_0805 11A7
R127  RESSMT_0805 11A7
R128  RESSMT_0805 7C4
R129  RESSMT_0805 7C4
R130  RESSMT_0805 7C3
R131  RESSMT_0805 9B1
R132  RESSMT_0805 9B1
R133  RESSMT_0805 8C4
R134  RESSMT_0805 8C4
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R135	RESSMT_0805	8C4
R136	RESSMT_0805	9D5
R137	RESSMT_0805	9D3
R138	RESSMT_0805	9B1
R139	RESSMT_0805	9B1
R140	RESSMT_0805	9B1
R141	RESSMT_0805	11A7
R142	RESSMT_0805	11A7
R143	RESSMT_0805	11A8
R144	RESSMT_0805	11A8
R145	RESSMT_0805	9B6
R146	RESSMT_0805	9B6
R147	RESSMT_0805	8C4
R148	RESSMT_0805	8C4
R149	RESSMT_0805	8C4
R150	RESSMT_0805	9B1
R151	RESSMT_0805	9A1
R152	RESSMT_0805	9B1
R153	RESSMT_0805	9B1
R154	RESSMT_0805	7C4
R155	RESSMT_0805	7C4
R156	RESSMT_0805	11A7
R157	RESSMT_0805	11A7
R158	RESSMT_0805	11A7
R159	RESSMT_0805	11A8
R160	RESSMT_0805	9A6
R161	RESSMT_0805	9B2
R162	RESSMT_0805	9B3
R163	RESSMT_0805	9B6
R164	RESSMT_0805	9B6
R165	RESSMT_0805	9B6
R166	RESSMT_0805	6C3
R167	RESSMT_0805	9B1
R168	RESSMT_0805	9B1
R169	RESSMT_0805	9A1
R170	RESSMT_0805	9A1
R171	RESSMT_0805	6C3
R172	RESSMT_0805	7C7
R173	RESSMT_0805	11A5
R174	RESSMT_1206	2C4
R175	RESSMT_1206	2C4
R176	RESSMT_1206	2C4
R177	RESSMT_1206	2C4
R178	RESSMT_0805	2B3
R179	RESSMT_0805	2B4
R180	RESSMT_0805	9D3
R181	RESSMT_0805	9C2
R182	RESSMT_0805	8C7
R183	RESSMT_0805	11A5
R184	RESSMT_0805	9B6
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R186	RESSMT_0805	9B6
R187	RESSMT_0805	9B6
R188	RESSMT_0805	6C4
R189	RESSMT_0805	6C4
R190	RESSMT_0805	11A5
R191	RESSMT_0805	11A5
R192	RESSMT_0805	9B4
R194	RESSMT_0805	11B3
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R196	RESSMT_0805	11B3
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R217	RESSMT_0805	5B7
R218	RESSMT_0805	5B7
R219	RESSMT_0805	11B3
R220	RESSMT_0805	4D5
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R222	RESSMT_0805	4C6
R223	RESSMT_0805	5B7
R224	RESSMT_0805	5B7
R225	RESSMT_0805	4D7
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R230	RESSMT_0805	5B7
R231	RESSMT_0805	5B7
R232	RESSMT_0805	5D3
R233	RESSMT_0805	11A3
R234	RESSMT_0805	11A3
R235	RESSMT_0805	5B2
R236	RESSMT_0805	2D7
R237	RESSMT_1206	4A6
R238	RESSMT_0805	5B2
R239	RESSMT_0805	5D4
R240	RESSMT_0805	5C2
R241	RESSMT_0805	5C3
R242	RESSMT_0805	5D4
R243	RESSMT_0805	21D8
R244	RESSMT_0805	4B5
R245	RESSMT_0805	5C2
R246	RESSMT_0805	21D8
R247	RESSMT_0805	21D7
R248	RESSMT_0805	5D3
R249	RESSMT_0805	5D4
R250	RESSMT_0805	5D6
R251	RESSMT_0805	5C3
R252	RESSMT_0805	21D7
R253	RESSMT_0805	6D7
R254	RESSMT_0805	2C5
R255	RESSMT_0805	21C5
R256	RESSMT_0805	10C5
R257	RESSMT_0805	10B4
R259	RESSMT_0805	10C4
R260	RESSMT_0805	6D4
R261	RESSMT_0805	18C4
R262	RESSMT_0805	9D6
R263	RESSMT_0805	9C2
R264	RESSMT_0805	5C3
R265	RESSMT_0805	7B7
R266	RESSMT_0805	10B5
R268	RESSMT_0805	10C4
R269	RESSMT_0805	21C5
R270	RESSMT_0805	21C6
R271	RESSMT_0805	21C6
R272	RESSMT_0805	21C6
R273	RESSMT_0805	7C3
R274	RESSMT_1206	10A3
R275	RESSMT_0805	9C6
R276	RESSMT_0805	6D7
R277	RESSMT_0805	10B4
R278	RESSMT_0805	10A4
R279	RESSMT_0805	10B4
R281	RESSMT_0805	8D7
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R283	RESSMT_0805	5B3
R284	RESSMT_0805	7D4
R286	RESSMT_0805	7D7
R287	RESSMT_0805	11D4
R288	RESSMT_1206	10B3
R289	RESSMT_1206	11D3
R290	RESSMT_0805	10B4
R291	RESSMT_0805	9A8
R292	RESSMT_0805	9C6
R293	RESSMT_0805	11D3
R294	RESSMT_0603	11D3
R295	RESSMT_0603	11D3
R296	RESSMT_0805	9D8
R297	RESSMT_0805	9C6
R298	RESSMT_0805	9C6
R299	RESSMT_0805	9C6
R301	RESSMT_0805	9C6
R302	RESSMT_0805	9C6
R303	RESSMT_0805	9D7
R304	RESSMT_0805	9D5
R305	RESSMT_0805	9D8
R306	RESSMT_0805	9C6
R307	RESSMT_0805	9C6
R308	RESSMT_0805	5D4
R309	RESSMT_0805	5D6
R310	RESSMT_0805	6D7
R311	RESSMT_0603	4B4
R312	RESSMT_0805	8C3
R313	RESSMT_0805	9D5
R314	RESSMT_0805	6C4
R315	RESSMT_0805	8C3
R316	RESSMT_0805	11D5
R317	RESSMT_0805	11C8
R318	RESSMT_0805	11C8
R319	RESSMT_0805	6C7
R320	RESSMT_0805	6B7
R321	RESSMT_0805	8C3
R322	RESSMT_0805	9D2
R323	RESSMT_0805	11D5
R324	RESSMT_0805	11D4
R325	RESSMT_0805	11C8
R326	RESSMT_0805	2D4
R327	RESSMT_0805	6C4
R328	RESSMT_0805	7C4
R329	RESSMT_0805	7C7
R330	RESSMT_0805	6C4
R331	RESSMT_0805	8D4
R332	RESSMT_0805	11A6
R333	RESSMT_1206	2D2
R334	RESSMT_0805	11D5
R335	RESSMT_0805	11D5
R336	RESSMT_0805	11D5
R337	RESSMT_0805	11D5
R338	RESSMT_0805	6C3
R339	RESSMT_0805	7C4
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R341	RESSMT_0805	2D1
R342	RESSMT_0805	8C4
R343	RESSMT_0805	6C4
R344	RESSMT_0805	11D5
R345	RESSMT_0805	11D5
R346	RESSMT_0805	11A6
R347	RESSMT_0805	11D5
R348	RESSMT_0805	11A6
R349	RESSMT_1206	2D2
R350	RESSMT_0805	2D2
R351	RESSMT_0805	8D4
R352	RESSMT_0805	11D5
R353	RESSMT_0805	2D4
R354	RESSMT_0805	8C4
R355	RESSMT_0805	7C4
R356	RESSMT_0805	11D6
R357	RESSMT_0805	11D5
R358	RESSMT_0805	11A7
R359	RESSMT_0805	11A7
R360	RESSMT_0805	11D5
R361	RESSMT_0805	2D3
R362	RESSMT_0805	9B6
R363	RESSMT_0805	4D3
R364	RESSMT_0805	6C4
R365	RESSMT_0805	11D6
R366	RESSMT_0805	11D6
R367	RESSMT_0805	11D6
R368	RESSMT_1206	2D2
R369	RESSMT_0805	5C7
R370	RESSMT_0805	2D3
R371	RESSMT_0805	2D3
R372	RESSMT_0805	9B3
R374	RESSMT_0805	6C4
R375	RESSMT_0805	9A1
R376	RESSMT_0805	9A1
R377	RESSMT_0805	9B1
R378	RESSMT_0805	11A6
R379	RESSMT_0805	11A6
R380	RESSMT_0805	11A5
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R382	RESSMT_0805	11A7
R383	RESSMT_0805	11A7
R384	RESSMT_0805	11A7
R385	RESSMT_0805	7C4
R386	RESSMT_0805	7C4
R387	RESSMT_0805	7B3
R388	RESSMT_0805	9B1
R389	RESSMT_0805	9B1
R390	RESSMT_0805	8C4
R391	RESSMT_0805	8C4
R392	RESSMT_0805	8C4
R393	RESSMT_0805	9C1
R394	RESSMT_0805	9D5
R395	RESSMT_0805	9D2
R396	RESSMT_0805	6B3
R397	RESSMT_0805	9B1
R398	RESSMT_0805	9B1
R399	RESSMT_0805	9B1
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R405	RESSMT_0805	8C4
R406	RESSMT_0805	11A6
R407	RESSMT_0805	11A6
R408	RESSMT_0805	11A5
R409	RESSMT_0805	2C5
R410	RESSMT_1206	2D3
R411	RESSMT_0805	9A1
R412	RESSMT_0805	6C3
R413	RESSMT_0805	9B1
R414	RESSMT_0805	9B1
R415	RESSMT_0805	7C4
R418	RESSMT_0805	7C4
R420	RESSMT_0805	11A7
R422	RESSMT_0805	11A7
R424	RESSMT_0805	11A8
R426	RESSMT_0805	11A8
R429	RESSMT_0805	9B6
R430	RESSMT_0805	9C2
R431	RESSMT_0805	9B3
R434	RESSMT_0805	9B2
R435	RESSMT_0805	4D4
R436	RESSMT_0805	9B6
R437	RESSMT_0805	9B6
R438	RESSMT_0805	9B6
R439	RESSMT_0805	9C4
R440	RESSMT_0805	11A5
R441	RESSMT_0805	6D4
R442	RESSMT_0805	9B1
R443	RESSMT_0805	9B1

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R445	RESSMT_0805	9B1
R446	RESSMT_0805	9B1
R447	RESSMT_0805	9B1
R448	RESSMT_0805	6C7
R449	RESSMT_0805	9B3
R450	RESSMT_0805	9B2
R451	RESSMT_0805	9C3
R452	RESSMT_1206	2C4
R453	RESSMT_0805	9D3
R454	RESSMT_0805	4C7
R455	RESSMT_0805	4C7
R456	RESSMT_0805	9B6
R457	RESSMT_0805	9D4
R458	RESSMT_0805	9C6
R459	RESSMT_0805	9B6
R460	RESSMT_0805	11A6
R461	RESSMT_0805	11A5
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R463	RESSMT_0805	9B6
R464	RESSMT_0805	9B6
R465	RESSMT_0805	9B6
R466	RESSMT_0805	9B6
R467	RESSMT_0805	6C4
R468	RESSMT_0805	6C4
R469	RESSMT_0805	9C3
R470	RESSMT_0805	9C6
R471	RESSMT_0805	9C6
R472	RESSMT_0805	9C6
R473	RESSMT_0805	9C6
R474	RESSMT_0805	9B6
R475	RESSMT_0805	9A6
R476	RESSMT_0805	9C6
R477	RESSMT_0805	9A6
R478	RESSMT_0805	9A6
R479	RESSMT_0805	9A3
R480	RESSMT_0805	9A6
R481	RESSMT_0805	9C3
R482	RESSMT_0805	9C6
R483	RESSMT_0805	9A6
R484	RESSMT_0805	9A6
R485	RESSMT_0805	9A6
R486	RESSMT_0805	9A6
R???	RESSMT_0805	4D6
TP1	TEST_POINT_COLOR	10C5
TP2	TEST_POINT_COLOR	10C6
TP3	TEST_POINT_COLOR	10C6
TP4	TEST_POINT_COLOR	11D1
TP5	TEST_POINT_COLOR	11D1
TP6	TEST_POINT_COLOR	11D1
TP7	TEST_POINT_COLOR	10C6
TP8	TEST_POINT_COLOR	9D6
TP9	TEST_POINT_COLOR	9D8
TP10	TEST_POINT_COLOR	2B8
TP11	TEST_POINT_COLOR	2C6
TP12	TEST_POINT_COLOR	10C5
TP13	TEST_POINT_COLOR	10C6
TP14	TEST_POINT_COLOR	2C3
TP15	TEST_POINT_COLOR	2C6
TP16	TEST_POINT_COLOR	2C6
TP17	TEST_POINT_COLOR	2D8
TP18	TEST_POINT_COLOR	2B7
TP19	TEST_POINT_COLOR	2B7
TP20	TEST_POINT_COLOR	2C7
TP21	TEST_POINT_COLOR	2D7
U1	LT1086	10C7
U2	EPC1	10D3
U3	74LPT16652	5C5
U4	74LCX16374	4D6
U5	74LCX16244	4D5
U6	74FCT88915	4D6
U7	74LCX16244	4B4
U8	FIFO_64X36X2	5D3
U9	74LCX16374_S	9C5 21C7

U10	74LCX16374	9B5
U11	LT1086	11D1
U12	74LCX16244_S	10B4 10C4 10C4 21C5
U13	EPF10K10TC144_VCC	13C6
U14	NM93CS46_VCC	9A8
U15	VSC7125_VCC	11D3
U16	EPF10K10TC144_VCC	14D6
U17	EPF10K10TC144_VCC	15D6
U18	EPF10K10TC144_VCC	16D5
U19	74LCX16652	6B7
U20	74LCX16652	7B7
U21	74LCX16652	8B7
U22	LT1086	11D1
U23	74LCX16652	6B6
U24	74LCX16652	7B6
U25	74LCX16652	8B6
U26	SDRAM_1MX16	6B5
U27	SDRAM_1MX16	7B5
U28	SDRAM_1MX16	8B5
U29	HP_TACHLITE_B_VCC	11D8
U30	PCI9050_32BIT_VCC	17D6
U31	EPF10K20RC208_VCC	12D6
U32	74LCX16652	8B2
U33	74LCX16652	6B2
U34	SDRAM_1MX16	6B3
U35	74LCX16652	7B2
U36	SDRAM_1MX16	7B3
U37	SDRAM_1MX16	8B3
U38	74LCX16652	8B2
U39	74LCX16652	6B2
U40	74LCX16652	7B2
U41	SSRAM64KX36P_VCC	11B3
U42	EPM7064_44	18C5
U43	FIFO_64X36X2	9D2
U45	PCI_PCI21152AB_VCC	2D5
U46	SSRAM64KX18_VCC	9C4
U47	SSRAM64KX18_VCC	9B4
U48	LT1086	2B8
XE4	SHORT_PC_X1	11A6
XE6	SHORT_PC_X1	11A3
XE8	SHORT_PC_X1	2C6
Y1	OSC_8P_EN_V33_VCC	11D3

OEC MEDICAL SYSTEMS, INC.

SIZE	DWG NO.	REV
D	00-880921	A1
SCALE:		SHEET 28

DWG NO.	SHT	REV
00-881445	1	A

M	ENGIN. REV. 1.2 REVISIONS		EDR 01346
REV	DESCRIPTION	DATE	APPROVED
A	RELEASED TO MANUFACTURING PER ECO BW21A	4-1-99	MAHON

PCI BUS INTERFACE

PCI BUS CONNECTOR
(FOR POWER & GND SEE SHEET 8)

P1 - B9 ← PRSNT1*
P1 -B11 ← PRSNT2*

P1 -A15 ← RST* → 148 RST
P1 -B16 ← CLK → 149 CLK

P1 -B39 ← LOCK* → 18 LOCK
P1 - A6 ← INTA* → 44 INTA
P1 -A43 ← PAR → 21 PAR
P1 -B40 ← PERR* → 19 PERR
P1 -B42 ← SERR* → 20 SERR

P1 -A26 ← IDSEL → 159 IDSEL
P1 -A34 ← FRAME* → 13 FRAME
P1 -B35 ← IRDY* → 14 IRDY
P1 -A36 ← TRDY* → 15 TRDY
P1 -A38 ← STOP* → 17 STOP
P1 -B37 ← DEVSEL* → 16 DEVSEL

C/BE<3..0>*

P1 -B26 ← C/BE<3>* 3
P1 -B33 ← C/BE<2>* 2
P1 -B44 ← C/BE<1>* 1
P1 -A52 ← C/BE<0>* 0

AD<31..0>

P1 -B20 ← AD<31> 31
P1 -A20 ← AD<30> 30
P1 -B21 ← AD<29> 29
P1 -A22 ← AD<28> 28
P1 -B23 ← AD<27> 27
P1 -A23 ← AD<26> 26
P1 -B24 ← AD<25> 25
P1 -A25 ← AD<24> 24
P1 -B27 ← AD<23> 23
P1 -A28 ← AD<22> 22
P1 -B29 ← AD<21> 21
P1 -A29 ← AD<20> 20
P1 -B30 ← AD<19> 19
P1 -A31 ← AD<18> 18
P1 -B32 ← AD<17> 17
P1 -A32 ← AD<16> 16
P1 -A44 ← AD<15> 15
P1 -B45 ← AD<14> 14
P1 -A46 ← AD<13> 13
P1 -B47 ← AD<12> 12
P1 -A47 ← AD<11> 11
P1 -B48 ← AD<10> 10
P1 -A49 ← AD<9> 9
P1 -B52 ← AD<8> 8
P1 -B53 ← AD<7> 7
P1 -A54 ← AD<6> 6
P1 -B55 ← AD<5> 5
P1 -A55 ← AD<4> 4
P1 -B56 ← AD<3> 3
P1 -A57 ← AD<2> 2
P1 -B58 ← AD<1> 1
P1 -A58 ← AD<0> 0

PCI BUS NO-CONNECT PINS

P1 - B7	N.C.	INTB*
P1 - A7	N.C.	INTC*
P1 - B8	N.C.	INTD*
P1 - A9	N.C.	RESERVED
P1 -B10	N.C.	RESERVED
P1 -A11	N.C.	RESERVED
P1 -A14	N.C.	RESERVED
P1 -B14	N.C.	RESERVED
P1 -A19	N.C.	RESERVED
P1 -B18	N.C.	REQ*
P1 -A17	N.C.	GNT*
P1 -A41	N.C.	SBO*
P1 -A40	N.C.	SDONE
P1 -A60	N.C.	REQ64*
P1 -B60	N.C.	ACK64*
P1 - A1	N.C.	PCI_TRST*
P1 - B2	N.C.	PCI_TCK
P1 - A3	N.C.	PCI_TMS
P1 - A4	N.C.	PCI_TDI
P1 - B4	N.C.	PCI_TDO

VCC

R103 10K (1 2 3 4 / 8 7 6 5)
R104 10K (1 2 3 4 / 8 7 6 5)
R105 10K (1 2 3 4 / 8 7 6 5)

LINTR 2
TP39 WHT

PLX_RD* TP44 WHT
PLX_WR* TP43 WHT
LRDY* TP47 WHT
CS 2* TP40 WHT
CS 1* TP46 WHT
CS 0* TP45 WHT

PLX_LRESET* (OUT)
IPCLK4 (IN)
PLX_LINT2* (IN)

132 LRESET
63 BCLKO
135 LCLK
136 LINTI2
137 LINTI1
134 LHOLD
133 LHOLDA

SEE SHEET 11 (PLX9050), U36

PCI9050_32BIT

RST	148	
CLK	149	
LOCK	18	
INTA	44	
PAR	21	
PERR	19	
SERR	20	
IDSEL	159	
FRAME	13	
IRDY	14	
TRDY	15	
STOP	17	
DEVSEL	16	
C/BE<3..0>n		
AD<31..0>		
LW/Rn	127	
WR	125	PLX_LWR_RD* (OUT), PLX_WR* (OUT)
RD	126	PLX_RD* (OUT)
BTERM	129	
LRDYI	128	PLX_LRDY* (IN)
BLAST	124	
LLOCK	139	
USER1	141	
WAITO	138	LPT_RESET (OUT)
USER0		
ADS	123	
ALE	64	
USER3	141	
CS3		
USER2	140	PLX_CS2* (OUT)
CS2		
CS1	131	PLX_CS1* (OUT)
CS0	130	PLX_C50* (OUT)
LBE<3..0>n		PLX_LBE<3..0> (OUT)
LA<27..2>		PLX_LA<27..2>
LAD<31..0>		PLX_LD<31..0> (BI)
EESK	144	
EECS	142	
EEDI	145	
EEDO	143	
TEST	99	
MODE	68	

PLX_LA<23..2> <23..2>
PLX_LBE<1> 1
PLX_LBE<0> 0
PLX_ADR<23..0> (OUT)

U22
NM93CS46
SK 2
PE 6 CS 1
PRE 7 DI 3
DO 4
PACK_TYPE=SDIP

VCC
R102 10K 5% 0.06W (6 7 1 4 / 3 2 8 5)

VCC
R121 10K (1 2 3 4 / 8 7 6 5) PLX_LD<31..24>
R120 10K (1 2 3 4 / 8 7 6 5) PLX_LD<23..16>
R110 10K (1 2 3 4 / 8 7 6 5) PLX_LD<15..8>
R109 10K (1 2 3 4 / 8 7 6 5) PLX_LD<7..0>
R108 10K (1 2 3 4 / 8 7 6 5) PLX_LA<31..28>
R107 10K (1 2 3 4 / 8 7 6 5) PLX_LA<27..24>
R91 10K (5 6 7 8 / 4 3 2 1) PLX_LA<23..20>
R90 10K (8 7 6 5 / 1 2 3 4) PLX_LA<19..16>

VCC
R68 1K
R88 1K
R67 1K
R66 1K
R65 1K

JTAG BIT BLASTER CONNECTOR

TCK (DCLK)	P16 - 1	JTAG_TCK (OUT)
GND	P16 - 2	
TDO (CONF_DONE)	P16 - 3	JTAG_TDO
VCC	P16 - 4	
TMS (CONFIG*)	P16 - 5	JTAG_TRST* (OUT), JTAG_TMS (OUT)
BBVCC	P16 - 6 ←	
(STATUS*)	P16 - 7 ←	
BBGND	P16 - 8 ←	
TDI (DATA0)	P16 - 9	JTAG_TDI
GND	P16 - 10	

NOTE 1

JTAG_TDI = EPC_JTAG_TDI (OUT)
EPC_JTAG_TDO (IN) = L_JTAG_TDI (OUT)
L_JTAG_TDO (IN) = R_JTAG_TDI (OUT)
R_JTAG_TDO (IN) = TV_JTAG_TDI (OUT)
TV_JTAG_TDO (IN) = JTAG_TDO

-01 SHOWN

DRAWING
LAST_MODIFIED=Thu Apr 1 10:40:14 1999

ITEM	QTY.	PART OR IDENT NO.	DESCRIPTION

PARTS LIST

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		CONTRACT NO.	
		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS: +/- DECIMALS: .XX+/- .XXX+/- ANGLES: +/-	MATERIAL / FINISH
00-878980	9800		
NEXT ASSEMBLY	USED ON		
APPLICATION		DO NOT SCALE DRAWING	

	APPROVED	DATE
DRAWN	G. POPE	11-3-98
CHECKED	J. ALLRED	1-11-99
ENGINEERING	G. POPE	1-11-99
APPROVED		

OEC MEDICAL SYSTEMS, INC.

DWG TITLE: 9800 DISPLAY ADAPTER

SIZE D | DWG NO. 00-881445 | REV A

SCALE: | SHEET 1 OF 19

05-016-9/93

IP INTERFACE

IP INTERFACE CONNECTOR

NO CONNECT → 4 - P9
NO CONNECT → 5 - P9
NO CONNECT → 17 - P9
NO CONNECT → 27 - P9
NO CONNECT → 28 - P9
NO CONNECT → 39 - P9
NO CONNECT → 40 - P9

CONNECTOR GNDS

1 - P9, 2 - P9, 3 - P9, 41 - P9, 43 - P9, 44 - P9, 45 - P9, 46 - P9, 47 - P9, 48 - P9, 49 - P9, 50 - P9, 51 - P9, 52 - P9, 53 - P9, 54 - P9, 55 - P9, 56 - P9, 57 - P9, 58 - P9, 59 - P9, 60 - P9, 61 - P9, 62 - P9, 63 - P9, 64 - P9, 65 - P9, 66 - P9, 67 - P9, 68 - P9, 69 - P9, 70 - P9, 71 - P9, 72 - P9, 73 - P9, 74 - P9, 75 - P9, 76 - P9, 77 - P9, 78 - P9, 79 - P9, 80 - P9

IPCLK*
TP32
WHT

U11
49FCT3806
OEB
OEA
MON
INB
INA
OB4
OB3
OB2
OB1
OB0
OA4
OA3
OA2
OA1
OA0

P9 - 42 ← IP_DIS_PIXCLK

R63 75, C34 330P
R64 10K
R44 75, C26 330P
R3 75, C8 330P
R114 75, C72 330P
R106 75, C70 330P
R93 75, C65 330P

IPCLK1 →
IPCLK2 →
IPCLK3 →
IPCLK4 →
IPCLK5 →

IPCLK1

P9 - 7 ← LD_D7
P9 - 8 ← LD_D6
P9 - 9 ← LD_D5
P9 - 10 ← LD_D4
P9 - 11 ← LD_D3
P9 - 12 ← LD_D2
P9 - 13 ← LD_D1
P9 - 14 ← LD_D0

R35, R37 75, C35, C36 330P

P9 - 19 ← RD_D7
P9 - 20 ← RD_D6
P9 - 21 ← RD_D5
P9 - 22 ← RD_D4
P9 - 23 ← RD_D3
P9 - 24 ← RD_D2
P9 - 25 ← RD_D1
P9 - 26 ← RD_D0

R38, R39 75, C37, C38 330P

P9 - 31 ← AD_D7
P9 - 32 ← AD_D6
P9 - 33 ← AD_D5
P9 - 34 ← AD_D4
P9 - 35 ← AD_D3
P9 - 36 ← AD_D2
P9 - 37 ← AD_D1
P9 - 38 ← AD_D0

R40, R41 75, C39, C40 330P

P9 - 15 ← DC_HDRV*
P9 - 16 ← DC_VDRV*
P9 - 6 ← LD_WREN*
P9 - 18 ← RD_WREN*
P9 - 30 ← AD_WREN*
P9 - 29 ← TAG*

R42, R43 75, C41, C42 330P

U12
74LCX16374
CLK1
OE1
CLK2
OE2
I0 I1 I2 I3 I4 I5 I6 I7
O0 O1 O2 O3 O4 O5 O6 O7

LFT_PIX_DATA<7..0> →
RHT_PIX_DATA<7..0> →

U14
74LCX16374

AUX_PIX_DATA<7..0> →
IP_HS* →
IP_VS* →
L_PIXWE_IN* →
R_PIXWE_IN* →
AUX_PIXWE_IN* →
IP_DATA_TAG* →

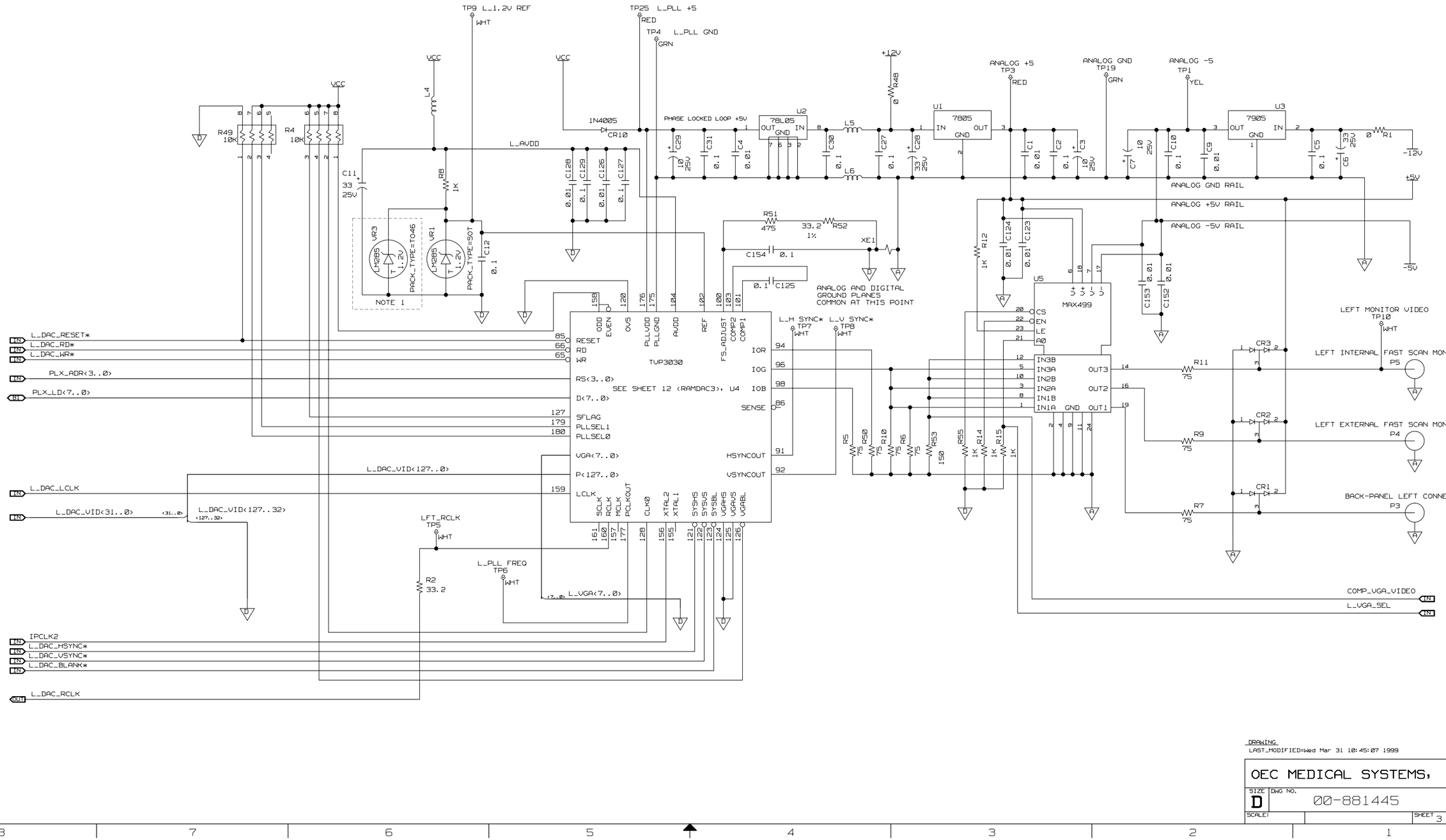
DRAWING
LAST_MODIFIED=Wed Mar 31 10:29:33 1999

OEC MEDICAL SYSTEMS, INC.

SIZE	DWG NO.	REV
D	00-881445	A
SCALE:	SHEET 2 OF 19	

05-017-9/93

LEFT CHANNEL VIDEO DAC & OUTPUT



DRAWING
LAST_MODIFIED=Wed Mar 31 10:45:07 1999

OEC MEDICAL SYSTEMS, INC.

SIZE	DWG NO.	REV
D	00-881445	A
SCALE:		SHEET 3 OF 19

05-017-9/93

RIGHT CHANNEL VIDEO DAC & OUTPUT

TP18 R_1.2V REF WHT
TP13 R_PLL +5 RED
TP31 R_PLL GND GRN
VCC
+12V
L3
L1
L2
R59 10K
R29 10K
1N4005 CR11
PHASE LOCKED LOOP +5V
U9 78L05 OUT GND IN
C13 10 25V
C15 0.1
C14 0.01
C33 0.1
C22 25V 33
R34 1K
R_AVDD
C115 0.01
C116 0.1
C113 0.01
C114 0.1
C20 0.01
C21 0.1
C19 10 25V
C17 0.01
C18 0.1
C16 10 25V
ANALOG GND RAIL
ANALOG +5V RAIL
ANALOG -5V RAIL
+5V
-5V
VR4 LM285 1.2V PACK_TYPE=TO46
VR2 LM285 1.2V PACK_TYPE=SOT
C23 0.1
NOTE 1
R61 475
33.2 R62
C138 0.1
C112 0.1
1K R21
C120 0.01
C119 0.01
U8 MAX499
C148 0.01
C147 0.01
TVP3030
ODD EVEN OVS PLLVDD PLLGND AVDD REF FS_ADJUST COMP2 COMP1
RESET RD WR RS<3..0> D<7..0> SFLAG PLLSEL1 PLLSEL0 VGA<7..0> P<127..0> LCLK
IOR IOG IOB SENSE HSYNCOUT VSYNCOUT
SCLK RCLK MCLK PCLKOUT CLK0 XTAL2 XTAL1 SYSHS SYSVS SYSBL VGAHS VGAVS VGABL
SEE SHEET 13 (RAMDAC4), U10
R_H SYNC* TP16 WHT
R_V SYNC* TP17 WHT
R32 75
R60 75
R19 75
R33 75
R57 150
R24 1K
R22 1K
R23 1K
CS EN LE A0
IN3B IN3A IN2B IN2A IN1B IN1A
OUT3 OUT2 OUT1 GND
R27 75
R26 75
R25 75
CR9
CR8
CR7
RIGHT MONITOR VIDEO TP15 WHT
RIGHT INTERNAL FAST SCAN MONITOR P8
RIGHT EXTERNAL FAST SCAN MONITOR P7
BACK-PANEL RIGHT CONNECTOR P6
COMP_VGA_VIDEO
R_VGA_SEL
R_DAC_RESET*
R_DAC_RD*
R_DAC_WR*
PLX_ADR<3..0>
PLX_LD<7..0>
R_DAC_VID<127..0>
R_DAC_LCLK
R_DAC_VID<31..0>
R_DAC_VID<127..32>
RT_RCLK TP12 WHT
R_PLL FREQ TP14 WHT
R28 33.2
R_VGA<7..0>
IPCLK2
R_DAC_HSYNC*
R_DAC_VSYNC*
R_DAC_BLANK*
R_DAC_RCLK

DRAWING
LAST_MODIFIED=Wed Mar 31 10:46:03 1999

OEC MEDICAL SYSTEMS, INC.

SIZE	DWG NO.	REV
D	00-881445	A
SCALE:		SHEET 4 OF 19

05-017-9/93

LEFT CHANNEL MASTER SLAVE FRAME BUFFER

V3.3
R77
10K

LEFT_VIDEO_CTRL

IN L_JTAG_TDI — TDI
IN JTAG_TMS — TMS
IN JTAG_TCK — TCK
IN JTAG_TRST* — TRSTn
SEE SHEET 14, U18
TDO — OUT L_JTAG_TDO
IN L_CONF_CE* — CEn
IN CONFIG* — CONFIGn
IN CONF_DCLK — DCLK
IN CONF_DATA — DATA
CEOn — OUT L_CONF_CEO*
CONF_DONE — OUT CONF_DONE
STATUSn — OUT CONF_STATUS*
MSEL0
MSEL1
DEV_OE
IN PLX_LRESET* — DEV_CLRn

LFT_RHTn
VGA_SEL — OUT L_VGA_SEL
DAC_LCLK — OUT L_DAC_LCLK
IN L_DAC_RCLK — DAC_RCLK
DAC_HSn — OUT L_DAC_HSYNC*
DAC_VSn — OUT L_DAC_VSYNC*
IN IPCLK5 — IP_CLK
IN IP_HS* — IP_HSn
IN IP_VS* — IP_VSn
DAC_BLANKn — OUT L_DAC_BLANK*
DAC_WRn — OUT L_DAC_WR*
DAC_RDn — OUT L_DAC_RD*
IN L_PIXWE_IN* — IP_PXLWRn
DAC_RESETn — OUT L_DAC_RESET*
IN LFT_PIX_DATA<7..0> — IP_VID<7..0>
DAC_VID<31..0> — OUT L_DAC_VID<31..0>
IN PLX_CS1* — PLX_CS1n
PLX_LRDYn — OUT PLX_LRDY*
IN PLX_WR* — PLX_WRn
IN PLX_RD* — PLX_RDn
MRSR_CSn
IN PLX_CS0* — PLX_CS0n
IN PLX_LWR_RD* — PLX_LWR_RDn
MR_CASn
IN PLX_ADR<23..2> — PLX_ADR<23..2>
MR_RASn
IN PLX_BE<3..0> — PLX_BEn<3..0>
MR_WEn
IN PLX_LD<31..0> — PLX_DB<31..0>
MR_BA<1..0>
MR_ADR<11..0>
MR_DQM<3..0>
MR_DQ<31..0>
SR_CASn
SR_RASn
SR_WEn
SR_BA<1..0>
SR_ADR<11..0>
SR_DQM<3..0>
SR_DQ<31..0>

LVID_MD TP27 WHT
LRUN TP26 WHT
VID_MD_REQ
IP_COMP_ACTIVE
OUT_SYNC_RESET
COMP_RUN
INFI_WRREQ
INFI_RDREQ
MSFI_WRREQ
MSFI_RDREQ
DACFI_WRREQ
DACFI_RDREQ
OUTFI_WRREQ
OUTFI_RDREQ
TP_LED — OUT LFPGA_LED

U23 SDRAM_64MBIT
IN IPCLK5 — CLK
CKE
CAS
RAS
WE
CS
UDQM
LDQM
BA1, BA0
A12 A11 A10 A09 A08 A07 A06 A05 A04 A03 A02 A01 A00
DQ15 DQ14 DQ13 DQ12 DQ11 DQ10 DQ09 DQ08 DQ07 DQ06 DQ05 DQ04 DQ03 DQ02 DQ01 DQ00
R92 10K

U24 SDRAM_64MBIT
CLK
CKE
CAS
RAS
WE
CS
UDQM
LDQM
BA1, BA0
A12 A11 A10 A09 A08 A07 A06 A05 A04 A03 A02 A01 A00
DQ15 DQ14 DQ13 DQ12 DQ11 DQ10 DQ09 DQ08 DQ07 DQ06 DQ05 DQ04 DQ03 DQ02 DQ01 DQ00

U25 SDRAM_64MBIT
IPCLK5 IN — CLK
CKE
CAS
RAS
WE
CS
UDQM
LDQM
BA1, BA0
A12 A11 A10 A09 A08 A07 A06 A05 A04 A03 A02 A01 A00
DQ15 DQ14 DQ13 DQ12 DQ11 DQ10 DQ09 DQ08 DQ07 DQ06 DQ05 DQ04 DQ03 DQ02 DQ01 DQ00
R95 10K

U26 SDRAM_64MBIT
CLK
CKE
CAS
RAS
WE
CS
UDQM
LDQM
BA1, BA0
A12 A11 A10 A09 A08 A07 A06 A05 A04 A03 A02 A01 A00
DQ15 DQ14 DQ13 DQ12 DQ11 DQ10 DQ09 DQ08 DQ07 DQ06 DQ05 DQ04 DQ03 DQ02 DQ01 DQ00
V3.3
R94
10K

L_MR_BA<1..0>
L_MR_ADR<11..0>
L_MR_DQM<3..0>
L_MR_DQ<31..0>
L_SR_BA<1..0>
L_SR_ADR<11..0>
L_SR_DQM<3..0>
L_SR_DQ<31..0>

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LAST_MODIFIED=Wed Mar 31 10:46:51 1999

OEC MEDICAL SYSTEMS, INC.

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RIGHT CHANNEL MASTER SLAVE FRAME BUFFER

V3.3
R81
10K

RIGHT_VIDEO_CTRL

IN R_JTAG_TDI
IN JTAG_TMS
IN JTAG_TCK
IN JTAG_TRST*
IN R_CONF_CE*
IN CONFIG*
IN CONF_DCLK
IN CONF_DATA
IN PLX_LRESET*
IN R_DAC_RCLK
IN IPCLK4
IN IP_HS*
IN IP_VS*
IN R_PIXWE_IN*
IN RHT_PIX_DATA<7..0>
IN PLX_CS1*
IN PLX_WR*
IN PLX_RD*
IN PLX_CS0*
IN PLX_LWR_RD*
IN PLX_ADR<23..2>
IN PLX_LBE<3..0>
IN PLX_LD<31..0>

TDI
TMS SEE SHEET 15, U19
TCK
TRSTn
CEn
CONFIGn
DCLK
DATA
MSEL0
MSEL1
DEV_OE
DEV_CLRn

TDO → OUT R_JTAG_TDO
CEOn → OUT R_CONF_CEO*
CONF_DONE → OUT CONF_DONE
STATUSn → OUT CONF_STATUS*

LFT_RHTn
DAC_RCLK
IP_CLK
IP_HSn
IP_VSn
IP_PXLWRn
IP_VID<7..0>
PLX_CS1n
PLX_WRn
PLX_RDn
PLX_CS0n
PLX_LWR_RDn
PLX_ADR<23..2>
PLX_BEn<3..0>
PLX_DB<31..0>

VGA_SEL → OUT R_VGA_SEL
DAC_LCLK → OUT R_DAC_LCLK
DAC_HSn → OUT R_DAC_HSYNC*
DAC_VSn → OUT R_DAC_VSYNC*
DAC_BLANKn → OUT R_DAC_BLANK*
DAC_WRn → OUT R_DAC_WR*
DAC_RDn → OUT R_DAC_RD*
DAC_RESETn → OUT R_DAC_RESET*
DAC_VID<31..0> → OUT R_DAC_VID<31..0>
PLX_LRDYn → OUT PLX_LRDY*
MRSR_CSn
MR_CASn
MR_RASn
MR_WEn
MR_BA<1..0>
MR_ADR<11..0>
MR_DQM<3..0>
MR_DQ<31..0>
SR_CASn
SR_RASn
SR_WEn
SR_BA<1..0>
SR_ADR<11..0>
SR_DQM<3..0>
SR_DQ<31..0>

RVID_MD TP30 WHT
RRUN TP29 WHT
VID_MD_REQ
IP_COMP_ACTIVE
OUT_SYNC_RESET
COMP_RUN
INFI_WRREQ
INFI_RDREQ
MSFI_WRREQ
MSFI_RDREQ
DACFI_WRREQ
DACFI_RDREQ
OUTFI_WRREQ
OUTFI_RDREQ
TP_LED → OUT RFPGA_LED

U28 SDRAM_64MBIT
U29 SDRAM_64MBIT
U31 SDRAM_64MBIT
U32 SDRAM_64MBIT

IN IPCLK4
CLK, CKE, CAS, RAS, WE, CS, UDQM, LDQM
BA1, BA0, A12, A11, A10, A09, A08, A07, A06, A05, A04, A03, A02, A01, A00
DQ15, DQ14, DQ13, DQ12, DQ11, DQ10, DQ09, DQ08, DQ07, DQ06, DQ05, DQ04, DQ03, DQ02, DQ01, DQ00

R97 10K
R98 10K
R96 10K
V3.3

R_MR_BA<1..0>
R_MR_ADR<11..0>
R_MR_DQM<3..0>
R_MR_DQ<31..0>
R_SR_BA<1..0>
R_SR_ADR<11..0>
R_SR_DQM<3..0>
R_SR_DQ<31..0>

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OEC MEDICAL SYSTEMS, INC.

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FPGA CONFIG, VGA INPUT, AND EPP PRINTER PORT

VGA INPUT CONNECTOR

RED	P15 - 1	← N.C.
GREEN	P15 - 2	← VGA_GREEN
BLUE	P15 - 3	← VGA_BLUE
N.C.	P15 - 4	← N.C.
DIGITAL GND	P15 - 5	
RED RETURN	P15 - 6	← N.C.
GREEN RETURN	P15 - 7	← GREEN RETURN
BLUE RETURN	P15 - 8	← BLUE RETURN
N.C.	P15 - 9	← N.C.
DIGITAL GND	P15 - 10	
N.C.	P15 - 11	← N.C.
N.C.	P15 - 12	← N.C.
H. DRIVE	P15 - 13	→ VGA_HD
V. DRIVE	P15 - 14	→ VGA_VD
N.C.	P15 - 15	← N.C.

NOTE 1

E1 COMP_VGA_VIDEO

R71 75, R70 75, R72 1K, CR12 BAT54C (N.C.), U17 CA3246 ×4

R83 475, R69 200, R84 1K, R85 200, -5V

VGA_CS, VGA_HD, VGA_VD

BIT BLASTER CONNECTOR

DCLK	P10 - 1	
GND	P10 - 2	
CONF_DONE	P10 - 3	→ CONF_DONE
VCC	P10 - 4	
CONFIG*	P10 - 5	→ CONFIG*
BBVCC	P10 - 6	
STATUS*	P10 - 7	→ CONF_STATUS*
BBGND	P10 - 8	
DATA0	P10 - 9	→ CONF_DATA
GND	P10 - 10	

NOTE 1

R74 1K, R75 1K, R73 1K, R76 1K

CONF_DCLK, CONF_DONE, CONFIG*, CONF_STATUS*, CONF_DATA

U15 EPC2 (EPROM1), U13 EPC2 (EPROM2)

EPC_JTAG_TDI, JTAG_TMS, JTAG_TCK, EPC_JTAG_TDO

R46 10K

L_CONF_CE*, L_CONF_CE0*, R_CONF_CE*, R_CONF_CE0*, TV_CONF_CE*

EPP_IOCHRDY* (TP41 WHT), EPP_IRQ* (TP36 WHT)

PLX_ADR<10..0>, PLX_LD<31..0>, EPP_IOCHRDY*, EPP_IRQ*

LPT_RESET, PLX_RD*, PLX_WR*, PLX_CS2*

R89 10K, R87 374

U21 ST78C36 (CLOCK, RESET, IOR, IOW, AEN, CS, DACK, TC, IRQ, IOCHRDY, DRQ, PDIR)

24MHZ Y1, R86 1K, V5CLK, FL2 EMI FL 7A 50V, C52 0.1, C53 0.01

ENHANCED PARALLEL PORT

PE, ACK*, BUSY, SLCT, ERROR*, SLCTI*, INIT, AFDXT*, STROBE*

PLX_LD<7..0> → D7..D0

PD7..PD0 → R99 R100 R101 R117 R118 R119 R115 R116 33.2

C67 C68 C69 C73 C74 C75 C76 C77 180P

PD7 → P11 - 9, PD6 → P11 - 8, PD5 → P11 - 7, PD4 → P11 - 6, PD3 → P11 - 5, PD2 → P11 - 4, PD1 → P11 - 3, PD0 → P11 - 2

PE → P11 - 12, ACK* → P11 - 10, BUSY → P11 - 11, SLCT → P11 - 13, ERROR* → P11 - 15, SLCTI* → P11 - 17, INIT → P11 - 16, AFDXT* → P11 - 14, STROBE* → P11 - 1

P11 - 18, P11 - 19, P11 - 20, P11 - 21, P11 - 22, P11 - 23, P11 - 24, P11 - 25

U16 74ABT240

PLX_CS0*, LFPGA_LED, RFPGA_LED

DS1 → CS0*, LTP, RTP, CONFIG

R45 10K

DS2 → -5V, +5V, +3.3V, +2.5V

R30 1K, R31 1K, R47 374, R35 150

+5V, V3.3, V2.5

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OEC MEDICAL SYSTEMS, INC.

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TV VIDEO CONTROL & OUTPUT

TV_VIDEO_CTRL
SEE SHEET 16, U20
TDI
TMS
TCK
TRSTn
TDO
CEn
CONFIGn
DCLK
DATA
MSEL
DEV_OE
DEV_CLRn
CEOn
CONF_DONE
STATUSn
TV_JTAG_TDI
JTAG_TMS
JTAG_TCK
JTAG_TRST*
TV_JTAG_TDO
TV_CONF_CE*
CONFIG*
CONF_DCLK
CONF_DATA
TV_CONF_CEO*
CONF_DONE
CONF_STATUS*
PLX_LRESET*
R82 10K
V3.3
IPCLK3
IP_HS*
IP_VS*
AUX_PIX_DATA<7..0>
IP_HSn
IP_VSn
IP_VID<7..0>
PLX_CS1*
PLX_WR*
PLX_CS0*
PLX_LWR_RD*
PLX_CS1n
PLX_LWRn
PLX_CS0n
PLX_LWR_RDn
PLX_ADR<23..2>
PLX_LD<15..0>
PLX_LA<23..2>
PLX_LD<15..0>
PLX_CS2*
EPP_IOCHRDY*
EPP_IRQ*
PLX_CS2n
EPP_IOCHRDYn
EPP_IRQn
TV_PLX_LRDYn
PLX_LRDY*
EPP_PLX_LRDYn
PLX_LINT2*
PLX_LINT2n
VGA_HD
VGA_VD
VGA_CS
RAM1_CASn
RAM1_RASn
RAM1_WEn
RAMX_CSn
RAM1_DQM
RAM1_BANK
RAM1_A<11..0>
RAM1_DQ<15..0>
U33
SDRAM_64MBIT
CLK
CKE
CAS
RAS
WE
CS
UDQM
LDQM
BA1
BA0
A12
A11
A10
A09
A08
A07
A06
A05
A04
A03
A02
A01
A00
DQ15
DQ14
DQ13
DQ12
DQ11
DQ10
DQ09
DQ08
DQ07
DQ06
DQ05
DQ04
DQ03
DQ02
DQ01
DQ00
R112 10K
R111 10K
U35
485506
WCK
RSTW
WE
MD
RCK
RSTR
RE
OE
DIN15 DOUT15
DIN14 DOUT14
DIN13 DOUT13
DIN12 DOUT12
DIN11 DOUT11
DIN10 DOUT10
DIN9 DOUT9
DIN8 DOUT8
DIN7 DOUT7
DIN6 DOUT6
DIN5 DOUT5
DIN4 DOUT4
DIN3 DOUT3
DIN2 DOUT2
DIN1 DOUT1
DIN0 DOUT0
R113 10K
DEL_VID<7..0>
DAC_CSn
DAC_CBn
DAC_VID<7..0>
RSTWn
RSTRn
IP_VID_OUT<7..0>
TV_RSTR*
TV_RSTW*
RAM2_CASn
RAM2_RASn
RAM2_WEn
RAM2_DQM
RAM2_BANK
RAM2_A<11..0>
RAM2_DQ<15..0>
U34
U7
BT121
VAA1
VAA0
GND7
GND6
GND5
GND4
GND3
GND2
GND1
GND0
GND8
SYNC
BLANK
VREF
FS_ADJ
COMP
CLK
IOR
IOG
IOB
R7
R6
R5
R4
R3
R2
R1
R0
G7
G6
G5
G4
G3
G2
G1
G0
B7
B6
B5
B4
B3
B2
B1
B0
C32 0.1
R78 511
R54 15
R58 75
C151 0.01
C171 0.1
C173 0.1
R18 1K
R79 75
R80 75
R13 75
R56 75
+5V
-5V
U6
MAX499
CS
CEN
LE
A0
IN3B
IN3A
IN2B
IN2A
IN1B
IN1A
OUT3
OUT2
OUT1
GND
C122 0.01
C121 0.1
C150 0.01
C149 0.01
TV MONITOR VIDEO
TP11
WHT
CR6
CR5
CR4
P12
P13
P14
R16 75
R17 75
R20 75

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OEC MEDICAL SYSTEMS, INC.

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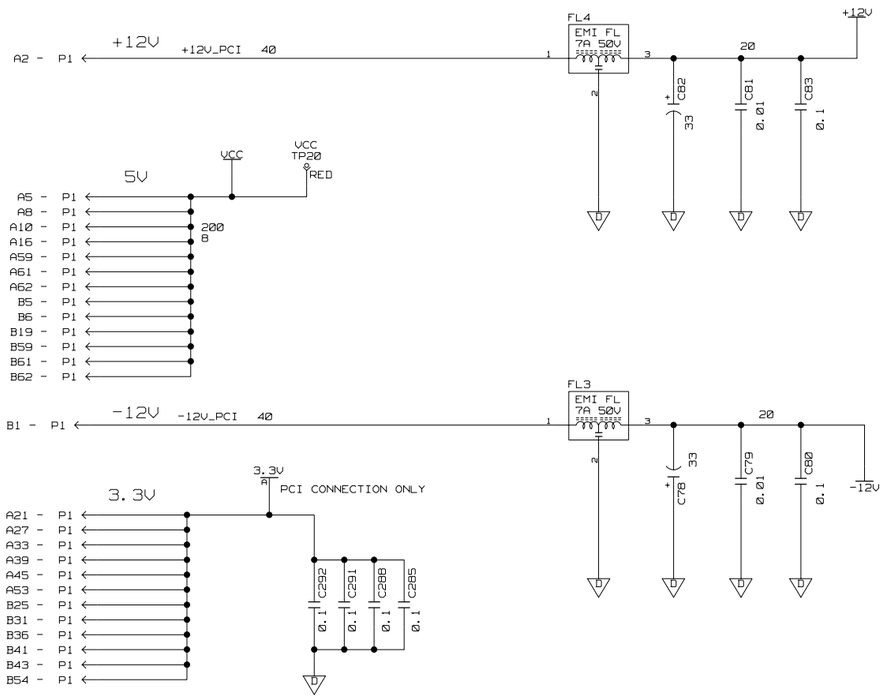
POWER ENTRY, BYPASS, AND FILTERING

PCI BUS CONNECTOR



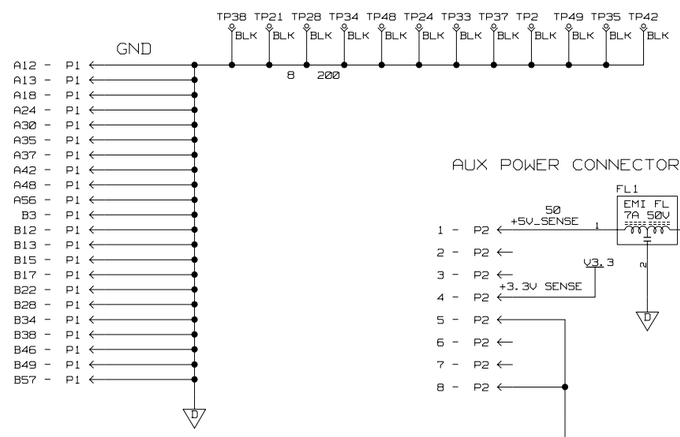
REFERENCE DESIGNATIONS

HIGHEST	UNUSED
C292	C91-C99
CR12	
DS2	
E1	
FL4	
L6	
P16	
R125	
TP49	
U36	
VR4	
XE2	
Y1	

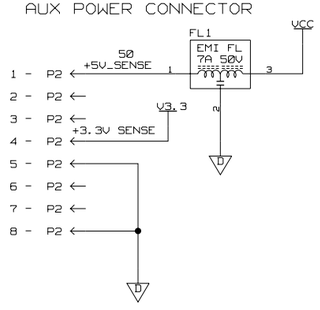
NOTE 1
THESE PARTS ARE NOT INSTALLED
CR12
E1
P10, P15, P16
R69, R70, R71, R72, R83, R84, R85, R122
U17
VR3, VR4

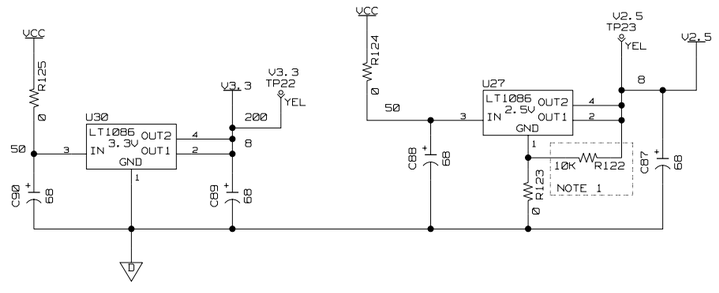
REF DES	DEVICE	2.5V	3.3V	+5V	-5V	+12V	-12V	AGND	GND
U1	7805			3		1			2
U2, 9	78L05			1		8			2, 3, 6, 7
U3	7905				3		2		1
U4, 10	TVP3030			29, 30,					27, 28, 68, 89, 93, 95,
				67, 90,					97, 99, 108, 109, 110,
				153, 174					111, 154, 172, 173
U5, 6, 8	MAX499			6, 18	7, 17				2, 4, 9, 11, 24
U7	BT121VCC			32, 33					4, 5, 16, 17, 27, 28, 29,
									30, 31
U11	49FCT3805		1, 20						5, 8, 16
U12, 14	74LCX16374		7, 18, 31						4, 10, 15, 21, 28, 34,
									39, 45
U13	EPC1LC20			18, 20					10
U15	EPC2			18, 20					10
U16	74ABT240			20					10
U17	CA3246							2, 4	
U18, 30, 15	49FCT805			1, 20					5, 8, 16
U18, 19	EPF10KEFC484	C11, C15, H14,							A1, A8, A22, B1, B2, B17,
		J8, J10, J12,							B21, B22, C2, C21, E21,
		J15, L9, L10,							G3, G21, H2, H8, H15, J9,
		L13, M10, M13,							J14, J20, K3, K10, K12,
		M14, N12, P8,							K13, L11, L12, M11, M12,
		P10, P12, P15,							M20, N10, N13, P9, P14,
		R14, V5, W21,							R8, R15, R22, T1, V3,
		Y8, AA12,							W11, W20, Y1, Y2, Y3,
									Y21, Y22, AA1, AA6,
									AA22, AB11, AB16
U20	EPF6016AQC208		8, 9, 26, 27,						7, 25,
			44, 45, 63, 79,						43, 62,
			96, 111, 112,						78, 95,
			130, 131, 148,						110, 129,
			149, 166, 183,						147, 165,
			200						182, 199
U21	5T78C36			44					23, 30
U22	NM93CS46			8					5
U23-26, 28,	SDRAM_64MBIT		1, 3, 9, 14, 27,						6, 12, 28,
29, 31-34			43, 49						41, 46,
									52, 54
U27	LT1086(2.5V)			3				2, 4	1
U30	LT1086(3.3V)		2, 4	3					1
U35	485506			14, 31					11, 34
U36	PCI9050			1, 10, 27,					9, 26, 40, 51, 65, 80,
				41, 50,					104, 120, 147, 160
				66, 81,					
				103, 121,					
				146					

GND TEST POINTS



AUX POWER CONNECTOR





00-881445-01 SCH, PCB, DISPLAY ADAPTER, 9800

00-881446-01 PCB, DISPLAY ADAPTER, A/F, 9800

00-881447-60 SPEC, PERF, DISPLAY ADAPTER PCA, 9800

00-881726-01 ASM, FW, U15, DSPLY APTR, 9800

00-881728-01 ASM, FW, U13, DSPLY APTR, 9800

00-881730-01 ASM, FW, PLX, DSPLY APTR, 9800

00-901419-01 BRKT, ISA, DSUB CUTOUT

22-399900-00 BRKT, CONN MTG, D-TYPE, .035 THK, SBN

51-500507-00 HDW KIT, CONN, JK SKT SET, 4-40 .50L

13-311104-00 NUT, HEX-LK-EXT-T, 4-40, SST, NA, A-.250

12-225104-05 SCR, SEMS SPR, PAN, TRX, 4-40, 5/16, SZC

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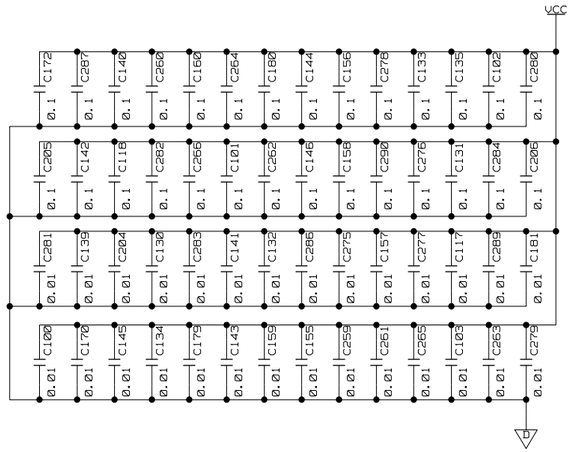

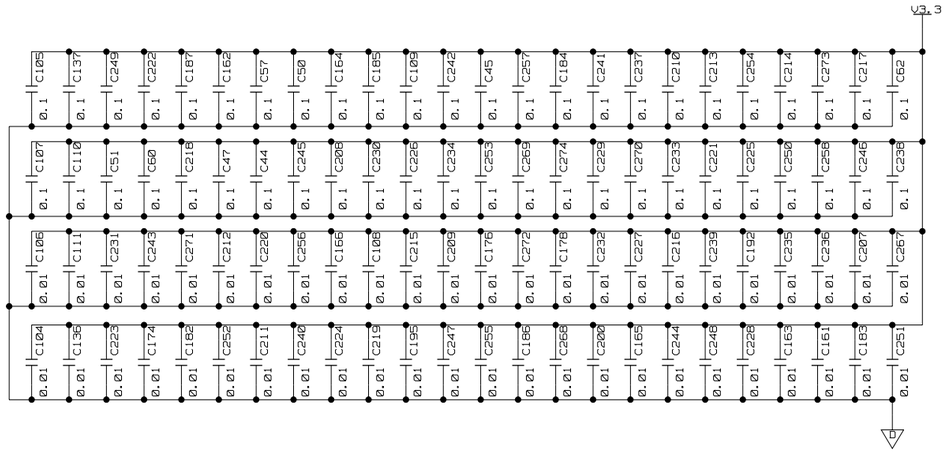

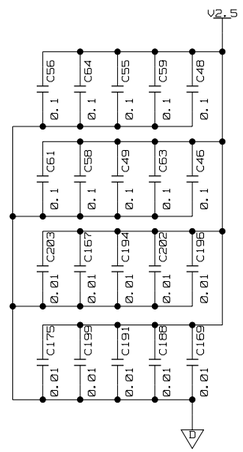

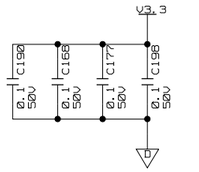

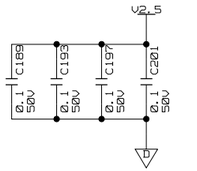

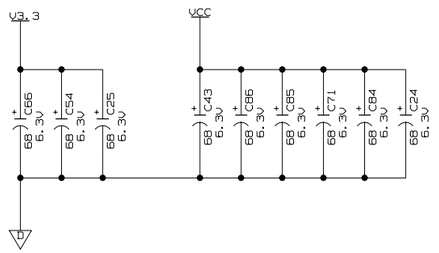

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C/BE<3..0>*\I

U36

SPEED=33_MHZ

PCI9050_32BIT

LA<27..2>\I

LAD<31..0>\I

AD<31..0>\I

LBE<3..0>*\I

PLX9050

DRAWING

LAST_MODIFIED=Wed Mar 31 10:57:12 1999

OEC MEDICAL SYSTEMS, INC.

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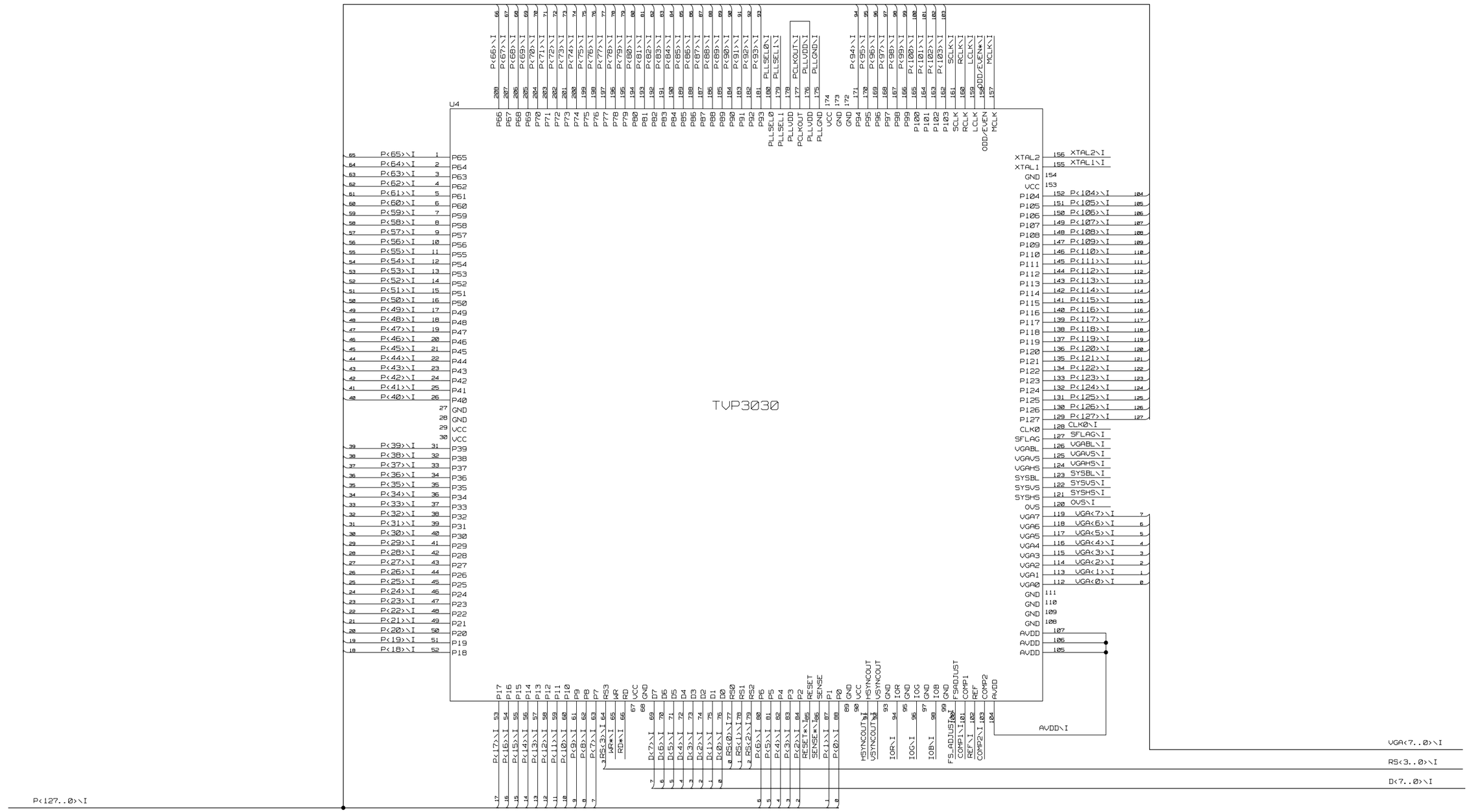

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OEC MEDICAL SYSTEMS, INC.

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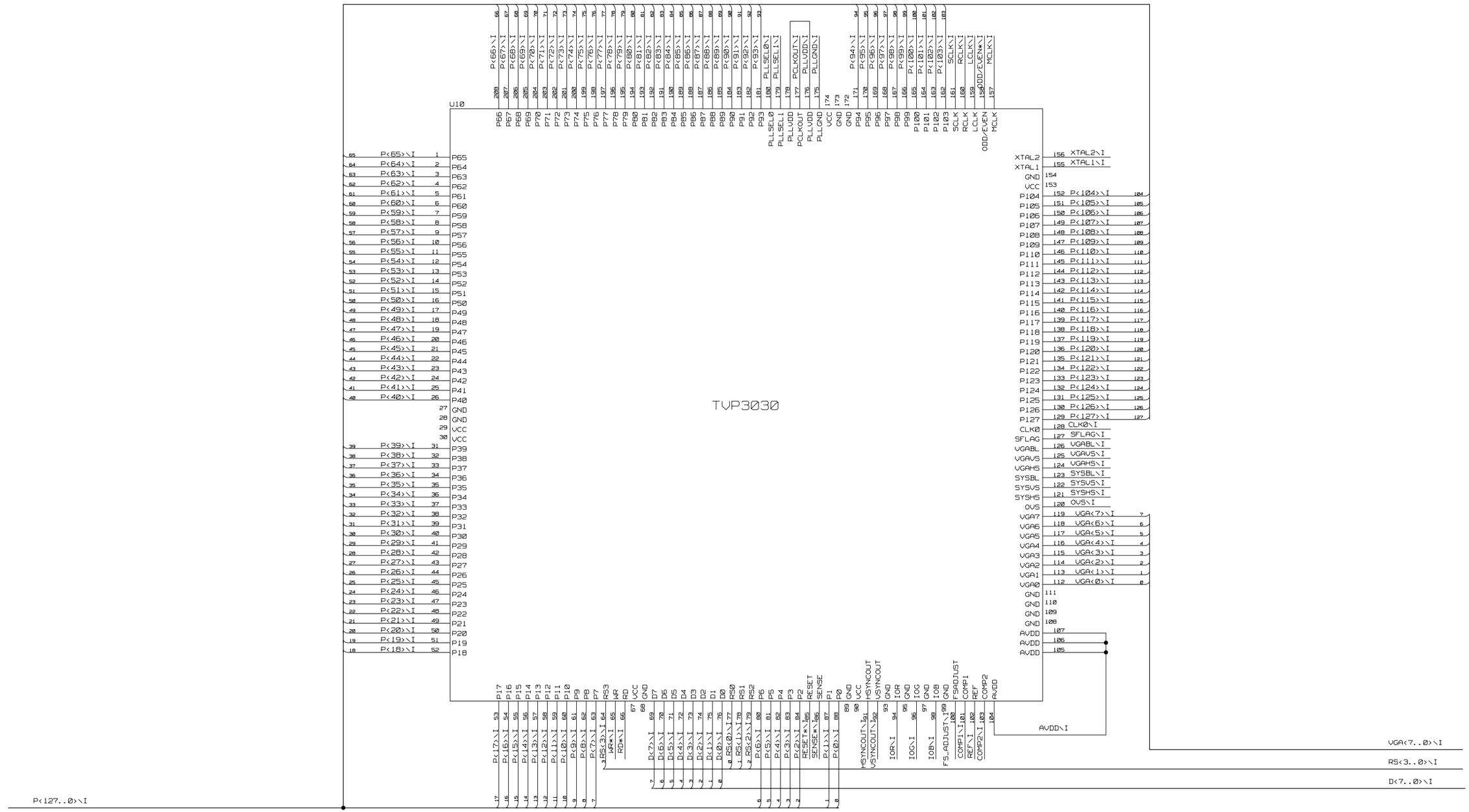

DRAWING

LAST_MODIFIED=Wed Mar 31 10:59:32 1999

OEC MEDICAL SYSTEMS, INC.

SIZE	DWG NO.	REV
D	00-881445	A

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IP_VID<7..0>\I
7 IP_VID<7>\I
6 IP_VID<6>\I
5 IP_VID<5>\I
4 IP_VID<4>\I
3 IP_VID<3>\I
2 IP_VID<2>\I
1 IP_VID<1>\I
0 IP_VID<0>\I

PLX_BEn<3..0>\I
3 PLX_BEN<3>\I
2 PLX_BEN<2>\I
1 PLX_BEN<1>\I
0 PLX_BEN<0>\I

SR_BA<1..0>\I
1 SR_BA<1>\I
0 SR_BA<0>\I

MR_BA<1..0>\I
1 MR_BA<1>\I
0 MR_BA<0>\I

SR_DQM<3..0>\I
3 SR_DQM<3>\I
2 SR_DQM<2>\I
1 SR_DQM<1>\I
0 SR_DQM<0>\I

MR_DQM<3..0>\I
3 MR_DQM<3>\I
2 MR_DQM<2>\I
1 MR_DQM<1>\I
0 MR_DQM<0>\I

PLX_ADR<23..2>\I
23 PLX_ADR<23>\I
22 PLX_ADR<22>\I
21 PLX_ADR<21>\I
20 PLX_ADR<20>\I
19 PLX_ADR<19>\I
18 PLX_ADR<18>\I
17 PLX_ADR<17>\I
16 PLX_ADR<16>\I
15 PLX_ADR<15>\I
14 PLX_ADR<14>\I
13 PLX_ADR<13>\I
12 PLX_ADR<12>\I
11 PLX_ADR<11>\I
10 PLX_ADR<10>\I
9 PLX_ADR<9>\I
8 PLX_ADR<8>\I
7 PLX_ADR<7>\I
6 PLX_ADR<6>\I
5 PLX_ADR<5>\I
4 PLX_ADR<4>\I
3 PLX_ADR<3>\I
2 PLX_ADR<2>\I

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SPEED=3
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	A10	A10	
SR_ADR<6>\I	A16	A16	
SR_ADR<7>\I	A17	A17	
DAC_VID<6>\I	A18	A18	
DAC_VID<2>\I	A19	A19	
SR_DQ<20>\I	B6	B6	
MR_DQ<10>\I	B7	B7	
MR_BA<0>\I	B8	B8	
OUT_SYNC_RESET\I	B11	B11	
PLX_CS1n\I	B13	B13	
PLX_ADR<16>\I	B14	B14	
OUTFI_RDREQ\I	B15	B15	
MR_DQ<18>\I	B18	B18	
SR_DQ<12>\I	C3	C3	
SR_DQ<9>\I	C4	C4	
PLX_ADR<13>\I	C5	C5	
PLX_ADR<9>\I	C7	C7	
IP_VID<1>\I	C8	C8	
DAC_VID<0>\I	C18	C18	
SR_ADR<9>\I	C19	C19	
DAC_VID<4>\I	C20	C20	
DATA\I	D4	DATA0	
MR_BA<1>\I	D5	D5	
PLX_DB<11>\I	D6	D6	
MR_DQ<7>\I	D7	D7	
PLX_ADR<11>\I	D8	D8	
PLX_DB<7>\I	D9	D9	
	D10	D10	
COMP_RUN\I	D11	D11	
DAC_RCLK\I	D12	D12	
PLX_DB<29>\I	D13	D13	
MR_ADR<2>\I	D14	D14	
SR_ADR<10>\I	D15	D15	
MR_ADR<3>\I	D16	D16	
DAC_VID<8>\I	D17	D17	
SR_ADR<5>\I	D18	D18	
DAC_VID<13>\I	D19	D19	
PLX_DB<25>\I	D22	D22	
CEn\I	E4	nCE	
DCLK\I	E5	DCLK	
SR_DQ<11>\I	E6	E6	
PLX_DB<10>\I	E7	E7	
MR_DQ<16>\I	E8	E8	
MR_DQ<11>\I	E9	E9	
	E10	E10	
MR_DQ<6>\I	E11	E11	
PLX_CS0n\I	E12	E12	
IP_VID<3>\I	E13	E13	
VGA_SEL\I	E14	E14	
SR_ADR<0>\I	E15	E15	
MR_ADR<6>\I	E16	E16	
SR_ADR<8>\I	E17	E17	
TCK\I	E18	TCK	
CEOn\I	E19	nCEO	
	F3	F3	PLX_DB<23>\I
	F4	F4	PLX_DB<24>\I
	F5	TDI	TDI\I
	F6	F6	
	F7	F7	MR_DQ<1>\I
	F8	F8	SR_DQ<4>\I
	F9	F9	PLX_DB<30>\I
	F10	F10	PLX_DB<9>\I
	F11	F11	
	F12	F12	DEV_OE\I
	F13	F13	VID_MD_REQ\I
	F14	F14	DAC_RESETn\I
	F15	F15	
	F16	F16	PLX_DB<6>\I
	F17	F17	SR_CASn\I
	F18	CONF_DONE	CONF_DONE\I
	F19	TDO	TDO\I
	F22	F22	DAC_VID<25>\I
	G4	G4	PLX_DB<22>\I
	G5	G5	DAC_VID<9>\I
	G6	G6	DAC_VID<22>\I
	G7	G7	SR_DQ<3>\I
	G8	G8	SR_DQ<7>\I
	G9	G9	
	G10	G10	PLX_DB<28>\I
	G11	G11	DEV_CLRn\I
	G12	G12	PLX_ADR<17>\I
	G13	G13	SR_ADR<4>\I
	G14	G14	SR_DQM<2>\I
	G16	G16	MSFI_RDREQ\I
	G17	G17	MR_DQ<15>\I
	G18	G18	SR_DQ<15>\I
	G19	G19	DAC_VID<26>\I
	H1	H1	DAC_BLANKn\I
	H3	H3	IP_COMP_ACTIVE\I
	H4	H4	DAC_VID<24>\I
	H5	H5	DAC_VID<19>\I
	H6	H6	PLX_DB<1>\I
	H7	H7	MR_DQ<4>\I
	H10	H10	MR_DQ<2>\I
	H11	H11	PLX_ADR<2>\I
	H12	H12	PLX_ADR<14>\I
	H13	H13	PLX_DB<4>\I
	H16	H16	PLX_DB<2>\I
	H17	H17	PLX_DB<0>\I
	H18	H18	DACFI_WRREQ\I
	H19	H19	DAC_VID<16>\I
	H21	H21	SR_DQ<26>\I
	H22	H22	DAC_VID<27>\I
	J4	J4	SR_DQ<18>\I
	J5	J5	SR_DQ<22>\I
	J6	J6	DAC_VID<21>\I
	J7	J7	SR_ADR<3>\I
	J16	J16	DAC_VID<23>\I
	J17	J17	DAC_VID<20>\I

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SR_DQ<23>\I	J18	J18	
SR_DQ<28>\I	J19	J19	
SR_DQ<27>\I	J22	J22	
OUTFI_WRREQ\I	K1	K1	
MR_DQ<23>\I	K4	K4	
MR_DQ<12>\I	K5	K5	
IP_VID<2>\I	K6	K6	
SR_DQ<21>\I	K7	K7	
SR_DQ<19>\I	K8	K8	
SR_DQ<24>\I	K15	K15	
SR_DQ<25>\I	K16	K16	
IP_VID<7>\I	K17	K17	
IP_VID<4>\I	K18	K18	
MR_DQ<20>\I	K19	K19	
MR_DQ<26>\I	K21	K21	
SR_DQ<31>\I	L3	L3	
MSFI_WRREQ\I	L4	L4	
MR_ADR<9>\I	L5	L5	
IP_VSn\I	L6	L6	
MR_DQ<31>\I	L7	L7	
MR_DQ<28>\I	L8	L8	
MR_ADR<7>\I	L15	L15	
IP_HSn\I	L16	L16	
DAC_VID<31>\I	L17	L17	
MR_ADR<10>\I	L18	L18	
INFI_WRREQ\I	L19	L19	
DAC_VID<11>\I	L21	L21	
MR_DQ<13>\I	M1	M1	
MR_DQ<17>\I	M4	M4	
DAC_VID<10>\I	M5	M5	
SR_DQ<0>\I	M6	M6	
PLX_BEn<0>\I	M7	M7	
DAC_VID<7>\I	M8	M8	
PLX_LRDYn\I	M15	M15	
PLX_BEn<2>\I	M16	M16	
PLX_BEn<3>\I	M17	M17	
MR_DQ<5>\I	M18	M18	
IP_PXLWRn\I	M19	M19	
PLX_BEn<1>\I	M21	M21	
PLX_DB<12>\I	N4	N4	
DAC_VID<12>\I	N5	N5	
PLX_DB<14>\I	N6	N6	
DAC_LCLK\I	N7	N7	
SR_DQ<17>\I	N8	N8	
DAC_VID<1>\I	N15	N15	
PLX_DB<20>\I	N16	N16	
PLX_DB<19>\I	N17	N17	
PLX_DB<18>\I	N18	N18	
PLX_DB<21>\I	N19	N19	
SR_DQ<16>\I	P1	P1	
PLX_DB<13>\I	P2	P2	
SR_BA<1>\I	P4	P4	
SR_DQ<14>\I	P5	P5	
	P6	P6	SR_DQ<6>\I
	P7	P7	MR_DQ<22>\I
	P11	P11	IP_CLK\I
	P16	P16	MR_CASn\I
	P17	P17	SR_DQ<2>\I
	P18	P18	SR_DQ<1>\I
	P19	P19	SR_DQ<5>\I
	R4	R4	MR_DQ<27>\I
	R5	R5	MR_DQ<29>\I
	R6	R6	MR_DQ<30>\I
	R7	R7	MR_DQ<24>\I
	R10	R10	
	R11	R11	DACFI_RDREQ\I
	R12	R12	PLX_LWR_RDn\I
	R13	R13	MR_RASn\I
	R16	R16	SR_ADR<11>\I
	R17	R17	IP_VID<6>\I
	R18	R18	MR_DQ<19>\I
	R19	R19	IP_VID<5>\I
	R20	R20	MR_DQ<25>\I
nCONFIG	T4	T4	DAC_VID<18>\I
	T5	T5	DAC_VID<29>\I
	T6	T6	DAC_VID<17>\I
	T7	T7	CONFIGn\I
	T8	T8	PLX_ADR<10>\I
	T9	T9	MR_DQ<9>\I
	T10	T10	PLX_DB<5>\I
	T11	T11	
	T12	T12	PLX_ADR<20>\I
	T13	T13	SR_ADR<2>\I
	T14	T14	PLX_ADR<15>\I
	T16	T16	DAC_VID<3>\I
	T17	T17	MR_DQ<21>\I
	T18	T18	DAC_VID<15>\I
	T19	T19	PLX_ADR<4>\I
MSEL0	U4	U4	MSEL0\I
	U5	U5	DAC_VID<30>\I
	U6	U6	PLX_DB<8>\I
	U7	U7	MR_DQM<3>\I
	U8	U8	PLX_DB<15>\I
	U9	U9	PLX_ADR<12>\I
	U10	U10	
	U11	U11	DAC_HSn\I
	U12	U12	PLX_ADR<23>\I
	U13	U13	PLX_ADR<22>\I
	U14	U14	SR_DQM<3>\I
	U15	U15	MR_ADR<8>\I
	U16	U16	INFI_RDREQ\I
	U17	U17	PLX_ADR<3>\I
TMS	U18	U18	TMS\I
	U19	U19	DAC_VID<28>\I
	V1	V1	PLX_ADR<5>\I
MSEL1	V4	V4	MSEL1\I
	V6	V6	PLX_ADR<19>\I

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PLX_DB<16>\I	V7	V7	
	V8	V8	
PLX_DB<31>\I	V9	V9	
MR_DQ<3>\I	V10	V10	
LFT_RHTn\I	V11	V11	
	V12	V12	
PLX_WRn\I	V13	V13	
DAC_VID<5>\I	V14	V14	
	V15	V15	
MR_DQM<2>\I	V16	V16	
SR_BA<0>\I	V17	V17	
DAC_RDn\I	V18	V18	
TRSTn\I	V19	nTRST	
DAC_VID<14>\I	V21	V21	
SR_DQ<8>\I	W3	W3	
SR_DQ<13>\I	W4	W4	
MR_DQM<0>\I	W5	W5	
SR_DQ<10>\I	W6	W6	
PLX_ADR<6>\I	W7	W7	
PLX_ADR<8>\I	W8	W8	
PLX_DB<3>\I	W9	W9	
	W10	W10	
PLX_ADR<21>\I	W12	W12	
PLX_RDn\I	W13	W13	
SR_DQM<1>\I	W14	W14	
TP_LED\I	W15	W15	
MR_DQ<14>\I	W16	W16	
MR_ADR<0>\I	W17	W17	
DAC_WRn\I	W18	W18	
STATUSn\I	W19	nSTATUS	
MRSR_CSn\I	Y5	Y5	
PLX_ADR<7>\I	Y6	Y6	
PLX_DB<17>\I	Y7	Y7	
PLX_DB<27>\I	Y10	Y10	
MR_DQ<0>\I	Y11	Y11	
MR_ADR<1>\I	Y14	Y14	
SR_RASn\I	Y15	Y15	
MR_WEn\I	Y17	Y17	
SR_WEn\I	Y18	Y18	
MR_DQ<8>\I	AA5	AA5	
SR_DQ<30>\I	AA7	AA7	
DAC_VSn\I	AA8	AA8	
SR_DQ<29>\I	AA10	AA10	
SR_ADR<1>\I	AA14	AA14	
MR_ADR<11>\I	AA16	AA16	
MR_ADR<5>\I	AA17	AA17	
SR_DQM<0>\I	AA18	AA18	
MR_ADR<4>\I	AA19	AA19	
PLX_DB<26>\I	AA20	AA20	
PLX_ADR<18>\I	AB6	AB6	
MR_DQM<1>\I	AB10	AB10	
IP_VID<0>\I	AB14	AB14	
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	A6	VCCIO	A6
	A13	VCCIO	A13
	B5	VCCIO	B5
	E1	VCCIO	E1
	G1	VCCIO	G1
	G15	VCCIO	G15
	H9	VCCIO	H9
	H20	VCCIO	H20
	J11	VCCIO	J11
	J13	VCCIO	J13
	K9	VCCIO	K9
	K11	VCCIO	K11
	K14	VCCIO	K14
	K20	VCCIO	K20
	L14	VCCIO	L14
	M9	VCCIO	M9
	N3	VCCIO	N3
	N9	VCCIO	N9
	N11	VCCIO	N11
	N14	VCCIO	N14
	N20	VCCIO	N20
	P13	VCCIO	P13
	R1	VCCIO	R1
	R9	VCCIO	R9
	T3	VCCIO	T3
	T15	VCCIO	T15
	T22	VCCIO	T22
	V22	VCCIO	V22
	AB13	VCCIO	AB13

MR_ADR<11..0>\I
11 MR_ADR<11>\I
10 MR_ADR<10>\I
9 MR_ADR<9>\I
8 MR_ADR<8>\I
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6 MR_ADR<6>\I
5 MR_ADR<5>\I
4 MR_ADR<4>\I
3 MR_ADR<3>\I
2 MR_ADR<2>\I
1 MR_ADR<1>\I
0 MR_ADR<0>\I

SR_ADR<11..0>\I
11 SR_ADR<11>\I
10 SR_ADR<10>\I
9 SR_ADR<9>\I
8 SR_ADR<8>\I
7 SR_ADR<7>\I
6 SR_ADR<6>\I
5 SR_ADR<5>\I
4 SR_ADR<4>\I
3 SR_ADR<3>\I
2 SR_ADR<2>\I
1 SR_ADR<1>\I
0 SR_ADR<0>\I

PLX_DB<31..0>\I
31 PLX_DB<31>\I
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2 PLX_DB<2>\I
1 PLX_DB<1>\I
0 PLX_DB<0>\I

MR_DQ<31..0>\I
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4 MR_DQ<4>\I
3 MR_DQ<3>\I
2 MR_DQ<2>\I
1 MR_DQ<1>\I
0 MR_DQ<0>\I

SR_DQ<31..0>\I
31 SR_DQ<31>\I
30 SR_DQ<30>\I
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DAC_VID<31..0>\I
31 DAC_VID<31>\I
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9 DAC_VID<9>\I
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6 DAC_VID<6>\I
5 DAC_VID<5>\I
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3 DAC_VID<3>\I
2 DAC_VID<2>\I
1 DAC_VID<1>\I
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LEFT VIDEO CONTROL

DRAWING

LAST_MODIFIED=Wed Mar 31 10:55:10 1999

OEC MEDICAL SYSTEMS, INC.

SIZE	DWG NO.	REV
D	00-881445	A

SCALE: | SHEET 14 OF 19

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IP_VID<7..0>\I
- 7 IP_VID<7>\I
- 6 IP_VID<6>\I
- 5 IP_VID<5>\I
- 4 IP_VID<4>\I
- 3 IP_VID<3>\I
- 2 IP_VID<2>\I
- 1 IP_VID<1>\I
- 0 IP_VID<0>\I

PLX_BEn<3..0>\I
- 3 PLX_BEN<3>\I
- 2 PLX_BEN<2>\I
- 1 PLX_BEN<1>\I
- 0 PLX_BEN<0>\I

SR_BA<1..0>\I
- 1 SR_BA<1>\I
- 0 SR_BA<0>\I

MR_BA<1..0>\I
- 1 MR_BA<1>\I
- 0 MR_BA<0>\I

SR_DQM<3..0>\I
- 3 SR_DQM<3>\I
- 2 SR_DQM<2>\I
- 1 SR_DQM<1>\I
- 0 SR_DQM<0>\I

MR_DQM<3..0>\I
- 3 MR_DQM<3>\I
- 2 MR_DQM<2>\I
- 1 MR_DQM<1>\I
- 0 MR_DQM<0>\I

PLX_ADR<23..2>\I
- 23 PLX_ADR<23>\I
- 22 PLX_ADR<22>\I
- 21 PLX_ADR<21>\I
- 20 PLX_ADR<20>\I
- 19 PLX_ADR<19>\I
- 18 PLX_ADR<18>\I
- 17 PLX_ADR<17>\I
- 16 PLX_ADR<16>\I
- 15 PLX_ADR<15>\I
- 14 PLX_ADR<14>\I
- 13 PLX_ADR<13>\I
- 12 PLX_ADR<12>\I
- 11 PLX_ADR<11>\I
- 10 PLX_ADR<10>\I
- 9 PLX_ADR<9>\I
- 8 PLX_ADR<8>\I
- 7 PLX_ADR<7>\I
- 6 PLX_ADR<6>\I
- 5 PLX_ADR<5>\I
- 4 PLX_ADR<4>\I
- 3 PLX_ADR<3>\I
- 2 PLX_ADR<2>\I

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A10	A10	F3	PLX_DB<23>\I
SR_ADR<6>\I	A16	F4	PLX_DB<24>\I
SR_ADR<7>\I	A17	TDI	TDI\I
DAC_VID<6>\I	A18	F6	
DAC_VID<2>\I	A19	F7	MR_DQ<1>\I
		F8	SR_DQ<4>\I
SR_DQ<20>\I	B6	F9	PLX_DB<30>\I
MR_DQ<10>\I	B7	F10	PLX_DB<9>\I
MR_BA<0>\I	B8	F11	
OUT_SYNC_RESET\I	B11	F12	DEV_OE\I
PLX_CS1n\I	B13	F13	VID_MD_REQ\I
PLX_ADR<16>\I	B14	F14	DAC_RESETn\I
OUTFI_RDREQ\I	B15	F15	
MR_DQ<18>\I	B18	F16	PLX_DB<6>\I
		F17	SR_CASn\I
SR_DQ<12>\I	C3	CONF_DONE	CONF_DONE\I
SR_DQ<9>\I	C4	TDO	TDO\I
PLX_ADR<13>\I	C5	F22	DAC_VID<25>\I
PLX_ADR<9>\I	C7		
IP_VID<1>\I	C8	G4	PLX_DB<22>\I
DAC_VID<0>\I	C18	G5	DAC_VID<9>\I
SR_ADR<9>\I	C19	G6	DAC_VID<22>\I
DAC_VID<4>\I	C20	G7	SR_DQ<3>\I
		G8	SR_DQ<7>\I
DATA\I	D4	G9	
MR_BA<1>\I	D5	G10	PLX_DB<28>\I
PLX_DB<11>\I	D6	G11	DEV_CLRn\I
MR_DQ<7>\I	D7	G12	PLX_ADR<17>\I
PLX_ADR<11>\I	D8	G13	SR_ADR<4>\I
PLX_DB<7>\I	D9	G14	SR_DQM<2>\I
	D10	G16	MSFI_RDREQ\I
COMP_RUN\I	D11	G17	MR_DQ<15>\I
DAC_RCLK\I	D12	G18	SR_DQ<15>\I
PLX_DB<29>\I	D13	G19	DAC_VID<26>\I
MR_ADR<2>\I	D14		
SR_ADR<10>\I	D15	H1	DAC_BLANKn\I
MR_ADR<3>\I	D16	H3	IP_COMP_ACTIVE\I
DAC_VID<8>\I	D17	H4	DAC_VID<24>\I
SR_ADR<5>\I	D18	H5	DAC_VID<19>\I
DAC_VID<13>\I	D19	H6	PLX_DB<1>\I
PLX_DB<25>\I	D22	H7	MR_DQ<4>\I
		H10	MR_DQ<2>\I
CEn\I	E4	H11	PLX_ADR<2>\I
DCLK\I	E5	H12	PLX_ADR<14>\I
SR_DQ<11>\I	E6	H13	PLX_DB<4>\I
PLX_DB<10>\I	E7	H16	PLX_DB<2>\I
MR_DQ<16>\I	E8	H17	PLX_DB<0>\I
MR_DQ<11>\I	E9	H18	DACFI_WRREQ\I
	E10	H19	DAC_VID<16>\I
MR_DQ<6>\I	E11	H21	SR_DQ<26>\I
PLX_CS0n\I	E12	H22	DAC_VID<27>\I
IP_VID<3>\I	E13		
VGA_SEL\I	E14	J4	SR_DQ<18>\I
SR_ADR<0>\I	E15	J5	SR_DQ<22>\I
MR_ADR<6>\I	E16	J6	DAC_VID<21>\I
SR_ADR<8>\I	E17	J7	SR_ADR<3>\I
TCK\I	E18	J16	DAC_VID<23>\I
CEO\I	E19	J17	DAC_VID<20>\I

		nCE	nCE
		DCLK	DCLK
		E6	E6
		E7	E7
		E8	E8
		E9	E9
		E10	E10
		E11	E11
		E12	E12
		E13	E13
		E14	E14
		E15	E15
		E16	E16
		E17	E17
		TCK	TCK
		nCEO	J17

PACK_TYPE=PBGAVIA

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SECTION 2 of 3

SR_DQ<23>\I	J18	P6	SR_DQ<6>\I
SR_DQ<28>\I	J19	P7	MR_DQ<22>\I
SR_DQ<27>\I	J22	P11	IP_CLK\I
		P16	MR_CASn\I
OUTFI_WRREQ\I	K1	P17	SR_DQ<2>\I
MR_DQ<23>\I	K4	P18	SR_DQ<1>\I
MR_DQ<12>\I	K5	P19	SR_DQ<5>\I
IP_VID<2>\I	K6		
SR_DQ<21>\I	K7	R4	MR_DQ<27>\I
SR_DQ<19>\I	K8	R5	MR_DQ<29>\I
SR_DQ<24>\I	K15	R6	MR_DQ<30>\I
SR_DQ<25>\I	K16	R7	MR_DQ<24>\I
IP_VID<7>\I	K17	R10	
IP_VID<4>\I	K18	R11	DACFI_RDREQ\I
MR_DQ<20>\I	K19	R12	PLX_LWR_RDn\I
MR_DQ<26>\I	K21	R13	MR_RASn\I
		R16	SR_ADR<11>\I
SR_DQ<31>\I	L3	R17	IP_VID<6>\I
MSFI_WRREQ\I	L4	R18	MR_DQ<19>\I
MR_ADR<9>\I	L5	R19	IP_VID<5>\I
IP_VSn\I	L6	R20	MR_DQ<25>\I
MR_DQ<31>\I	L7		
MR_DQ<28>\I	L8	T4	DAC_VID<18>\I
MR_ADR<7>\I	L15	T5	DAC_VID<29>\I
IP_HSn\I	L16	T6	DAC_VID<17>\I
DAC_VID<31>\I	L17	nCONFIG	CONFIGn\I
MR_ADR<10>\I	L18	T8	PLX_ADR<10>\I
INFI_WRREQ\I	L19	T9	MR_DQ<9>\I
DAC_VID<11>\I	L21	T10	PLX_DB<5>\I
		T11	
MR_DQ<13>\I	M1	T12	PLX_ADR<20>\I
MR_DQ<17>\I	M4	T13	SR_ADR<2>\I
DAC_VID<10>\I	M5	T14	PLX_ADR<15>\I
SR_DQ<0>\I	M6	T16	DAC_VID<3>\I
PLX_BEn<0>\I	M7	T17	MR_DQ<21>\I
DAC_VID<7>\I	M8	T18	DAC_VID<15>\I
PLX_LRDYn\I	M15	T19	PLX_ADR<4>\I
PLX_BEn<2>\I	M16		
PLX_BEn<3>\I	M17	MSEL0	MSEL0\I
MR_DQ<5>\I	M18	U5	DAC_VID<30>\I
IP_PXLWRn\I	M19	U6	PLX_DB<8>\I
PLX_BEn<1>\I	M21	U7	MR_DQM<3>\I
		U8	PLX_DB<15>\I
PLX_DB<12>\I	N4	U9	PLX_ADR<12>\I
DAC_VID<12>\I	N5	U10	U10
PLX_DB<14>\I	N6	U11	DAC_HSn\I
DAC_LCLK\I	N7	U12	PLX_ADR<23>\I
SR_DQ<17>\I	N8	U13	PLX_ADR<22>\I
DAC_VID<1>\I	N15	U14	SR_DQM<3>\I
PLX_DB<20>\I	N16	U15	MR_ADR<8>\I
PLX_DB<19>\I	N17	U16	INFI_RDREQ\I
PLX_DB<18>\I	N18	U17	PLX_ADR<3>\I
PLX_DB<21>\I	N19	TMS	TMS\I
		U19	DAC_VID<28>\I
SR_DQ<16>\I	P1		
PLX_DB<13>\I	P2	V1	PLX_ADR<5>\I
SR_BA<1>\I	P4	MSEL1	MSEL1\I
SR_DQ<14>\I	P5	V6	PLX_ADR<19>\I

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SECTION 3 of 3

PLX_DB<16>\I	V7	V7	
	V8	V8	
PLX_DB<31>\I	V9	V9	
MR_DQ<3>\I	V10	V10	
LFT_RHTn\I	V11	V11	
	V12	V12	
PLX_WRn\I	V13	V13	
DAC_VID<5>\I	V14	V14	
	V15	V15	
MR_DQM<2>\I	V16	V16	
SR_BA<0>\I	V17	V17	
DAC_RDn\I	V18	V18	
TRSTn\I	V19	nTRST	
DAC_VID<14>\I	V21	V21	
SR_DQ<8>\I	W3	W3	
SR_DQ<13>\I	W4	W4	
MR_DQM<0>\I	W5	W5	
SR_DQ<10>\I	W6	W6	
PLX_ADR<6>\I	W7	W7	
PLX_ADR<8>\I	W8	W8	
PLX_DB<3>\I	W9	W9	
	W10	W10	
PLX_ADR<21>\I	W12	W12	
PLX_RDn\I	W13	W13	
SR_DQM<1>\I	W14	W14	
TP_LED\I	W15	W15	
MR_DQ<14>\I	W16	W16	
MR_ADR<0>\I	W17	W17	
DAC_WRn\I	W18	W18	
STATUSn\I	W19	nSTATUS	
MRSR_CSn\I	Y5	Y5	
PLX_ADR<7>\I	Y6	Y6	
PLX_DB<17>\I	Y7	Y7	
PLX_DB<27>\I	Y10	Y10	
MR_DQ<0>\I	Y11	Y11	
MR_ADR<1>\I	Y14	Y14	
SR_RASn\I	Y15	Y15	
MR_WEn\I	Y17	Y17	
SR_WEn\I	Y18	Y18	
MR_DQ<8>\I	AA5	AA5	
SR_DQ<30>\I	AA7	AA7	
DAC_VSn\I	AA8	AA8	
SR_DQ<29>\I	AA10	AA10	
SR_ADR<1>\I	AA14	AA14	
MR_ADR<11>\I	AA16	AA16	
MR_ADR<5>\I	AA17	AA17	
SR_DQM<0>\I	AA18	AA18	
MR_ADR<4>\I	AA19	AA19	
PLX_DB<26>\I	AA20	AA20	
		AB6	
PLX_ADR<18>\I	AB6	AB10	
MR_DQM<1>\I	AB10	AB14	
IP_VID<0>\I	AB14		

		VCCIO	A6
		VCCIO	A13
		VCCIO	B5
		VCCIO	E1
		VCCIO	G1
		VCCIO	G15
		VCCIO	H9
		VCCIO	H20
		VCCIO	J11
		VCCIO	J13
		VCCIO	K9
		VCCIO	K11
		VCCIO	K14
		VCCIO	K20
		VCCIO	L14
		VCCIO	M9
		VCCIO	N3
		VCCIO	N9
		VCCIO	N11
		VCCIO	N14
		VCCIO	N20
		VCCIO	P13
		VCCIO	R1
		VCCIO	R9
		VCCIO	T3
		VCCIO	T15
		VCCIO	T22
		VCCIO	V22
		VCCIO	AB13

V3.3

MR_ADR<11..0>\I
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RIGHT VIDEO CONTROL

DRAWING

LAST_MODIFIED=Wed Mar 31 11:00:19 1999

OEC MEDICAL SYSTEMS, INC.

SIZE	DWG NO.	REV
D	00-881445	A

SCALE: | SHEET 15 OF 19

05-017-9-93

PLX_LA<23..2>\I
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- 1 IP_VID<1>\I
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IP_VID_OUT<7..0>\I
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RAM1_A<11..0>\I
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- 10 RAM1_A<10>\I
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RAM2_DQ<15..0>\I
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U20

EPF6016AQC208

SPEED=2

NOTE:

THIS COMPONENT BODY DRAWING IS NOT INTENDED FOR PRODUCTION SCHEMATIC USE.

PACK_TYPE=SQFPV33

		RAM1_BANK\I	208 P208
		IP_VID_OUT<1>\I	207 P207
		RSTR\I	206 P206
		RAM1_A<3>\I	205 P205
		PLX_LD<1>\I	204 P204
		PLX_LD<5>\I	203 P203
		PLX_LD<4>\I	202 P202
		PLX_LD<8>\I	201 P201
			200 VCCIO
			199 GND
		PLX_LD<11>\I	198 P198
		PLX_LD<10>\I	197 P197
		PLX_LD<15>\I	196 P196
		PLX_LD<14>\I	195 P195
		RAM1_DQ<2>\I	194 P194
		RAM1_DQ<1>\I	193 P193
		RAM1_DQ<6>\I	192 P192
		RAM1_DQ<5>\I	191 P191
		RAM1_DQ<9>\I	190 P190
		RAM1_DQ<12>\I	189 P189
		RAM1_DQ<11>\I	188 P188
		DEV_CLR\I	187 P187
		RAM2_DQ<2>\I	186 P186
		RAM2_DQ<1>\I	185 P185
		DCLK\I	184 DCLK
			183 VCCIO
			182 GND
		DATA\I	181 DATA0
		RAM2_DQ<5>\I	180 P180
		RAM2_DQ<7>\I	179 P179
		DEV_OE\I	178 P178
		RAM2_DQ<10>\I	177 P177
		RAM2_DQ<14>\I	176 P176
		RAM2_DQ<13>\I	175 P175
		PLX_LA<13>\I	174 P174
		IP_VID<3>\I	173 P173
		IP_VID<2>\I	172 P172
		TV_PLX_LRDY\I	171 P171
		PLX_LA<17>\I	170 P170
		PLX_LA<12>\I	169 P169
		RAM1_WE\I	168 P168
		RAM1_RAS\I	167 P167
			166 VCCIO
			165 GND
		RAM1_CAS\I	164 P164
		RAM1_A<0>\I	163 P163
			162 P162
		RAM1_A<10>\I	161 P161
		PLX_LA<10>\I	160 P160
		RSTWN\I	159 P159
		RAM2_A<0>\I	158 P158
		RAM2_A<8>\I	157 P157

IP_HSn\I	1	P1
RAM1_A<6>\I	2	P2
RAM1_A<1>\I	3	P3
RAM1_A<4>\I	4	P4
RAM1_A<9>\I	5	P5
CEn\I	6	nCE
	7	GND
	8	V33
	9	VCCIO
RAM1_A<7>\I	10	P10
RAM1_A<5>\I	11	P11
RAM2_A<11>\I	12	P12
RAM2_DQM\I	13	P13
RAM1_A<11>\I	14	P14
RAM1_DQM\I	15	P15
PLX_LA<14>\I	16	P16
DEL_VID<7>\I	17	P17
DEL_VID<6>\I	18	P18
TDI\I	19	TDI
DEL_VID<3>\I	20	P20
DEL_VID<0>\I	21	P21
DEL_VID<2>\I	22	P22
DEL_VID<1>\I	23	P23
CLK\I	24	IN/GCLK
	25	GND
	26	V33
	27	VCCIO
IP_VSn\I	28	IN/GCLK
VGA_HD\I	29	P29
VGA_VD\I	30	P30
RAMX_CSn\I	31	P31
IP_VID_OUT<6>\I	32	P32
IP_VID_OUT<2>\I	33	P33
IP_VID_OUT<3>\I	34	P34
IP_VID_OUT<0>\I	35	P35
VGA_CS\I	36	P36
RAM1_A<2>\I	37	P37
TMS\I	38	TMS
PLX_CS1n\I	39	P39
PLX_LA<9>\I	40	P40
PLX_LA<19>\I	41	P41
PLX_LA<18>\I	42	P42
	43	GND
	44	V33
	45	VCCIO
MSEL\I	46	MSEL
TCK\I	47	TCK
PLX_LA<22>\I	48	P48
PLX_LWR_RDn\I	49	P49
DAC_VID<4>\I	50	P50
PLX_CS0n\I	51	P51
PLX_LA<23>\I	52	P52

			P156 156
			P155 155
			P154 154
			P153 153
			P152 152
			P151 151
		CONF_DONE	150 CONF_DONE\I
			149 VCCIO
			148 V33
			147 GND
			146 P146
			145 P145
			144 P144
			143 P143
			142 P142
			141 P141
			140 P140
			139 P139
			138 P138
			137 P137
			136 P136
			135 P135
			134 P134
			133 P133
		IN/GCLK	132 IN/GCLK
			131 VCCIO
			130 V33
			129 GND
		IN/GCLK	128 IN/GCLK
			127 P127
			126 P126
			125 P125
			124 P124
			123 P123
			122 P122
			121 P121
			120 P120
			119 P119
			118 P118
			117 P117
			116 P116
			115 P115
			114 P114
			113 P113
			112 VCCIO
			111 V33
			110 GND
			109 P109
			108 P108
		TDO	107 TDO\I
			106 P106
			105 P105

			53 P53
			54 P54
			55 P55
			56 P56
			57 P57
			58 P58
			59 P59
			60 P60
			61 P61
			62 GND
			63 VCCIO
			64 P64
			65 P65
			66 P66
			67 P67
			68 P68
			69 P69
			70 P70
			71 P71
			72 P72
			73 P73
			74 P74
			75 P75
			76 P76
			77 nCONFIG
			78 GND
			79 VCCIO
			80 nSTATUS
			81 P81
			82 P82
			83 P83
			84 P84
			85 P85
			86 P86
			87 P87
			88 P88
			89 P89
			90 P90
			91 P91
			92 P92
			93 P93
			94 P94
			95 GND
			96 VCCIO
			97 P97
			98 P98
			99 P99
			100 P100
			101 P101
			102 P102
			103 P103
			104 P104

PLX_LA<21>\I	53	P53
DAC_VID<1>\I	54	P54
DAC_VID<2>\I	55	P55
DAC_VID<3>\I	56	P56
PLX_LD<0>\I	57	P57
PLX_LD<2>\I	58	P58
PLX_LD<3>\I	59	P59
PLX_LD<6>\I	60	P60
PLX_LD<7>\I	61	P61
	62	GND
	63	VCCIO
PLX_LD<9>\I	64	P64
PLX_LD<12>\I	65	P65
PLX_LD<13>\I	66	P66
RAM1_DQ<0>\I	67	P67
RAM1_DQ<3>\I	68	P68
RAM1_DQ<4>\I	69	P69
RAM1_DQ<7>\I	70	P70
RAM1_DQ<8>\I	71	P71
RAM1_DQ<10>\I	72	P72
RAM1_DQ<13>\I	73	P73
RAM1_DQ<14>\I	74	P74
RAM1_DQ<15>\I	75	P75
RAM2_DQ<0>\I	76	P76
CONFIGn\I	77	nCONFIG
	78	GND
	79	VCCIO
STATUSn\I	80	nSTATUS
RAM2_DQ<3>\I	81	P81
RAM2_DQ<4>\I	82	P82
RAM2_DQ<6>\I	83	P83
RAM2_DQ<8>\I	84	P84
RAM2_DQ<9>\I	85	P85
RAM2_DQ<11>\I	86	P86
RAM2_DQ<12>\I	87	P87
RAM2_DQ<15>\I	88	P88
PLX_LA<20>\I	89	P89
PLX_LA<11>\I	90	P90
EPP_PLX_LRDY\I	91	P91
IP_VID<1>\I	92	P92
RAM2_WEn\I	93	P93
DAC_VID<7>\I	94	P94
	95	GND
	96	VCCIO
DAC_VID<6>\I	97	P97
DAC_VID<5>\I	98	P98
DAC_VID<0>\I	99	P99
RAM2_A<10>\I	100	P100
RAM2_A<7>\I	101	P101
RAM2_A<9>\I	102	P102
RAM2_A<6>\I	103	P103
EPP_IOCHRDY\I	104	P104

TV VIDEO CONTROL

DRAWING

LAST_MODIFIED=Wed Mar 31 11:01:27 1999

OEC MEDICAL SYSTEMS, INC.

SIZE	DWG NO.	REV
D	00-881445	A

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05-017-9/93

*** Signal Cross-Reference ***
--- for the entire design --

+5V_SENSE	9A6
+12V_PCI	9D7
-12V_PCI	9C7
ACK *	7C3
AD <31..0>	1A8 1B8 1C8 1C7
AD_D0	2B5
AD_D1	2B5
AD_D2	2B5
AD_D3	2B5
AD_D4	2B5
AD_D5	2B5
AD_D6	2B5
AD_D7	2B5
AD_WREN *	2A5
AFDXT *	7C3
AUX_PIXWE_IN *	2A2
AUX_PIX_DATA <7..0>	2A2 8C7
BUSY	7C3
C/BE <3..0> *	1C8 1C7
CLK	1D8
COMP_VGA_VIDEO	7D5 3A1 4A1
CONFIG *	7B5 5D8 6D8 8D7
CONF_DATA	7B5 5D8 6D8 8D7
CONF_DCLK	7B5 5D8 6D8 8D7
CONF_DONE	5D6 6D6 8D5 7B5
CONF_STATUS *	5D6 6D6 8D5 7B5
DAC_VID <7..0>	8B5
DC_HDRV *	2A5
DC_VDRV *	2A5
DEL_VID <7..0>	8B7
DEVSEL *	1C8
EPC_JTAG_TDI	1A5 7B8
EPC_JTAG_TDO	7B5 1A6
EPP_IOCHRDY *	7D7 8C7
EPP_IRQ *	7D7 8C7
ERROR *	7C3
FRAME *	1C8
IDSEL	1C8
INIT	7C3
INTA *	1C8
IPCLK1	2D1 2D4
IPCLK2	2D1 3A8 4A8 8C3
IPCLK3	2D1 8B5 8C8 8D5 8D7
IPCLK4	2D1 1D2 6C8 6D3 6D4
IPCLK5	2D1 5C8 5D3 5D4
IP_DATA_TAG *	2A2
IP_DIS_PIXCLK	2D6
IP_HS *	2A2 5C8 6C8 8D7
IP_VID_OUT <7..0>	8A6
IP_VS *	2A2 5C8 6C8 8C7
IRDY *	1C8
JTAG_TCK	1A6 5D8 6D8 7A8 8D7
JTAG_TDI	1A6
JTAG_TDO	1A5 1A6
JTAG_TMS	1A6 5D8 6D8 7B8 8D7
JTAG_TRST *	1A6 5D8 6D8 8D7
LD_D0	2C5
LD_D1	2C5
LD_D2	2C5
LD_D3	2C5
LD_D4	2C5
LD_D5	2C5
LD_D6	2C5
LD_D7	2C5
LD_WREN *	2A5
LFPGA_LED	5B6 7B5
LFT_PIX_DATA <7..0>	2C2 5C8
LOCK *	1C8
LPT_RESET	1C2 7D7
L_AVDD	3C5

L_CONF_CE *	7A5 5D8
L_CONF_CEO *	5D6 7A6
L_DAC_BLANK *	5C6 3A8
L_DAC_HSYNC *	5C6 3A8
L_DAC_LCLK	5C6 3B8
L_DAC_RCLK	3A8 5C8
L_DAC_RD *	5C6 3B8
L_DAC_RESET *	5C6 3B8
L_DAC_VID <127..0>	5C6 3B6 3B7 3B8
L_DAC_VSYNC *	5C6 3A8
L_DAC_WR *	5C6 3B8
L_JTAG_TDI	1A5 5D8
L_JTAG_TDO	5D6 1A6
L_MR_ADR <11..0>	5A5
L_MR_BA <1..0>	5B5
L_MR_DQ <31..0>	5A5
L_MR_DQM <3..0>	5A5
L_PIXWE_IN *	2A2 5C8
L_SR_ADR <11..0>	5A5
L_SR_BA <1..0>	5A5
L_SR_DQ <31..0>	5A5
L_SR_DQM <3..0>	5A5
L_VGA <7..0>	3A5
L_VGA_SEL	5C6 3A1
PAR	1C8
PD0	7C3
PD1	7C3
PD2	7C3
PD3	7C3
PD4	7C3
PD5	7C3
PD6	7C3
PD7	7C3
PE	7D3
PERR *	1C8
PLX_ADR <23..0>	1B2 3B8 4B8 5C8 6C8 7D7 8C7
PLX_CS0 *	1C2 5C8 6C8 7C5 8C7
PLX_CS1 *	1C2 5C8 6C8 8C7
PLX_CS2 *	1C2 7D7 8C7
PLX_LA <27..2>	1B3 1C4
PLX_LBE <3..0>	1C2 1B3 5C8 6C8
PLX_LD <31..0>	1B4 1B5 1B6 1C2 3B8 4B8 7C4 7D7 5C8 6C8 8C7
PLX_LINT2 *	8C5 1D2
PLX_LRDY *	5C6 6C6 8C5 1C2
PLX_LRESET *	1D2 5D8 6C8 8D7
PLX_LWR_RD *	1D2 5C8 6C8 8C7
PLX_RD *	1D2 5C8 6C8 7D7
PLX_WR *	1D2 5C8 6C8 7D7 8C7
PRSNT2 *	1D8
RAM1_A <11..0>	8C5
RAM1_DQ <15..0>	8C5
RAM2_A <11..0>	8B5
RAM2_DQ <15..0>	8B5
RD_D0	2B5
RD_D1	2B5
RD_D2	2C5
RD_D3	2C5
RD_D4	2C5
RD_D5	2C5
RD_D6	2C5
RD_D7	2C5
RD_WREN *	2A5
RFPGA_LED	6A6 7B5
RHT_PIX_DATA <7..0>	2C2 6C8
RST *	1D8
R_AVDD	4C5
R_CONF_CE *	7A5 6D8
R_CONF_CEO *	6D6 7A6
R_DAC_BLANK *	6C6 4A8
R_DAC_HSYNC *	6C6 4A8
R_DAC_LCLK	6C6 4B8
R_DAC_RCLK	4A8 6C8

R_DAC_RD *	6C6 4B8
R_DAC_RESET *	6C6 4B8
R_DAC_VID <127..0>	6C6 4B6 4B7 4B8
R_DAC_VSYNC *	6C6 4A8
R_DAC_WR *	6C6 4B8
R_JTAG_TDI	1A5 6D8
R_JTAG_TDO	6D6 1A6
R_MR_ADR <11..0>	6A5
R_MR_BA <1..0>	6B5
R_MR_DQ <31..0>	6A5
R_MR_DQM <3..0>	6A5
R_PIXWE_IN *	2A2 6C8
R_SR_ADR <11..0>	6A5
R_SR_BA <1..0>	6A5
R_SR_DQ <31..0>	6A5
R_SR_DQM <3..0>	6A5
R_VGA <7..0>	4A5
R_VGA_SEL	6C6 4A1
SERR *	1C8
SLCT	7C3
SLCTI *	7C3
STOP *	1C8
STROBE *	7C3
TAG *	2A5
TRDY *	1C8
TV_CONF_CE *	7A5 8D7
TV_CONF_CEO *	8D5
TV_JTAG_TDI	1A5 8D7
TV_JTAG_TDO	8D5 1A6
TV_RSTR *	8A6
TV_RSTW *	8A6
V5CLK	7D2
VGA_CS	8C5 7C7
VGA_HD	7C7 8C7
VGA_VD	7C7 8C7

OEC MEDICAL SYSTEMS, INC.

SIZE	DWG NO.	REV
D	00-881445	A

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*** Unit Cross-Reference ***
--- for the entire design --

C1	CERSMT_1206	3C3
C2	CERSMT_1206	3C3
C3	TASMT_7343	3C3
C4	CERSMT_1206	3C4
C5	CERSMT_1206	3C1
C6	TASMT_7343	3C1
C7	TASMT_7343	3C2
C8	CERSMT_1206	2D4
C9	CERSMT_1206	3C2
C10	CERSMT_1206	3C2
C11	TASMT_7343	3C6
C12	CERSMT_1206	3C6
C13	TASMT_7343	4C5
C14	CERSMT_1206	4C4
C15	CERSMT_1206	4C4
C16	TASMT_7343	4C2
C17	CERSMT_1206	4C2
C18	CERSMT_1206	4C2
C19	TASMT_7343	4C3
C20	CERSMT_1206	4C3
C21	CERSMT_1206	4C3
C22	TASMT_7343	4C6
C23	CERSMT_1206	4C6
C24	TASMT_7343	10B6
C25	TASMT_7343	10B7
C26	CERSMT_1206	2D5
C27	CERSMT_1206	3C4
C28	TASMT_7343	3C3
C29	TASMT_7343	3C5
C30	CERSMT_1206	3C4
C31	CERSMT_1206	3C4
C32	CERSMT_1206	8C3
C33	CERSMT_1206	4C4
C34	CERSMT_1206	2D6
C35	CERSMT8DIP4X	2C6
C36	CERSMT8DIP4X	2C6
C37	CERSMT8DIP4X	2B6
C38	CERSMT8DIP4X	2B6
C39	CERSMT8DIP4X	2A6
C40	CERSMT8DIP4X	2A6
C41	CERSMT8DIP4X	2A6
C42	CERSMT8DIP4X	2A6
C43	TASMT_7343	10B7
C44	CERSMT_1206	10D5
C45	CERSMT_1206	10D5
C46	CERSMT_1206	10D2
C47	CERSMT_1206	10D5
C48	CERSMT_1206	10D2
C49	CERSMT_1206	10D3
C50	CERSMT_1206	10D5
C51	CERSMT_1206	10D6
C52	CERSMT_1206	7D3
C53	CERSMT_1206	7D2
C54	TASMT_7343	10B7
C55	CERSMT_1206	10D3
C56	CERSMT_1206	10D3
C57	CERSMT_1206	10D5
C58	CERSMT_1206	10D3
C59	CERSMT_1206	10D2
C60	CERSMT_1206	10D6
C61	CERSMT_1206	10D3
C62	CERSMT_1206	10D3
C63	CERSMT_1206	10D2
C64	CERSMT_1206	10D3
C65	CERSMT_1206	2D3
C66	TASMT_7343	10B7
C67	CERSMT_1206	7C3
C68	CERSMT_1206	7C3
C69	CERSMT_1206	7C3
C70	CERSMT_1206	2D3
C71	TASMT_7343	10B6
C72	CERSMT_1206	2D4
C73	CERSMT_1206	7C3
C74	CERSMT_1206	7C3
C75	CERSMT_1206	7C3
C76	CERSMT_1206	7C3
C77	CERSMT_1206	7C3
C78	TASMT_7343	9C6
C79	CERSMT_1206	9C6
C80	CERSMT_1206	9C5
C81	CERSMT_1206	9D6
C82	TASMT_7343	9D6
C83	CERSMT_1206	9D5
C84	TASMT_7343	10B6
C85	TASMT_7343	10B6
C86	TASMT_7343	10B6
C87	TASMT_7343	9A3
C88	TASMT_7343	9A4
C89	TASMT_7343	9A5
C90	TASMT_7343	9A5
C100	CERSMT_1206	10C8
C101	CERSMT_1206	10D7
C102	CERSMT_1206	10D6
C103	CERSMT_1206	10C7
C104	CERSMT_1206	10C6
C105	CERSMT_1206	10D6
C106	CERSMT_1206	10C6
C107	CERSMT_1206	10D6
C108	CERSMT_1206	10C5
C109	CERSMT_1206	10D5
C110	CERSMT_1206	10D6
C111	CERSMT_1206	10C6
C112	CERSMT_1206	4C4
C113	CERSMT_1206	4C5
C114	CERSMT_1206	4C5
C115	CERSMT_1206	4C5
C116	CERSMT_1206	4C5
C117	CERSMT_1206	10C7
C118	CERSMT_1206	10D8
C119	CERSMT_1206	4C3
C120	CERSMT_1206	4C3
C121	CERSMT_1206	8C2
C122	CERSMT_1206	8C2
C123	CERSMT_1206	3C3
C124	CERSMT_1206	3C3
C125	CERSMT_1206	3C4
C126	CERSMT_1206	3C5
C127	CERSMT_1206	3C5
C128	CERSMT_1206	3C5
C129	CERSMT_1206	3C5
C130	CERSMT_1206	10C8
C131	CERSMT_1206	10D7
C132	CERSMT_1206	10C7
C133	CERSMT_1206	10D7
C134	CERSMT_1206	10C8
C135	CERSMT_1206	10D7
C136	CERSMT_1206	10C6
C137	CERSMT_1206	10D6
C138	CERSMT_1206	4C4
C139	CERSMT_1206	10C8
C140	CERSMT_1206	10D8
C141	CERSMT_1206	10C7
C142	CERSMT_1206	10D8
C143	CERSMT_1206	10C7
C144	CERSMT_1206	10D7
C145	CERSMT_1206	10C8
C146	CERSMT_1206	10D7
C147	CERSMT_1206	4C2
C148	CERSMT_1206	4C2
C149	CERSMT_1206	8C1
C150	CERSMT_1206	8C1
C151	CERSMT_1206	8D3
C152	CERSMT_1206	3C2
C153	CERSMT_1206	3C2
C154	CERSMT_1206	3C4
C155	CERSMT_1206	10C7
C156	CERSMT_1206	10D7
C157	CERSMT_1206	10C7
C158	CERSMT_1206	10D7
C159	CERSMT_1206	10C7
C160	CERSMT_1206	10D7
C161	CERSMT_1206	10C3
C162	CERSMT_1206	10D5
C163	CERSMT_1206	10C4
C164	CERSMT_1206	10D5
C165	CERSMT_1206	10C4
C166	CERSMT_1206	10C5
C167	CERSMT_1206	10C3
C168	CERSMT_0805	10C4
C169	CERSMT_1206	10C2
C170	CERSMT_1206	10C8
C171	CERSMT_1206	8D3
C172	CERSMT_1206	10D8
C173	CERSMT_1206	8D2
C174	CERSMT_1206	10C6
C175	CERSMT_1206	10C3
C176	CERSMT_1206	10C5
C177	CERSMT_0805	10C3
C178	CERSMT_1206	10C4
C179	CERSMT_1206	10C7
C180	CERSMT_1206	10D7
C181	CERSMT_1206	10C6
C182	CERSMT_1206	10C5
C183	CERSMT_1206	10C3
C184	CERSMT_1206	10D4
C185	CERSMT_1206	10D5
C186	CERSMT_1206	10C4
C187	CERSMT_1206	10D5
C188	CERSMT_1206	10C2
C189	CERSMT_0805	10C3
C190	CERSMT_0805	10C4
C191	CERSMT_1206	10C3
C192	CERSMT_1206	10C4
C193	CERSMT_0805	10C3
C194	CERSMT_1206	10C3
C195	CERSMT_1206	10C5
C196	CERSMT_1206	10C2
C197	CERSMT_0805	10C2
C198	CERSMT_0805	10C3
C199	CERSMT_1206	10C3
C200	CERSMT_1206	10C4
C201	CERSMT_0805	10C2
C202	CERSMT_1206	10C2
C203	CERSMT_1206	10C3
C204	CERSMT_1206	10C8
C205	CERSMT_1206	10D8
C206	CERSMT_1206	10D6
C207	CERSMT_1206	10C3
C208	CERSMT_1206	10D5
C209	CERSMT_1206	10C5
C210	CERSMT_1206	10D4
C211	CERSMT_1206	10C5
C212	CERSMT_1206	10C5
C213	CERSMT_1206	10D4
C214	CERSMT_1206	10D4
C215	CERSMT_1206	10C5
C216	CERSMT_1206	10C4
C217	CERSMT_1206	10D3
C218	CERSMT_1206	10D5
C219	CERSMT_1206	10C5
C220	CERSMT_1206	10C5
C221	CERSMT_1206	10D4
C222	CERSMT_1206	10D6
C223	CERSMT_1206	10C6
C224	CERSMT_1206	10C5
C225	CERSMT_1206	10D4
C226	CERSMT_1206	10D5
C227	CERSMT_1206	10C4
C228	CERSMT_1206	10C4
C229	CERSMT_1206	10D4
C230	CERSMT_1206	10D5
C231	CERSMT_1206	10C6
C232	CERSMT_1206	10C4
C233	CERSMT_1206	10D4
C234	CERSMT_1206	10D5
C235	CERSMT_1206	10C4
C236	CERSMT_1206	10C3
C237	CERSMT_1206	10D4
C238	CERSMT_1206	10D3
C239	CERSMT_1206	10C4
C240	CERSMT_1206	10C5
C241	CERSMT_1206	10D4
C242	CERSMT_1206	10D5
C243	CERSMT_1206	10C6
C244	CERSMT_1206	10C4
C245	CERSMT_1206	10D5
C246	CERSMT_1206	10D3
C247	CERSMT_1206	10C5
C248	CERSMT_1206	10C4
C249	CERSMT_1206	10D6
C250	CERSMT_1206	10D4
C251	CERSMT_1206	10C3
C252	CERSMT_1206	10C5
C253	CERSMT_1206	10D5
C254	CERSMT_1206	10D4
C255	CERSMT_1206	10C5
C256	CERSMT_1206	10C5
C257	CERSMT_1206	10D4
C258	CERSMT_1206	10D3
C259	CERSMT_1206	10C7
C260	CERSMT_1206	10D8
C261	CERSMT_1206	10C7
C262	CERSMT_1206	10D7
C263	CERSMT_1206	10C6
C264	CERSMT_1206	10D7
C265	CERSMT_1206	10C7
C266	CERSMT_1206	10D7
C267	CERSMT_1206	10C3
C268	CERSMT_1206	10C4
C269	CERSMT_1206	10D4
C270	CERSMT_1206	10D4
C271	CERSMT_1206	10C5
C272	CERSMT_1206	10C4
C273	CERSMT_1206	10D3
C274	CERSMT_1206	10D4
C275	CERSMT_1206	10C7
C276	CERSMT_1206	10D7
C277	CERSMT_1206	10C7
C278	CERSMT_1206	10D7
C279	CERSMT_1206	10C6
C280	CERSMT_1206	10D6
C281	CERSMT_1206	10C8
C282	CERSMT_1206	10D8
C283	CERSMT_1206	10C7
C284	CERSMT_1206	10D6
C285	CERSMT_1206	9B7
C286	CERSMT_1206	10C7
C287	CERSMT_1206	10D8
C288	CERSMT_1206	9B7
C289	CERSMT_1206	10C6
C290	CERSMT_1206	10D7
C291	CERSMT_1206	9B7
C292	CERSMT_1206	9B7
CR1	DIO_SMT_BAV99	3B2
CR2	DIO_SMT_BAV99	3B2
CR3	DIO_SMT_BAV99	3B2
CR4	DIO_SMT_BAV99	8C1
CR5	DIO_SMT_BAV99	8C1
CR6	DIO_SMT_BAV99	8C1

CR7	DIO_SMT_BAV99	4B2
CR8	DIO_SMT_BAV99	4B2
CR9	DIO_SMT_BAV99	4B2
CR10	1N4005	3C5
CR11	1N4005	4C5
CR12	SCHOTTKY_SMT_BAT54C	7C6
DS1	LED4_67480200	7C4
DS2	LED4_67480201	7B4
E1	JMPST_1X3_90012601	7D6
FL1	EMI_FLTR_43600000	9A6
FL2	EMI_FLTR_43600000	7D2
FL3	EMI_FLTR_43600000	9C6
FL4	EMI_FLTR_43600000	9D6
L1	FR_BD_SMT_43610000	4C4
L2	FR_BD_SMT_43610000	4C4
L3	FR_BD_SMT_43610000	4C6
L4	FR_BD_SMT_43610000	3C6
L5	FR_BD_SMT_43610000	3C4
L6	FR_BD_SMT_43610000	3C4
P1	CONN_EDGE_PCI_124_5V	1A8 1A8 1A8 1B7 1B7 1B7 1B8 1B8 1B8 1C8 1D8 1D8 9A8 9B8 9B8 9B8 9C8 9C8 9C8 9D8
P2	MINJRRA_2X4_51411109	9A6
P3	CONN_SMBH_AG_58019880	3B1
P4	CONN_SMBH_AG_58019880	3B1
P5	CONN_SMBH_AG_58019880	3B1
P6	CONN_SMBH_AG_58019880	4B1
P7	CONN_SMBH_AG_58019880	4B1
P8	CONN_SMBH_AG_58019880	4B1
P9	D50RA_80P_51180008	2A6 2A6 2A6 2B6 2B6 2B6 2B7 2B7 2B7 2B7 2C6 2C6 2C6 2C7 2C7 2C7 2C7 2C7 2D7
P10	HDBKST_2X5_90012602	7B8
P11	DSUBRA_25_CHAS_51109724	7C2 7C2 7D2
P12	CONN_SMBH_AG_58019880	8C1
P13	CONN_SMBH_AG_58019880	8C1
P14	CONN_SMBH_AG_58019880	8C1
P15	DSUBRA_15_HD_NC_51970020	7C8
P16	HDBKST_2X5_90012602	1A7
R1	RESSMT_1206	3C1
R2	RESSMT_1206	3A6
R3	RESSMT_1206	2D4
R4	RESSMT8DIP4X	3C7
R5	RESSMT_1206	3B4
R6	RESSMT_1206	3B3
R7	RESSMT_1206	3B2
R8	RESSMT_1206	3C6
R9	RESSMT_1206	3B2
R10	RESSMT_1206	3B4
R11	RESSMT_1206	3B2
R12	RESSMT_1206	3C3
R13	RESSMT_1206	8B2
R14	RESSMT_1206	3B3
R15	RESSMT_1206	3B3
R16	RESSMT_1206	8C2
R17	RESSMT_1206	8C1
R18	RESSMT_1206	8D2
R19	RESSMT_1206	4B4
R20	RESSMT_1206	8C1
R21	RESSMT_1206	4C3
R22	RESSMT_1206	4B3
R23	RESSMT_1206	4B3
R24	RESSMT_1206	4B3
R25	RESSMT_1206	4B2
R26	RESSMT_1206	4B2
R27	RESSMT_1206	4B2
R28	RESSMT_1206	4A5
R29	RESSMT8DIP4X	4C7
R30	RESSMT_1206	7B4
R31	RESSMT_1206	7B4
R32	RESSMT_1206	4B4
R33	RESSMT_1206	4B3
R34	RESSMT_1206	4C6
R35	RESSMT_1206	7B4
R36	RESSMT8DIP4X	2C6
R37	RESSMT8DIP4X	2C6
R38	RESSMT8DIP4X	2B6
R39	RESSMT8DIP4X	2B6
R40	RESSMT8DIP4X	2B6
R41	RESSMT8DIP4X	2B6
R42	RESSMT8DIP4X	2A6
R43	RESSMT8DIP4X	2A6
R44	RESSMT_1206	2D5
R45	RESSMT8DIP4X	7B5
R46	RESSMT8DIP4X	7A7
R47	RESSMT_1206	7B4
R48	RESSMT_1206	3C3
R49	RESSMT8DIP4X	3C7
R50	RESSMT_1206	3B4
R51	RESSMT_1206	3C4
R52	RESSMT_1206	3C4
R53	RESSMT_1206	3B3
R54	RESSMT_1206	8D3
R55	RESSMT_1206	3B3
R56	RESSMT_1206	8B2
R57	RESSMT_1206	4B3
R58	RESSMT_1206	8B3
R59	RESSMT8DIP4X	4C7
R60	RESSMT_1206	4B4
R61	RESSMT_1206	4C4
R62	RESSMT_1206	4C4
R63	RESSMT_1206	2D6
R64	RESSMT8DIP4X	2D6
R65	RESSMT_1206	1A6
R66	RESSMT_1206	1A6
R67	RESSMT_1206	1A6
R68	RESSMT_1206	1A7
R69	RESSMT_1206	7C6
R70	RESSMT_1206	7C6
R71	RESSMT_1206	7C6
R72	RESSMT_1206	7C7
R73	RESSMT_1206	7B7
R74	RESSMT_1206	7B7
R75	RESSMT_1206	7B7
R76	RESSMT_1206	7B7
R77	RESSMT_1206	5D7
R78	RESSMT_1206	8C3
R79	RESSMT_1206	8B3
R80	RESSMT_1206	8B2
R81	RESSMT_1206	6D7
R82	RESSMT_1206	8D6
R83	RESSMT_1206	7C7
R84	RESSMT_1206	7C6
R85	RESSMT_1206	7C6
R86	RESSMT_1206	7D3
R87	RESSMT_1206	7D3
R88	RESSMT_1206	1A6
R89	RESSMT_1206	7D4
R90	RESSMT8DIP4X	1B4
R91	RESSMT8DIP4X	1B4
R92	RESSMT_1206	5C4
R93	RESSMT_1206	2D3
R94	RESSMT_1206	5B2
R95	RESSMT_1206	5C2
R96	RESSMT_1206	6A2
R97	RESSMT_1206	6C4
R98	RESSMT_1206	6C2
R99	RESSMT_1206	7C3
R100	RESSMT_1206	7C3
R101	RESSMT_1206	7C3
R102	RESSMT8DIP4X	1B7
R103	RESSMT8DIP4X	1D5
R104	RESSMT8DIP4X	1D5
R105	RESSMT8DIP4X	1D5
R106	RESSMT_1206	2D3
R107	RESSMT8DIP4X	1B5
R108	RESSMT8DIP4X	1B5
R109	RESSMT8DIP4X	1B5
R110	RESSMT8DIP4X	1B5
R111	RESSMT8DIP4X	8B4
R112	RESSMT_1206	8D4
R113	RESSMT_1206	8C7
R114	RESSMT_1206	2D4
R115	RESSMT_1206	7C3
R116	RESSMT_1206	7C3
R117	RESSMT_1206	7C3
R118	RESSMT_1206	7C3
R119	RESSMT_1206	7C3
R120	RESSMT8DIP4X	1B6
R121	RESSMT8DIP4X	1B6
R122	RESSMT_1206	9A4
R123	RESSMT_1206	9A4
R124	RESSMT_1206	9A4
R125	RESSMT_1206	9A5
TP1	TEST_POINT_COLOR	3D2
TP2	TEST_POINT_COLOR	9B6
TP3	TEST_POINT_COLOR	3D3
TP4	TEST_POINT_COLOR	3D5
TP5	TEST_POINT_COLOR	3B6
TP6	TEST_POINT_COLOR	3B5
TP7	TEST_POINT_COLOR	3B4
TP8	TEST_POINT_COLOR	3B4
TP9	TEST_POINT_COLOR	3D6
TP10	TEST_POINT_COLOR	3C1
TP11	TEST_POINT_COLOR	8C1
TP12	TEST_POINT_COLOR	4B5
TP13	TEST_POINT_COLOR	4D5
TP14	TEST_POINT_COLOR	4A6
TP15	TEST_POINT_COLOR	4C1
TP16	TEST_POINT_COLOR	4B4
TP17	TEST_POINT_COLOR	4B4
TP18	TEST_POINT_COLOR	4D6
TP19	TEST_POINT_COLOR	3D2
TP20	TEST_POINT_COLOR	9D7
TP21	TEST_POINT_COLOR	9B7
TP22	TEST_POINT_COLOR	9A5
TP23	TEST_POINT_COLOR	9A4
TP24	TEST_POINT_COLOR	9B7
TP25	TEST_POINT_COLOR	3D5
TP26	TEST_POINT_COLOR	5B6
TP27	TEST_POINT_COLOR	5B6
TP28	TEST_POINT_COLOR	9B7
TP29	TEST_POINT_COLOR	6B6
TP30	TEST_POINT_COLOR	6B6
TP31	TEST_POINT_COLOR	4D5
TP32	TEST_POINT_COLOR	2D5
TP33	TEST_POINT_COLOR	9B7
TP34	TEST_POINT_COLOR	9B7
TP35	TEST_POINT_COLOR	9B6
TP36	TEST_POINT_COLOR	7D6
TP37	TEST_POINT_COLOR	9B6
TP38	TEST_POINT_COLOR	9B7
TP39	TEST_POINT_COLOR	1D6
TP40	TEST_POINT_COLOR	1D4
TP41	TEST_POINT_COLOR	7D7
TP42	TEST_POINT_COLOR	9B6
TP43	TEST_POINT_COLOR	1D4
TP44	TEST_POINT_COLOR	1D4
TP45	TEST_POINT_COLOR	1D3
TP46	TEST_POINT_COLOR	1D3
TP47	TEST_POINT_COLOR	1D4
TP48	TEST_POINT_COLOR	9B7
TP49	TEST_POINT_COLOR	9B6
U1	7805	3C3
U2	78L05	3C4
U3	7905	3C2
U5	MAX499	3C3
U6	MAX499	8C2
U7	BT121VCC	8D3
U8	MAX499	4C3
U9	78L05	4C4
U11	49FCT3806	2D5
U12	74LCX16374	2B4
U13	EPC2_VCC	7B6
U14	74LCX16374	2A4
U15	EPC2_VCC	7B7
U16	74ABT240	7C5
U17	CA3246	7C6
U21	ST78C36	7D4
U22	NM93CS46	1B6
U23	SDRAM_64MBIT_62610288	5D4
U24	SDRAM_64MBIT_62610288	5C4
U25	SDRAM_64MBIT_62610288	5D2
U26	SDRAM_64MBIT_62610288	5C2
U27	LT1086	9A4
U28	SDRAM_64MBIT_62610288	6D4
U29	SDRAM_64MBIT_62610288	6C4
U30	LT1086	9A5
U31	SDRAM_64MBIT_62610288	6D2
U32	SDRAM_64MBIT_62610288	6C2
U33	SDRAM_64MBIT_62610288	8D4
U34	SDRAM_64MBIT_62610288	8B4
U35	485506	8C7
VR1	LM285_1X2V	3C6
VR2	LM285_1X2V	4C6
VR3	LM285_1X2V	3C6
VR4	LM285_1X2V	4C6
XE1	SHORT_PC_X1	3C4
XE2	SHORT_PC_X1	7C5
Y1	OSC_8P_EN_VCC_10TTL	7D3

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